

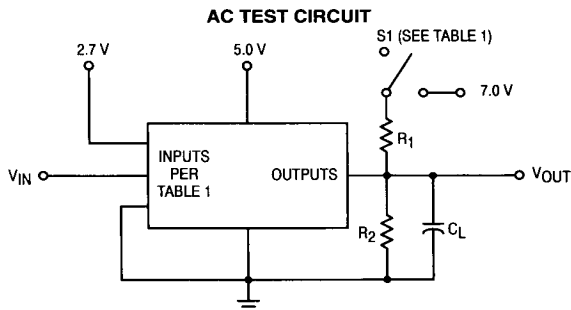
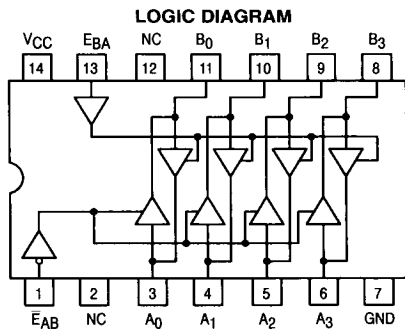


Quad Non-Inverting Bus Transceivers With 3-State Outputs

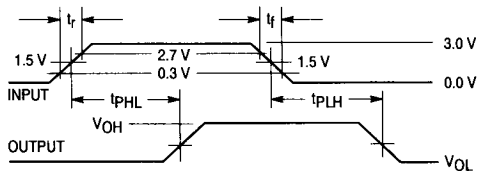
ELECTRICALLY TESTED PER:
MIL-M-38510/34802

The 54F243 is a Quad Bus Transmitter/Receivers designed for 4-line asynchronous 2-way data communications between data buses.

- 2-Way Asynchronous Data Bus Communication
- Input Clamp Diodes Limit High Speed Termination Effects



PROPAGATION DELAY TIMES



NOTES:

1. Pulse generator has the following characteristics: $t_r = t_f \leq 2.5$ ns, PRR = 1.0 MHz and $Z_{OUT} = 50 \Omega$.
2. $C_L = 50$ pF $\pm 10\%$ including scope probe, wiring and stray capacitance, without package in test fixture.
3. Voltage measurements are to be made with respect to network ground terminal.
4. $R_1 = R_2 = 500 \Omega \pm 5.0\%$.
5. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).

Military 54F243



AVAILABLE AS:

- 1) JAN: JM38510/34802BXA
- 2) SMD: 5962-8683401
- 3) 883: 54F243/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
EAB	1	1	2	VCC
NC	2	2	3	VCC
A ₀	3	3	4	OPEN
A ₁	4	4	6	OPEN
A ₂	5	5	8	OPEN
A ₃	6	6	9	OPEN
GND	7	7	10	GND
B ₃	8	8	12	OPEN
B ₂	9	9	13	OPEN
B ₁	10	10	14	OPEN
B ₀	11	11	16	OPEN
NC	12	12	18	VCC
EBA	13	13	19	VCC
VCC	14	14	20	VCC

BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

Inputs		Output	Inputs		Output
EAB	D		EBA	D	
L	L	L	X	(Z)	
L	H	H	L	(Z)	
H	X	(Z)	H	L	H
H	X	(Z)	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

MOTOROLA MILITARY FAST/LS/TTL DATA

4-113

ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

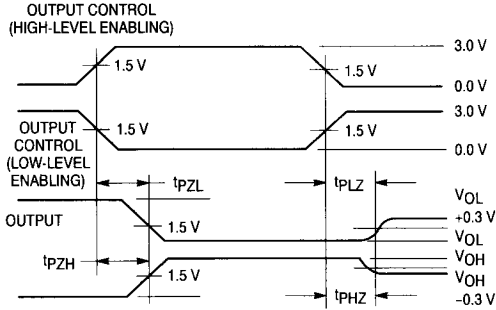


Table 1

Test Type	S1
tPLH	open
tPHL	open
tPHZ	open
tPZH	open
tPLZ	closed
tPZL	closed

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
VOH	Logical "1" Output Voltage	2.4		2.4		2.4		V	VCC = 4.5 V, IOH = -3.0 mA, VIN = 2.0 V or 0.8 V per Truth Table.
VOH1	Logical "1" Output Voltage	2.0		2.0		2.0		V	VCC = 4.5 V, IOH = -12 mA, VIN = 2.0 V or 0.8 V per Truth Table.
VOL	Logical "0" Output Voltage		0.55		0.55		0.55	V	VCC = 4.5 V, IOL = 48 mA, VIN = 2.0 V or 0.8 V per Truth Table.
VIC	Input Clamping Voltage		-1.2					V	VCC = 4.5 V, IIN = -18 mA, other inputs are open.
IiH1	Logical "1" Input Current		20		20		20	µA	VCC = 5.5 V, VIH = 2.7 V, other inputs are open.
IiH2	Logical "1" Input Current		100		100		100	µA	VCC = 5.5 V, VIN = 7.0 V, other inputs are open.
IiH3	Logical "1" Input Current		1.0		1.0		1.0	mA	VCC = 5.5 V, VIN = 5.5 V, (all inputs).
IiL	Logical "0" Input Current	-0.03	-1.0	-0.03	-1.0	-0.03	-1.0	mA	VCC = 5.5 V, VIN = 0.5 V, other inputs are open.
IOS	Output Short Circuit Current	-100	-325	-100	-325	-100	-325	mA	VCC = 5.5 V, VIN = 0 V or 5.5 V, VOUT = 0 V or 5.5 V (depending on input).
IIOZH	Output Off Current High		70		70		70	µA	VCC = 5.5 V, VIN = 2.0 V, other input = 0.8 V, VOUT = 0 V or 2.7 V.
IIOZL	Output Off Current Low	-0.06	-1.6	-0.06	-1.6	-0.06	-1.6	mA	VCC = 5.5 V, VIN = 2.0 V, other input = 0.8 V, VOUT = 0.5 V or 5.5 V.
ICCH	Power Supply Current		80		80		80	mA	VCC = 5.5 V, VIN = 5.5 V or 0 V (both inputs).
ICCL	Power Supply Current		92		92		92	mA	VCC = 5.5 V, VIN = 5.5 V or 0 V (both inputs).
IC CZ	Power Supply Current Off		90		90		90	mA	VCC = 5.5 V, VIN = 5.5 V, other input = 0 V.
VIH	Logical "1" Input Voltage	2.0		2.0		2.0		V	VCC = 4.5 V.
VIL	Logical "0" Input Voltage		0.8		0.8		0.8	V	VCC = 4.5 V.

54F243

Symbol	Parameter	Limits			Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C	+ 125°C	- 55°C		
	Functional Tests	Subgroup 7	Subgroup 8A	Subgroup 8B		per Truth Table with $V_{CC} = 4.5$ V, (Repeat at), $V_{CC} = 5.5$ V, $V_{INL} = 0.55$ V, $V_{INH} = 2.5$ V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
	Switching Parameters:	Min	Max	Min	Max	Min	Max		
t _{PHL1}	Propagation Delay /Data-Output B _n to A _n	1.5	5.2	1.0	8.5	1.0	8.5	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = R_2 = 500$ Ω, with switch S1 open.
t _{PLH1}	Propagation Delay /Data-Output B _n to A _n	1.5	5.2	1.0	6.5	1.0	6.5	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = R_2 = 500$ Ω, with switch S1 open.
t _{PHL2}	Propagation Delay /Data-Output A _n to B _n	1.5	5.2	1.0	8.5	1.0	8.5	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = R_2 = 500$ Ω.
t _{PLH2}	Propagation Delay /Data-Output A _n to B _n	1.5	5.2	1.0	6.5	1.0	6.5	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = R_2 = 500$ Ω.
t _{PLZ1}	Propagation Delay /Data-Output EBA to A _n	2.5	6.0	2.0	8.5	2.0	8.5	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = R_2 = 500$ Ω, with switch S1 closed.
t _{PHZ1}	Propagation Delay /Data-Output EBA to A _n	2.5	6.0	2.0	7.5	2.0	7.5	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = R_2 = 500$ Ω, with switch S1 open.
t _{PZL1}	Propagation Delay /Data-Output EBA to A _n	2.5	7.5	2.0	10.5	2.0	10.5	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = R_2 = 500$ Ω, with switch S1 closed.
t _{PZH1}	Propagation Delay /Data-Output EBA to A _n	2.5	5.7	2.0	8.0	2.0	8.0	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = R_2 = 500$ Ω, with switch S1 open.
t _{PLZ2}	Propagation Delay /Data-Output EAB to B _n	2.5	6.0	2.0	8.5	2.0	8.5	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = R_2 = 500$ Ω.
t _{PHZ2}	Propagation Delay /Data-Output EAB to B _n	2.5	6.0	2.0	7.5	2.0	7.5	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = R_2 = 500$ Ω.
t _{PZL2}	Propagation Delay /Data-Output EAB to B _n	2.5	7.5	2.0	10.5	2.0	10.5	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = R_2 = 500$ Ω.
t _{PZH2}	Propagation Delay /Data-Output EAB to B _n	2.5	5.7	2.0	8.0	2.0	8.0	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = R_2 = 500$ Ω.

4