PRELIMINARY | Data Sheet | February 28, 2006 | FN7488.0

Programmable 18-Channel Gamma with 1-Channel V_{COM} with Reference

The EL5625 represents a high integration programmable buffer solution from Intersil. The device integrates 18-channels of programmable buffers, with a single programmable V_{COM}, a reference output, and a supply side LDO.

The 18-channel programmable buffers have 11-bit resolution and rail-to-rail outputs. Each output is capable of driving 15mA continuous.

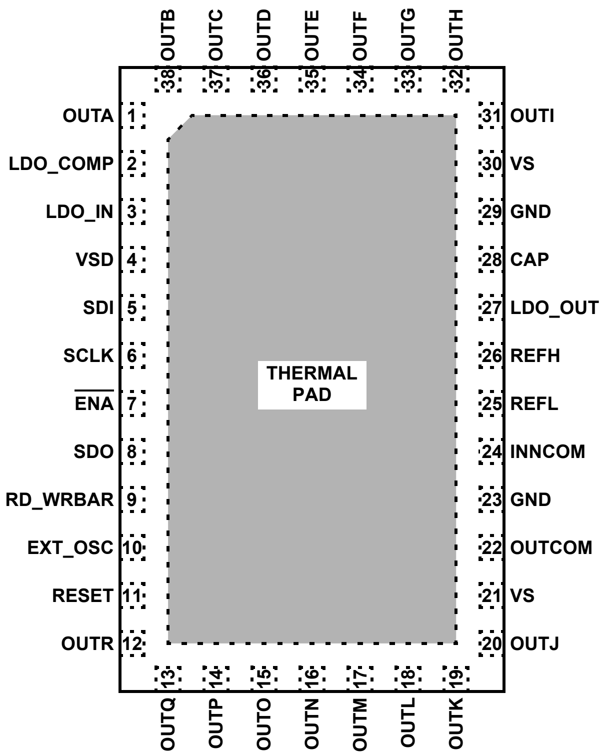
The V_{COM} output also features 11-bits of resolution. The generated voltage is connected to the non-inverting input of the integrated V_{COM} amplifier. This amplifier has a short-circuit current of 1A, 100mA continuous.

The integrated low drop-out regulator is used, in conjunction with an external transistor, to provide a solid supply voltage to the device. It features 200mV minimum drop-out and has very good load regulation for the cleanest gamma and V_{COM} outputs.

The EL5625 also includes over-temperature protection and is available in a 38-pin QFN package.

Pinout

EL5625
(38-PIN QFN)
TOP VIEW



Features

- 18-channel programmable gamma
  - Rail-to-rail
- Single V_{COM} amplifier
  - 1A peak output
- 11-bit resolution per output
- Accuracy ±0.5%
- Integrated supply LDO
  - Low drop out - 200mV
- Integrated reference
  - Very accurate - 0.75%
- +7V to +16V supply
- Thermal protection
- 38-pin QFN
- Pb-Free plus anneal available (RoHS compliant)

Applications

- LCD-TVs
- Flat panel monitors
- TFT-LCD displays

Ordering Information

PART NUMBER (See Note)	PACKAGE (Pb-Free)	TAPE & REEL	PKG. DWG. #
EL5625ILZ	38-Pin QFN	-	MDP0046
EL5625ILZ-T13	38-Pin QFN	13”	MDP0046

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_S and GND . . . . . 4.5V(min) to 18V(max)
Supply Voltage between V_{SD} and GND 3V(min) to V_S and +7(max)
Maximum Continuous Output Current (Gamma) 15mA
Maximum Continuous Output Current (V_{COM}) 100mA
Ambient Operating Temperature . . . . -40°C to +85°C
Maximum Die Temperature . . . . +125°C
Storage Temperature . . . . -65°C to +150°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S = 15V, V_{SD} = 5V, V_{REFH} = 13V, V_{REFL} = 2V, R_L = 1.5kΩ and C_L = 200pF to 0V, T_A = 25°C, unless otherwise specified.

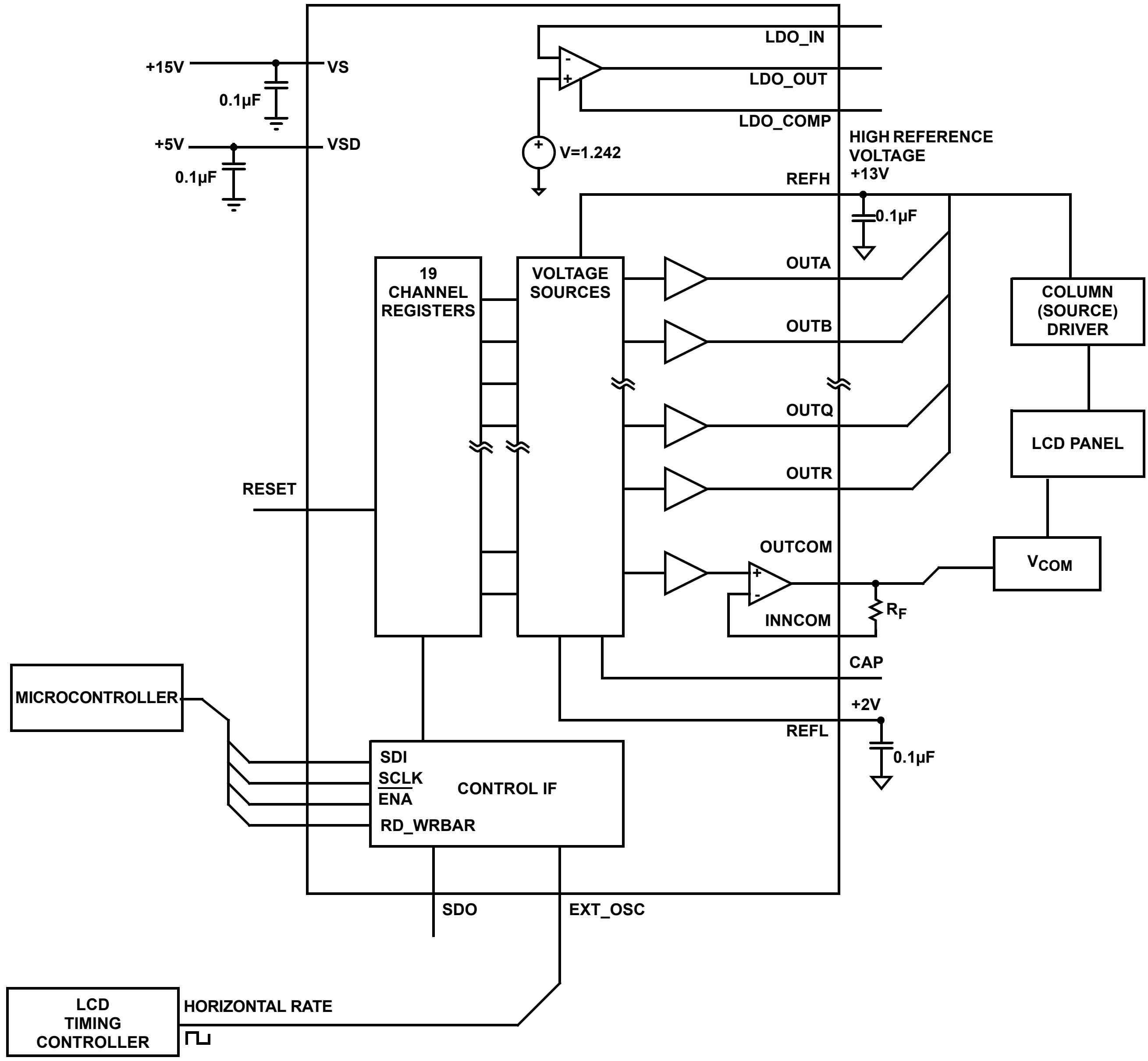
PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_S	Supply Current	No load		11	15	mA
I_{SD}	Digital Supply Current			1.1	1.35	mA
ANALOG						
V_{OL}	Output Swing Low (Chan 1-16)	Sinking 5mA (V_{REFH} = 15V, V_{REFL} = 0)		100	200	mV
	Output Swing Low (Chan 17, 18)			50	150	mV
V_{OH}	Output Swing High (Chan 1, 2)	Sourcing 5mA (V_{REFH} = 15V, V_{REFL} = 0)	14.85	14.95		V
	Output Swing High (Chan 3-18)		14.8	14.9		V
I_{SC}	Short Circuit Current	R_L = 10Ω	100	130		mA
PSRR	Power Supply Rejection Ratio	V_S+ is moved from 14V to 16V	50	70		dB
		V_{COM}	45	60		dB
t_D	Program to Out Delay			4		ms
V_{AC}	Accuracy Referred to the Ideal Value	Code = 512		20		mV
ΔV_{MIS}	Channel to Channel Mismatch	Code = 512		2		mV
V_{DROOP}	Droop Voltage			1	2	mV/ms
R_{INH}	Input Resistance @ V_{REFH}, V_{REFL}		25	32		kΩ
REG	Load Regulation	I_{OUT} = 5mA step		1	3	mV/mA
BG	Band Gap		1.227	1.242	1.257	V
DIGITAL						
V_{IH}	Logic 1 Input Voltage		2			V
V_{IL}	Logic 0 Input Voltage				1	V
F_{CLK}	Clock Frequency			5		MHz
t_S	Setup Time			20		ns
t_H	Hold Time			20		ns
t_{LC}	Load to Clock Time			20		ns
t_{CE}	Clock to Load Line			20		ns
t_{DCO}	Clock to Out Delay Time	Negative edge of SCLK		10		ns
R_{SDIN}	S_{DIN} Input Resistance			1		GΩ
T_{PULSE}	Minimum Pulse Width for EXT_OSC Signal			5		µs
Duty Cycle	Duty Cycle for EXT_OSC Signal			50		%

Electrical Specifications

V_S = 15V, V_{SD} = 5V, V_{REFH} = 13V, V_{REFL} = 2V, R_L = 1.5kΩ and C_L = 200pF to 0V, T_A = 25°C, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
F_OSC	Internal Refresh Oscillator Frequency	OSC_Select = 0		21		kHz
INL	Integral Nonlinearity Error			1.3		LSB
DNL	Differential Nonlinearity Error			0.5		LSB
V_{COM} CHARACTERISTICS						
BW	Bandwidth of V_{COM}			10		MHz
SR	Slew Rate		5	9		V/µs
I_{SC}	Short-Circuit Current			1000		mA

Typical Application Diagram



Pin Descriptions

PIN NUMBER	PIN NAME	PIN TYPE	PIN DESCRIPTION
1	OUTA	Analog Output	Channel A output voltage
2	LDO_COMP	Analog Input	LDO compensation capacitor
3	LDO_IN	Analog Input	LDO inverting input
4	VSD	Power	Positive power supply for digital circuits (3.3V - 5V)
5	SDI	Logic Input	Serial data input
6	SCLK	Logic Input	Serial data clock
7	$\overline{\text{ENA}}$	Logic Input	Chip select, low enables data input to logic
8	SDO	Logic Output	Serial data output
9	RD_WRBAR	Analog Input	Read, write select: “0” = write, “1” = read
10	EXT_OSC	Input/Output	Oscillator pin for synchronizing
11	RESET	Analog Input	Reset all registers: “0” = reset
12	OUTR	Analog Output	Channel R output voltage
13	OUTQ	Analog Output	Channel Q output voltage
14	OUTP	Analog Output	Channel P output voltage
15	OUTO	Analog Output	Channel O output voltage
16	OUTN	Analog Output	Channel N output voltage
17	OUTM	Analog Output	Channel M output voltage
18	OUTL	Analog Output	Channel L output voltage
19	OUTK	Analog Output	Channel K output voltage
20	OUTJ	Analog Output	Channel J output voltage
21, 30	VS	Power	Positive supply voltage for analog circuits (4.5V - 16.5V)
22	OUTCOM	Analog Output	V_{COM} output
23, 29	GND	Power	Ground
24	INNCOM	Analog Input	V_{COM} inverting input
25	REFL	Analog Input	Low reference voltage
26	REFH	Analog Input	High reference voltage
27	LDO_OUT	Analog Output	LDO output
28	CAP	Analog	Decoupling capacitor for internal reference
31	OUTI	Analog Output	Channel I output voltage
32	OUTH	Analog Output	Channel H output voltage
33	OUTG	Analog Output	Channel G output voltage
34	OUTF	Analog Output	Channel F output voltage
35	OUTE	Analog Output	Channel E output voltage
36	OUTD	Analog Output	Channel D output voltage
37	OUTC	Analog Output	Channel C output voltage
38	OUTB	Analog Output	Channel B output voltage

Typical Performance Curves

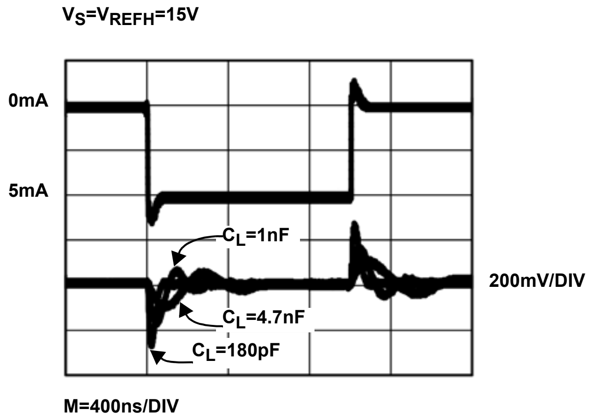


FIGURE 1. TRANSIENT LOAD REGULATION (SOURCING)

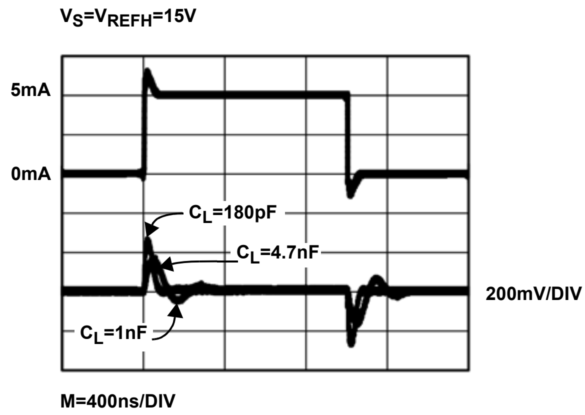


FIGURE 2. TRANSIENT LOAD REGULATION (SINKING)

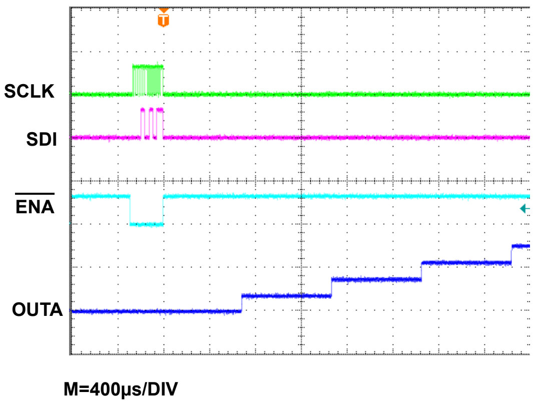


FIGURE 3. LARGE SIGNAL RESPONSE (RISING FROM 0V TO 8V)

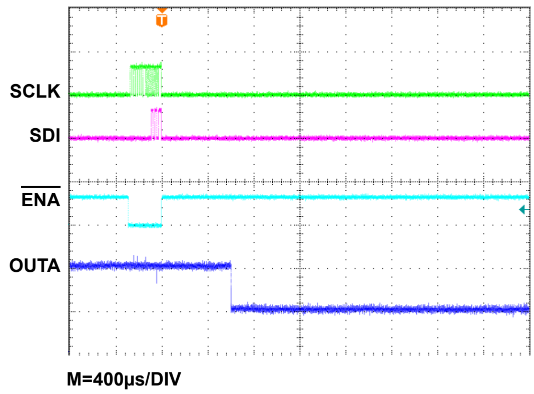


FIGURE 4. SMALL SIGNAL RESPONSE (FALLING FROM 200mV TO 100mV)

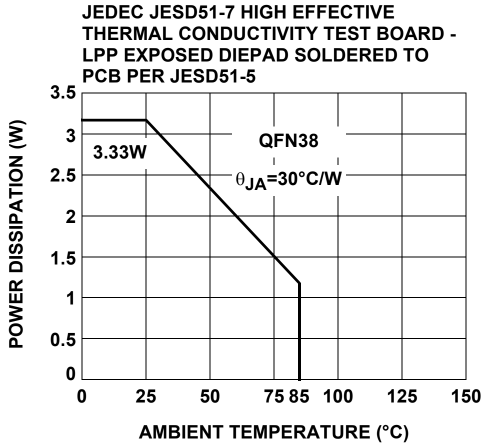


FIGURE 5. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

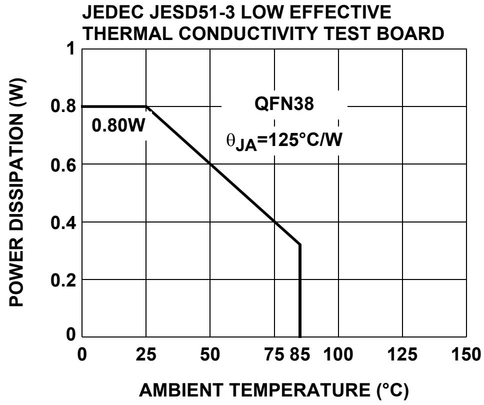


FIGURE 6. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

General Description

The EL5625 is designed to produce the reference voltages required in TFT-LCD applications. Each output is programmed to the required voltage with 11 bits of resolution. Ref-High and Ref-Low pins determine the high and low voltages of the output range. These outputs can be driven to within 50mV of the power rails of the EL5625. Programming of each output, 18 buffers and 1 Vcom, is performed using the USB interface.

USB Interface

The EL5625 uses USB interface to control the 18 Gamma channels and Vcom channel (Figure 7). Software is available for download on Intersil's website.

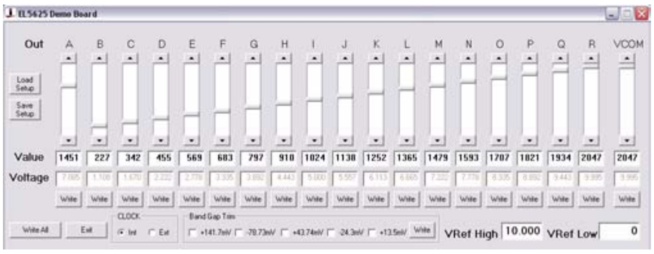


FIGURE 7. USB INTERFACE

Serial Interface

The EL5625 is programmed through a three-wire serial interface. The start and stop conditions are defined by the $\overline{\text{ENA}}$ signal. While the $\overline{\text{ENA}}$ is low, the data on the SDI (serial data input) pin is shifted into the 16-bit shift register on the positive edge of the SCLK (serial clock) signal. The MSB (bit 15) is loaded first and the LSB (bit 0) is loaded last (see Table 1). After the full 16-bit data has been loaded, the $\overline{\text{ENA}}$ is pulled high and the addressed output channel is updated. The SCLK is disabled internally when the $\overline{\text{ENA}}$ is high. The SCLK must be low before the $\overline{\text{ENA}}$ is pulled low.

The Serial Timing Diagram and parameters table show the timing requirements for three-wire signals.

The serial data has a minimum length of 16 bits, the MSB (most significant bit) is the first bit in the signal. The bits are allocated to the following functions (also refer to the Control Bits Logic Table).

- Bits 15 through 11 select the channel to be written to, these are binary coded with channel A = 0, and channel R = 17
- The 11-bit data is on bits 10 through 0. Some examples of data words are shown in the table of Serial Programming Examples

TABLE 1. CONTROL BITS LOGIC TABLE

BIT	NAME	DESCRIPTION
B15	A4	Channel Address
B14	A3	Channel Address
B13	A2	Channel Address
B12	A1	Channel Address
B11	A0	Channel Address
B10	D10	Data
B9	D9	Data
B8	D8	Data
B7	D7	Data
B6	D6	Data
B5	D5	Data
B4	D4	Data
B3	D3	Data
B2	D2	Data
B1	D1	Data
B0	D0	Data

Serial Timing Diagram

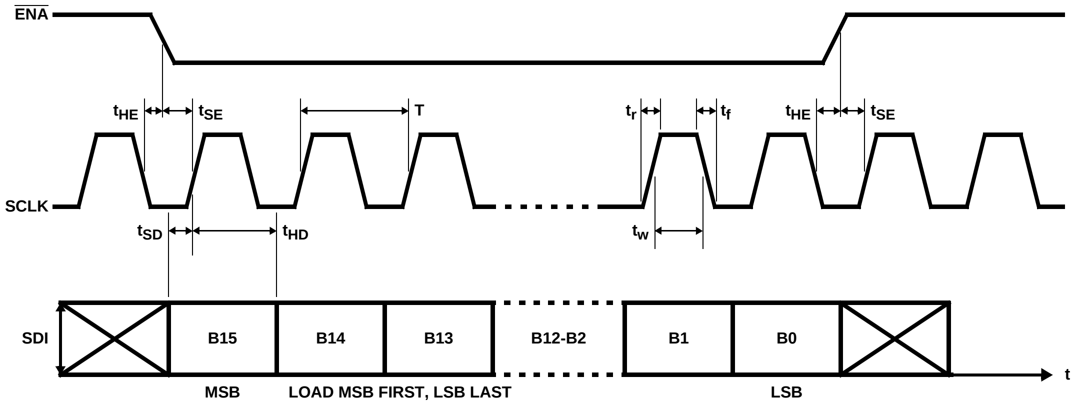


TABLE 2. SERIAL TIMING PARAMETERS

PARAMETER	RECOMMENDED OPERATING RANGE	DESCRIPTION
T	≥200ns	Clock Period
t_r/t_f	0.05 * T	Clock Rise/Fall Time
t_{HE}	≥10ns	$\overline{ENA}$ Hold Time
t_{SE}	≥10ns	$\overline{ENA}$ Setup Time
t_{HD}	≥10ns	Data Hold Time
t_{SD}	≥10ns	Data Setup Time
t_W	0.50 * T	Clock Pulse Width

V_{COM} Amplifier

The V_{COM} amplifier is designed to control the voltage on the back plate of an LCD display. This plate is capacitively coupled to the pixel drive voltage which alternately cycles positive and negative at the line rates for the display. Thus the amplifier must be capable of sourcing and sinking capacitive pulse of current, which can be quite large (100mA for typical applications).

Analog Section

TRANSFER FUNCTION

The transfer function is:

$$V_{OUT(IDEAL)} = V_{REFL} + \frac{data}{2048} \times (V_{REFH} - V_{REFL})$$

where data is the decimal value of the 11-bit data binary input code.

The output voltages from the EL5625 will be derived from the reference voltages present at the V_{REFL} and V_{REFH} pins. The impedance between those two pins is about 32kΩ.

Care should be taken that the system design holds these two reference voltages within the limits of the power rails of the EL5625. GND < $V_{REFH} \le V_S$ and GND $\le V_{REFL} \le V_{REFH}$.

CLOCK OSCILLATOR

The EL5625 requires an internal clock or external clock to refresh its outputs. The outputs are refreshed at the falling OSC clock edges. The output refreshed switches open at the rising edges of the OSC clock. The driving load shouldn't be changed at the rising edges of the OSC clock. Otherwise, it will generate a voltage error at the outputs. This clock may be input or output via the clock pin labelled EXT_OSC. The internal clock is provided by an internal oscillator running at approximately 21kHz and can be output to the EXT_OSC pin. In a 2 chip system, if the driving loads are stable, one chip may be programmed to use the internal oscillator; then the OSC pin will output the clock from the internal oscillator. The second chip may have the OSC pin connected to this clock source.

For transient load application, the external clock mode should be used to ensure all functions are synchronized together. The positive edge of the external clock to the OSC pin should be timed to avoid the transient load effect. The Application Drawing shows the LCD H rate signal used, here the positive clock edge is timed to avoid the transient load of the column driver circuits.

After power on, the chip will start with the internal oscillator mode. At this time, the EXT_OSC pin will be in a high impedance condition to prevent contention. By setting pin 10 to high, the chip is on external clock mode. Setting pin 10 to low, the chip is on internal clock mode.

CHANNEL OUTPUTS

Each of the channel outputs has a rail-to-rail buffer. This enables all channels to have the capability to drive to within 50mV of the power rails, (see Electrical Characteristics for details).

When driving large capacitive loads, a series resistor should be placed in series with the output (Usually between 5Ω and 50Ω).

Each of the channels is updated on a continuous cycle, the time for the new data to appear at a specific output will depend on the exact timing relationship of the incoming data to this cycle.

The best-case scenario is when the data has just been captured and then passed on to the output stage immediately; this can be as short as 48µs. In the worst-case scenario, this will be 860µs for EL5625, when the data has just missed the cycle at f_OSC = 21kHz.

When a large change in output voltage is required, the change will occur in 2V steps, thus the requisite number of timing cycles will be added to the overall update time. This means that a large change of 16V can take between 6.8ms and 7.2ms depending on the absolute timing relative to the update cycle.

Output Stage and the Use of External Oscillator

Simplified output sample and hold amp stage for one channel.

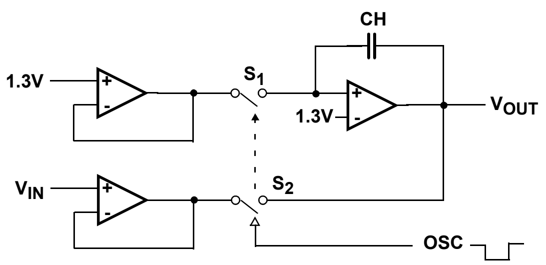


FIGURE 8.

The output voltage is generated from the DAC, which is V_{IN} in the above circuit. The refreshed switches are controlled by the internal or external oscillator signal. When the OSC clock signal is low, switches S_1 and S_2 are closed. The output $V_{OUT} = V_{IN}$ and at the same time the sample and hold cap CH is being charged. When the OSC clock signal is high, the refreshed switches S_1 and S_2 are opened and the output voltage is maintained by CH. This refreshed process will repeat every 18 clock cycles for each channel. The time takes to update the output depends on the timing at the V_{IN} and the state of the switches. It can take 1 to 19 clock cycles to update each output.

For the sample and hold capacitor CH to maintain the correct output voltage, the driving load shouldn't be changed at the rising edge of the OSC signal. Since at the rising edge of the OSC clock, the refreshed switches are being opened, if the load changes at that time, it will generate an error output voltage. For a fixed load condition, the internal oscillator can be used.

For the transient load condition, the external OSC mode should be used to avoid the conflict between the rising edge of the OSC signal and the changing load. So a timing delay circuit will be needed to delay the OSC signal and avoid the rising edge of the OSC signal and changing the load at the same time.

TRANSIENT LOAD RESPONSE

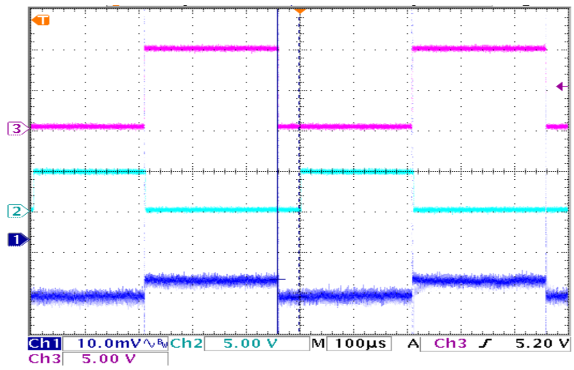


FIGURE 9.

Channel 3 --- sinking and sourcing 5mA current

Channel 2 --- EXT_OSC signal

Channel 1 --- V_{OUT}

Here, the OSC signal is synchronized to the load signal. The rising edge of the OSC signal is then delayed by some amount of time and gives enough time for CH to be charged to a new voltage before the switches are opened.

CHANNEL TO CHANNEL REFRESH

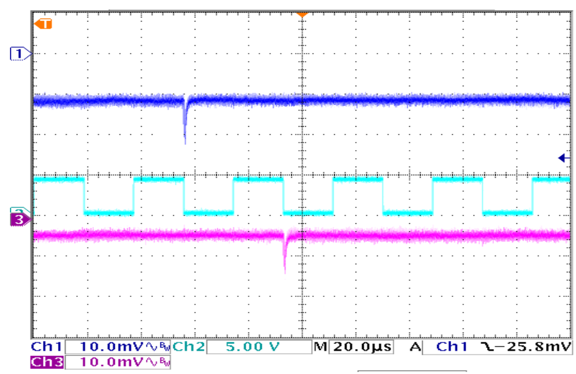


FIGURE 10.

Ch1 --- Output1

Ch3 --- Output2

Ch2 --- EXT_OSC

At the falling edge of the OSC, output 1 is being refreshed and one clock cycle later, output 2 is being refreshed. The spike you see here is the response of the output amplifier when the refreshed switches are closed. When driving a big capacitor load, there will be ringing at the spikes because the phase margin of the amplifier is decreased.

The speed of the external OSC signal shouldn't be greater than 70kHz because for the worst condition, it will take at least 4μs to charge the sample and hold capacitor CH. The pulse width has to be at least 4μs long. From our lab test, the duty cycle of the OSC signal must be greater than 30%.

POWER DISSIPATION

With the 100mA maximum continues output drive capability for V_{COM} channel, it is possible to exceed the 125°C absolute maximum junction temperature. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the part to remain in the safe operation.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by the IC is the total quiescent supply current times the total power supply voltage and plus the power in the IC due to the loads.

$$P_{DMAX} = V_S \times I_S + \Sigma[(V_S - V_{OUT}i) \times I_{LOAD}i]$$

when sourcing, and:

$$P_{DMAX} = V_S \times I_S + \Sigma(V_{OUT}i \times I_{LOAD}i)$$

when sinking.

Where:

- i = 18
- V_S = Supply voltage
- I_S = Quiescent current
- $V_{OUT}i$ = Output voltage of the i channel
- $I_{LOAD}i$ = Load current of the i channel

By setting the two P_{DMAX} equations equal to each other, we can solve for the R_{LOAD}s to avoid the device overheat. The package power dissipation curves provide a convenient way to see if the device will overheat.

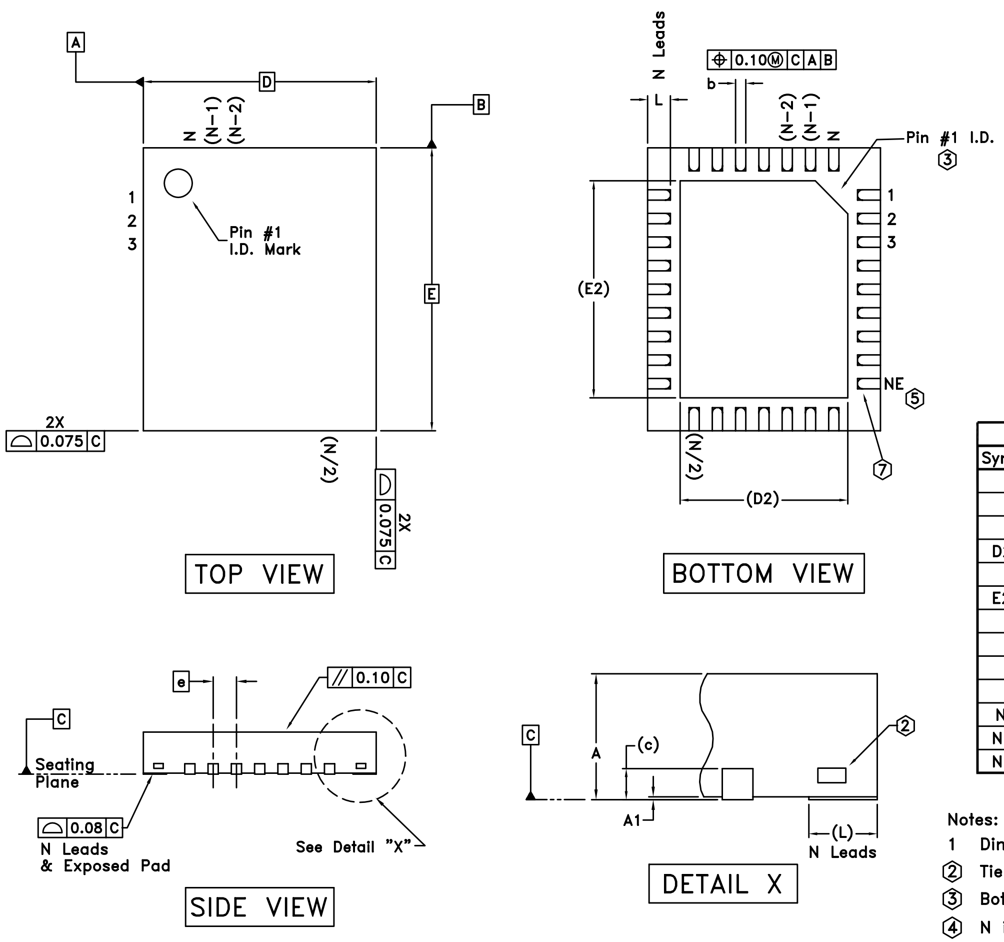
THERMAL SHUTDOWN

The EL5625 has an internal thermal shutdown circuitry that prevents overheating of the part. When the junction temperature goes up to about 150°C, the part will be disabled. When the junction temperature drops down to about 120°C, the part will be enabled. With this feature, any short circuit at the outputs will enable the thermal shutdown circuitry to disable the part.

POWER SUPPLY BYPASSING AND PRINTED CIRCUIT BOARD LAYOUT

Good printed circuit board layout is necessary for optimum performance. A low impedance and clean analog ground plane should be used for the EL5625. The traces from the two ground pins to the ground plane must be very short. The thermal pad of the EL5625 should be connected to the analog ground plane. Lead length should be as short as possible and all power supply pins must be well bypassed. A 0.1μF ceramic capacitor must be place very close to the V_S, V_{REFH}, V_{REFL}, and CAP pins. A 4.7μF local bypass tantalum capacitor should be placed to the V_S, V_{REFH}, and V_{REFL} pins.

QFN Package Outline Drawing



DIMENSION TABLE: 32 – 44 LEAD VARIATIONS					
Symbol	QFN44	QFN38	QFN32		Tolerance
A	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	+0.03/-0.02
D	7.00	5.00	8.00	5.00	Basic
D2 ⑧	5.10	3.80	5.80	3.60/2.48	Reference
E	7.00	7.00	8.00	6.00	Basic
E2 ⑧	5.10	5.80	5.80	4.60/3.40	Reference
L	0.55	0.40	0.53	0.50	±0.05
b	0.25	0.25	0.23	0.22	±0.02
c	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.80	0.50	Basic
N ④	44	38	32	32	Reference
ND ⑥	11	7	8	7	Reference
NE ⑤	11	12	8	9	Reference

DIMENSION TABLE: 16 – 28 LEAD VARIATIONS						
Symbol	QFN28	QFN24	QFN20		QFN16	Tolerance
A	0.90	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	0.02	+0.03/-0.02
D	4.00	4.00	5.00	4.00	4.00	Basic
D2 ⑧	2.65	2.80	3.70	2.70	2.40	Reference
E	5.00	5.00	5.00	4.00	4.00	Basic
E2 ⑧	3.65	3.80	3.70	2.70	2.40	Reference
L	0.40	0.40	0.40	0.40	0.60	±0.05
b	0.25	0.25	0.30	0.25	0.33	±0.02
c	0.20	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.65	0.50	0.65	Basic
N ④	28	24	20	20	16	Reference
ND ⑥	6	5	5	5	4	Reference
NE ⑤	8	7	5	5	4	Reference

Notes:

1 Dimensioning and tolerancing per ASME Y14.5M-1994.

② Tiebar view shown is a non-functional feature.

③ Bottom-side pin #1 I.D. is a diepad chamfer as shown.

④ N is the total number of terminals on the device.

⑤ NE is the number of terminals on the "E" side of the package (or Y-direction).

⑥ ND is the number of terminals on the "D" side of the package (or X-direction). ND = (N/2)-NE.

⑦ Inward end of terminal may be square or circular in shape with radius (b/2) as shown.

⑧ If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.

Drawing #: MDP0046	PACKAGE OUTLINE DRAWING QFN (QUAD FLAT NO-LEAD) PACKAGE FAMILY (Formerly Known as LPP)
Rev: 10	
Date: 12/1/04	
Units: mm	intersil SOLUTIONS IN SILICON
JEDEC Reg: MO-220	