ANALOG DEVICES

T-51-10-10

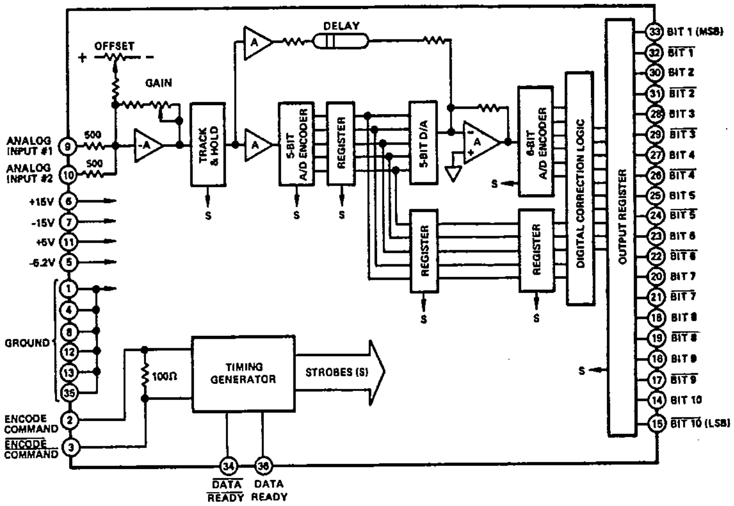
10-Bit Video Analog-to-Digital Converter

CAV-1040

FEATURES
10-Bit Resolution
40MHz Word Rate
Single 35-In² PC Board
ECL Compatible
No External Circuits Required

APPLICATIONS
Radar Digitizing
Medical Instrumentation
Digital Communications
Spectrum Analysis
Transient Analysis

CAV-1040 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The Analog Devices Model CAV-1040 A/D converter is a "system solution" which combines 10-bit resolution, 40MHz word rates, and small size to solve high-speed digitizing problems. Its design is based on proven concepts introduced in the MOD-1020 and MOD-1205 A/D Converters and takes advantage of recent advances in technology to achieve a new level of performance in high-resolution converters.

It is pin-for-pin compatible with the industry's first 10-bit, 20MHz A/D, the MOD-1020. But it *doubles* the word rate of its predecessor, making it possible for system designers to upgrade their systems without new layouts.

This remarkable converter is a complete answer to the question of digitizing radar, video, and/or other high-frequency inputs; it includes a track-and-hold, along with encoding and timing circuits. The CAV-1040 is an ideal choice for the designer who needs state-of-the-art performance in high-resolution, ultra-high-speed A/D conversion.

For applications requiring maximum analog bandwidth, the CAV-1040A is the choice. In this version, the input operational amplifier and its associated offset and gain controls have been eliminated; this effectively doubles the analog input bandwidth.

All inputs and outputs are ECL compatible. Analog input impedance is 250 ohms on 1V range; 500 ohms on 2V range. The A/D requires only an encode command and external power supplies for operation. The CAV-1040 is repairable and backed by Analog Devices' limited one-year warranty.

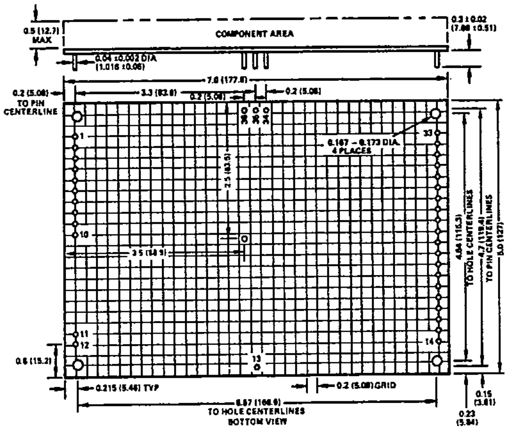
SPECIFICATIONS (typical at +25°C with nominal power supplies unless otherwise noted) T-51-10-10

Model	Units	CAV-1040	CAV-1040A
RESOLUTION (FS = Full Scale)	Bits	10	*
	%FS	0.1	*
LSB WEIGHT			
1V p-p FS	mV	1	N/A
2V p-p FS	mV	2	*
ACCURACY			
(Including Linearity) @ dc	%FS ± 1/2LSB	0.05	*
Monotonicity		Guaranteed	
Nonlinearity Vs. Temperature	ppm/°C	10	*
Offset vs. Temperature	ppm/°C (max)	200 (300)	*
Gain vs. Temperature	ppm/°C (max)	50 (100)	*
DYNAMIC CHARACTERISTICS			
In-Band Harmonics[1]			
500kHz input	dB below FS, min	65	*
2.3MHz input	dB below FS, min	55	*
9.3MHz input	dB below FS, min	48	*
Conversion Time[2]	ns	100 + 1 clock period	*
Conversion Rate	MHz, max	40	*
Aperture Uncertainty (Jitter)	ps, rms max	20	*
Effective Aperture Delay Time[3] (±2ns tolerance unit-to-unit)	ns	−2	8
Signal to Noise Ratio (SNR)[4]	dB, min	56	*
Noise Power Ratio (NPR)[5]	dB (min)	50 (47)	*
Transient Response[6]	ns	50	*
Overvoltage Recovery[7]	ns	50	*
Input Bandwidth			
Small Signal, 3dB[8]	MHz	30	60
Large Signal, 3dB[9]	MHz	20	40
Two-Tone Linearity (@ Input Frequencies)[10] (360kHz; 390kHz)	dB below FS, min	67	*
Differential Phase[11]	°	0.5	*
Differential Gain[11]	%	1	*
ANALOG INPUT			
Voltage Range			
Input Pins 9 & 10 Connected	V, p-p FS	1	N/A
Input Pin 9 or 10	V, p-p FS	2	N/A
	V, max	±4	*
Input Pin 9	V, p-p FS	N/A	2 ± 2%
Input Type		Either Unipolar or Bipolar	Bipolar only
Impedance			
1V Input Range	Ohms	250	N/A
2V Input Range	Ohms	500	*
Offset	mV	Adjustable to Zero with On-Card Potentiometer	±4 (Not adjustable)
vs. Temperature	ppm/°C (max)	200 (300)	*
ENCODE COMMAND INPUT[12]			
Logic Levels, ECL-Compatible	V	"0" = −1.7	*
(Balanced Input)	V	"1" = −0.9	*
Impedance (Line-to-Line)	Ohms, max	100	*
Rise and Fall Times	ns, max	5	*
Width			
Min	ns	10	*
Max		70% of Encode Command period	*
Frequency[13]	MHz	dc to 40	*
DIGITAL OUTPUT			
Format	Bits	10 Parallel; NRZ	*
Logic Levels, ECL-Compatible	V	"0" = −1.7	*
(Balanced Output)	V	"1" = −0.9	*
Drive (Line-to-Line)	Ohms, min	75	*
Time Skew	ns, max	5	*
Coding		Binary (BIN); 2's Complement (2SC)	Compl. Binary (CBIN) Compl. 2's Compl. (C2SC)
DATA READY OUTPUT			
Logic Levels, ECL-Compatible	V	"0" = −1.7	*
(Balanced Output)	V	"1" = −0.9	*
Drive (Line-to-Line)	Ohms, min	75	*
Rise and Fall Times	ns, max	5	*
Duration	ns (max)	10 (±2)	*
POWER REQUIREMENTS[14]			
+15V ±5%	mA, max	375	*
−15V ±5%	mA, max	200	*
+5V ±5%	mA, max	25	*
−5.2V ±5%	A, max	2.5	*
Power Consumption	W (max)	20 (22)	*
TEMPERATURE RANGE			
Operating	°C	0 to +70	*
Storage	°C	−55 to +85	*
Cooling Air Requirements	LFPM (Linear Feet Per Minute)	500	*
CONSTRUCTION			
Single Printed Circuit Card	Inches	7.0×5.0×0.5	*
MEAN TIME BETWEEN FAILURES[15]	Hours		3.22×10^4

For applications assistance, call Computer Labs Division at (919) 668-9511.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	19	$\overline{\text{BIT 8}}$
2	ENCODE COMMAND	20	BIT 7
3	$\overline{\text{ENCODE COMMAND}}$	21	$\overline{\text{BIT 7}}$
4	GROUND	22	$\overline{\text{BIT 6}}$
5	-5.2V	23	BIT 6
6	+15V	24	$\overline{\text{BIT 5}}$
7	-15V	25	BIT 5
8	GROUND	26	$\overline{\text{BIT 4}}$
9	ANALOG INPUT #1	27	BIT 4
10	ANALOG INPUT #2	28	BIT 3
11	+5V	29	$\overline{\text{BIT 3}}$
12	GROUND	30	BIT 2
13	GROUND	31	$\overline{\text{BIT 2}}$
14	BIT 10	32	$\overline{\text{BIT 1}}$
15	$\overline{\text{BIT 10}}$	33	BIT 1
16	BIT 9	34	$\overline{\text{DATA READY}}$
17	$\overline{\text{BIT 9}}$	35	GROUND
18	BIT 8	36	DATA READY

ALL GROUND PINS ARE CONNECTED TOGETHER WITHIN THE ADC.

NOTES

[1]In-Band Harmonics expressed in terms of spurious in-band signals and related harmonics generated at 40MHz encode rate.
[2]Measured from leading edge Encode Command to trailing edge Data Ready; use trailing edge to strobe output data into external circuits (see Text).
[3]See text for Effective Aperture Delay Time description.
[4]Rms signal to rms noise ratio with 500kHz analog input.
[5]Dc to 8.2MHz white noise bandwidth with slot frequency of 3.886MHz, and encode rate of 40MHz.
[6]For full-scale step input, 10-bit accuracy attained in specified time.
[7]Recovers to 10-bit accuracy in specified time after 2×FS input overvoltage.
[8]With analog input 40dB below FS.
[9]With FS analog input. (Large-signal bandwidth flat within 0.2dB, dc to 8MHz on CAV-1040; dc to 20MHz on CAV-1040A.)
[10]Each input frequency applied at level 7dB below full scale.
[11]Differential phase and differential gain measured with 20-IRE unit reference.
[12]Transition from digital "0" to digital "1" initiates encoding.
[13]For operation at word rates below 500kHz, consult factory.
[14]±15V must be equal and opposite within 200mV and track over temperature.
[15]Calculated using MIL HNBK-217; +25°C Ambient; Ground Fixed; 500 LFPM Air Flow.

*Specifications same as CAV-1040.
Specifications subject to change without notice.

THEORY OF OPERATION

Refer to the block diagram of the CAV-1040.

The OFFSET and GAIN controls shown on this diagram are exclusive to the model CAV-1040; they are not included in the model CAV-1040A. In the latter unit, the input operational amplifier is replaced by a buffer amplifier. As shown in the SPECIFICATIONS table, this difference in the front-end design causes the CAV-1040A to have only one input range (2V p-p); and materially increases the bandwidth of the converter.

Analog input signals to be digitized are applied through the input amplifier to a track-and-hold (T/H) amplifier which is normally operating as a buffer amplifier in the "track" mode, following all changes in analog input as they occur. The user of the CAV-1040 determines the point at which the analog signal is to be digitized by applying an Encode Command.

The leading edge of the encode command causes the track-and-hold to switch momentarily to the "hold" mode of operation, "freezing" the analog input signal long enough to begin the digitizing process.

In the CAV-1040, Effective Aperture Delay Time is defined as the interval between the leading edge of the encode command and that instant when the input signal is equal to the sampled value.

Basically, effective aperture delay time is a measure of the difference between the analog and digital delay (t_d-t_a) and can assume a zero, positive, or negative value depending on the comparative lengths of the two delays. In the CAV-1040, the analog delay (t_a) is greater than the switching delay (t_d), and causes the unit to hold an input voltage which occurred before the encode command because the track-and-hold sees a delayed version of the input signal.

Effective aperture delay time is different between the CAV-1040 and the CAV-1040A because the input amplifier of the CAV-1040 adds approximately 10 nanoseconds of analog delay to the signal path.

The "held" value of analog signal at the output of the T/H is applied to a 5-bit encoder. It is also applied through a buffer amplifier to an analog delay circuit, whose time delay is equal to the interval required for the first step of the digitizing/reconstruction process.

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After being digitized to 5-bit accuracy, the held value from the T/H is applied through registers to a 5-bit D/A converter which has 12-bit accuracy. Via a second set of registers, the same digital signal is directed to the digital correction logic circuits. The data stored in these latter registers will eventually represent Bits 1-5 of the 10-bit digital output of the CAV-1040.

The inverted, reconstructed output of the D/A converter becomes one input to an operational amplifier, whose other input is the delayed analog signal from the delay line. At the output of the wideband, fast-settling op amp, the resulting signal represents the residue which remains after a 5-bit digital representation of the analog input has been subtracted from that input.

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This residue, or error, signal is encoded by a second converter and is applied as 6-bit digital information to the digital correction logic circuits which contain Bits 1-5.

The correction circuits combine the 5-bit and 6-bit bytes of data to compensate for possible nonlinearities and other errors to assure the final 10-bit output of the CAV-1040 is 10-bit accurate.

Expressed in its simplest terms, the digital correction logic circuits use the information in the 6-bit signal to determine what modifications of Bits 1-5 may be necessary. The value of the MSB in the 6-bit byte establishes whether the 5-bit data are passed "as is" or whether they are increased by a value of binary "1". The remaining bits (2-6) of the 6-bit byte become Bits 6-10 of the CAV-1040 digital output.

Digitally corrected subranging (DCS), the innovative technique described here, helps compensate for a wide range of potential errors which could otherwise be avoided only if the CAV-1040 design included expensive, high precision components.

The use of 11 bits to obtain an accurate 10 bits of output cannot prevent gain error, track/hold droop error, linearity error, offset error, or any of the other inherent characteristics of "real world" A/D converters. But DCS can, and does, help nullify their effects and makes it economically feasible to accomplish high-speed, high-resolution digitizing of analog signals.

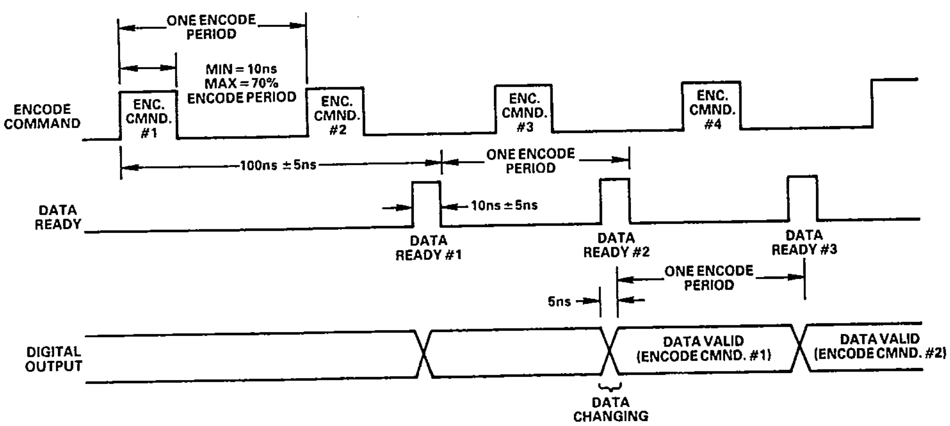


Figure 1. CAV-1040 Timing Diagram

CAV-1040 TIMING
Refer to Figure 1, the CAV-1040 Timing Diagram.

The intervals which are shown represent a continuous update rate of approximately 15.5MHz, which is considerably below the maximum capabilities of the CAV-1040. But that frequency helps to illustrate the "pipeline delay" characteristic of the converter.

At this word rate, spacing between encode commands is approximately 65 nanoseconds; and three encode commands have occurred before the data associated with the first command are valid. In Figure 1, this pipeline delay has a total time of approximately 155 nanoseconds (90ns + 65ns). This interval will be different at other word rates, but will always include 90ns; depending upon the update rate, either more or fewer encode commands may occur before the first data are available.

After the initial delay, valid data will be available at the word rate dictated by encode commands. Note that the spacing between Encode Command #1 and Encode Command #2 is equal to one encode period. This is the same spacing as between Data Ready #1 and Data Ready #2, and is also the spacing between the first and second groups of valid data.

System timing can be adjusted as necessary to take into account the pipeline delay effects and assure that the data of interest are strobed out of the converter at the appropriate time.

Figure 1 also illustrates why the trailing edge of the Data Ready pulse is recommended as the strobe for output data. Typically, data begin changing with the leading (rising) edge of each Data Ready pulse; they will be fully settled at the time of the trailing (falling) edge and available for use in external circuits.

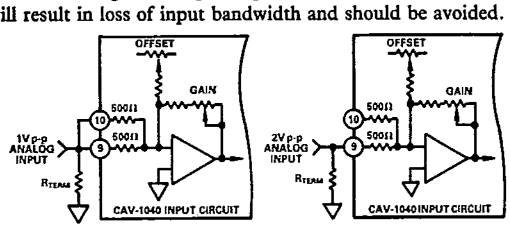
Another possibility for strobing the output data is to use the DATA READY pulse. Its trailing edge occurs at the same time as the trailing edge of the DATA READY signal, but is a rising edge, which may facilitate its use as a strobe.

ANALOG INPUT RANGE OPTIONS
Refer to Figure 2.

The input circuits which are shown apply only to the Model CAV-1040. The Model CAV-1040A does not include OFFSET and GAIN controls; nor is there a resistor connected to Pin 10 in that unit.

For a 1V range on the CAV-1040, connect the analog input to Pin 9, and connect Pins 9 and 10 together. The unterminated input impedance is 250 ohms. For a 2V range, connect the analog input to Pin 9, and leave Pin 10 disconnected. Unterminated impedance under these conditions is 500 ohms.

To obtain the desired input impedance for either a 1V range or a 2V range on the CAV-1040, connect the appropriate external terminating resistor between the analog input pin(s) and ground, as shown in Figure 2. Input impedances greater than 100 ohms will result in loss of input bandwidth and should be avoided.



Z_{IN}	R_{TERM}
50Ω	61.9Ω
75Ω	107Ω
93Ω	154Ω

1Vp-p INPUT OPTION

(R_{TERM} RESISTORS ARE 1%, 1/8W, MF)

Z_{IN}	R_{TERM}
50Ω	56.2Ω
75Ω	88.7Ω
93Ω	118Ω

2Vp-p INPUT OPTION

Figure 2. CAV-1040 Analog Input Range Options

The differences in the input circuit of the CAV-1040A preclude an ability to adjust gain and offset on that unit; in addition, there is no 1V input range available. The 2V input range of the CAV-1040A, however, can be terminated in the same way as the 2V range of the CAV-1040.

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OFFSET AND GAIN ADJUSTMENTS
The offset and gain of the CAV-1040A are set at the factory and are not adjustable by the user.

Refer to Figure 3, the CAV-1040 Adjustment Controls.

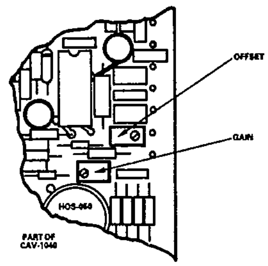

Figure 3. Offset and Gain Controls

When adjusting offset and gain of the CAV-1040 in the system, the OFFSET control should be adjusted first. It has sufficient range to allow the user to operate the CAV-1040 A/D in either the unipolar or bipolar mode. The adjustment sequence is:

1. Apply to the analog input a precise (±0.25mV) dc level corresponding to midscale of the desired input range.
2. Adust OFFSET control while observing MSB (Bit 1); adjust for MSB "toggling" between digital "0" and digital "1".
3. Apply a precise (±0.25mV) dc level corresponding to the most negative excursion of the desired input range.
4. Adjust GAIN control while observing LSB (Bit 10); adjust for output of Bits 1-9 solid "0" with LSB "toggling".
5. Apply a precise (±0.25mV) dc level corresponding to the most positive excursion of the desired input range.
6. Check digital output to assure Bits 1-9 are solid "1" with LSB "toggling".
7. Adjust OFFSET and GAIN controls alternately as necessary to obtain analog input range tolerance of ±1/2LSB.

ORDERING INFORMATION
For standard CAV-1040 units, order model number CAV-1040-400 or CAV-1040A-400. Standard units are set up at the factory to operate for optimum performance at word rates from 35-40MHz.

Converters intended to operate generally at word rates below 35MHz have different model numbers. Order by model number CAV-1040-XXX or CAV-1040A-XXX; in this designation, XXX is specified by the customer to indicate the desired optimized word rate. The decimal place is assumed (but not shown) between the second and third places. CAV-1040-300, for example, indicates final calibration and optimum performance at 30MHz. But the unit will operate over a range of word rates from 500kHz to 40MHz.

Optimum performance will be achieved within a band of frequencies approximately ±12% around the selected word rate. If later applications require word rates beyond the limits of the original optimum frequency, the unit can be returned to the factory for calibration; there is a nominal charge for this service.

Mating sockets for the CAV-1040 converters are model number MSB-2 (thru hole) or MSB-3 (closed end). These are individual solder-type pin sockets for mounting in PC boards; one is required for each of the 36 pins of the converter.