



Integrated Device Technology, Inc.

**8K x 8
16K x 8 CMOS
CMOS DUAL-PORT STATIC
RAM MODULE (MASTER)**

**IDT7M134S
IDT7M135S**

FEATURES:

- High-density 64K/128K CMOS Dual-Port RAM modules
- 16K x 8 (IDT7M135) or 8K x 8 (IDT7M134) option
- Fully asynchronous read/write operation from either port
- Fast access time
 - commercial: 30ns (max.)
 - military: 40ns (max.)
- Low power consumption
- On-chip port arbitration logic
- BUSY flags
- Single 5V (±10%) power supply
- Dual Vcc and GND pins for maximum noise immunity
- On-chip pull up resistors for open-drain BUSY flag option
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The IDT7M134/IDT7M135 are 64K/128K high-speed CMOS Dual-Port static RAM modules constructed on a multi-layered ceramic substrate using four IDT7132 2K x 8 dual-port static RAMs (IDT7M134) or eight IDT7132 dual-port static RAMs (IDT7M135) in leadless chip carriers. Dual-port function is achieved by utilization of the two on-board IDT54/IDT74FCT138 decoder circuits that interpret the higher order addresses AL11-13 and AR11-13 to select one of the eight 2K x 8 dual-port static RAMs. (On IDT7M134 8K x 8

option, AL13 and AR13 need to be externally grounded and the selection becomes one of the four 2K x 8 dual-port static RAMs). Extremely high speeds are achieved in this fashion due to the use of the IDT7132 dual-port static RAM, fabricated in IDT's high-performance CEMOS™ technology.

The IDT7M134/IDT7M135 provide two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in the memory. The BUSY flags are provided for the situation when both ports simultaneously access the same memory location. The on-chip arbitration logic will determine which port has access and sets the BUSY flag of the delayed port. BUSY is set at speeds that permit the processor to hold the operation and its respective address and data. The delayed port will have access when BUSY goes high (inactive).

The IDT7M134/IDT7M135 are available with access times as fast as 30ns commercial and 40ns military temperature range, with operating power consumption of only 2.1W/3.5W (max.). The module also offers a standby power mode of 1.4W/2.8W (max.) and a full standby mode of 660mW/1.3W (max.).

All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION (2)

GND	1	58	Vcc
CSL	2	57	CSR
R/WL	3	56	R/WR
R270	4	55	R270R
BUSYL	5	54	BUSYR
OEL	6	53	OER
A0L	7	52	A0R
A1L	8	51	A1R
A2L	9	50	A2R
A3L	10	49	A3R
A4L	11	48	A4R
A5L	12	47	A5R
A6L	13	46	A6R
A7L	14	45	A7R
A8L	15	44	A8R
A9L	16	43	A9R
A10L	17	42	A10R
A11L	18	41	A11R
A12L	19	40	A12R
A13L ⁽¹⁾	20	39	A13R ⁽¹⁾
I/O 0L	21	38	I/O0R
I/O 1L	22	37	I/O1R
I/O 2L	23	36	I/O2R
I/O 3L	24	35	I/O3R
I/O 4L	25	34	I/O4R
I/O 5L	26	33	I/O5R
I/O 6L	27	32	I/O6R
I/O 7L	28	31	I/O7R
GND	29	30	Vcc

DIP
TOP VIEW

2686 drw 01

PIN NAMES

Left Port	Right Port	Names
A0L-A13L	A0R-A13R	Address
I/O0L-I/O7L	I/O0R-I/O7R	Data Input/Output
CSL	CSR	Chip Select
R/WL	R/WR	Read/Write Enable
OEL	OER	Output Enable
BUSYL	BUSYR	BUSY Flag (Open Drain)
R270L	R270R	PULL-UP Resistors for Open-drain BUSY Flag option
Vcc	Vcc	Power
GND	GND	Ground

NOTES:

1. On 8K x 8 IDT7M134 option A13L and A13R need to be externally connected to ground for proper operation.
2. For module dimensions, please refer to module drawing M12 in the packaging section.

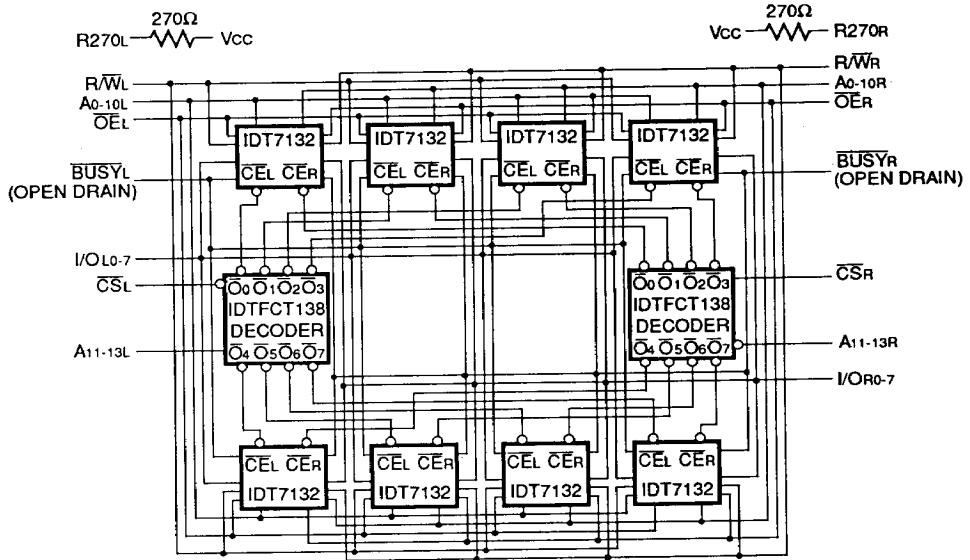
CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

SEPTEMBER 1990

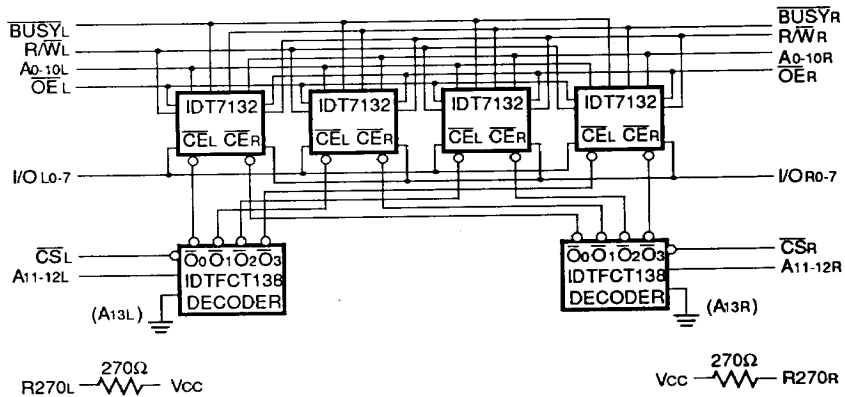
FUNCTIONAL BLOCK DIAGRAMS

IDT7M135 (16K x 8)



2686 drw 02

IDT7M134 (8K x 8)



2686 drw 03

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:

1. VIL = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS⁽⁴⁾

(Vcc = 5.0V ± 10%, TA = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7M134S			IDT7M135S			Unit
			Min.	Typ. ⁽¹⁾	Max.	Min.	Typ. ⁽¹⁾	Max.	
ILI	Input Leakage Current	Vcc = 5.5V, VIN = 0V to Vcc	—	—	15	—	—	20	µA
ILO	Output Leakage Current	$\overline{CS} = V_{IH}$, VOUT = 0V to Vcc	—	—	15	—	—	20	µA
VIH	Input High Voltage	—	2.2	—	6.0	2.2	—	6.0	V
VIL	Input Low Voltage	—	-1.0 ⁽²⁾	—	0.8	-1.0 ⁽²⁾	—	0.8	V
Icc	Dynamic Operating Current (Both Ports Active)	$\overline{CS} = V_{IL}$, Outputs Open, f = fMAX	—	190	380	—	320	640	mA
ISB	Standby Current (Both Ports Standby)	\overline{CSL} and $\overline{CSR} \geq V_{IH}$, Vcc = Max., Both Ports Output Open	—	130	260	—	260	520	mA
ISB1	Standby Current (One Port Standby)	\overline{CSL} or $\overline{CSR} \geq V_{IH}$, Vcc = Max. Active Port Outputs Open	—	160	320	—	290	580	mA
ISB2	Full Standby Current (Both Ports Full Standby)	Both Ports \overline{CSL} and $\overline{CER} \geq V_{cc} - 0.2V$ VIN ≥ Vcc - 0.2V or VIN ≤ 0.2V	—	4	120 ⁽³⁾	—	10	240 ⁽³⁾	mA
VOL	Output Low Voltage (I/Oo-I/O7)	IOL = 4mA, Vcc = 4.5V IOL = 8mA, Vcc = 4.5V	—	—	0.4	—	—	0.4	V
VOL	Open Drain Output Low Voltage (BUSY)	IOL = 16mA, Vcc = 4.5V	—	—	0.5	—	—	0.5	V
VOH	Output High Voltage	Ioh = -4mA, Vcc = 4.5V	2.4	—	—	2.4	—	—	V

NOTES:

- Vcc = 5V, TA = +25°C.
- VIL min. = -3.0V for pulse width less than 20ns.
- ISB2 max. of IDT7M134/IDT7M135 at commercial temperature = 80mA/150mA.
- For tAA = 30, 35, 40ns versions all D.C. parameters are preliminary only.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 and 3

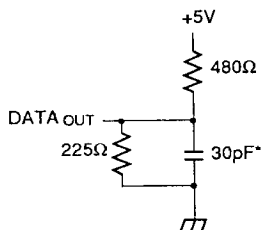


Figure 1. Output Load

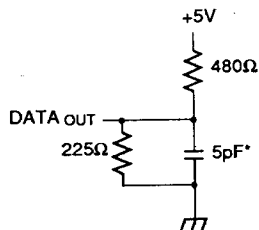


Figure 2. Output Load
(for tCHZ, tCLZ, tOHZ, tOLZ, tWHZ, tOW)

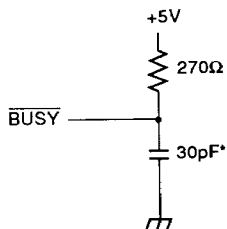


Figure 3. $\overline{\text{BUSY}}$ Output Load

* Including scope and jig. 30pF for fast speed versions. Consult factory for further details.

2686 drw 04

AC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ± 10%, TA = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	7M134S30 7M135S30 (Com'l. Only)		7M134S35 7M135S35 (Com'l. Only)		7M134S40 7M135S40		7M134S45 7M135S45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
tRC	Read Cycle Time	30	—	35	—	40	—	45	—	ns
tAA	Address Access Time	—	30	—	35	—	40	—	45	ns
tACS	Chip Select Access Time	—	30	—	35	—	40	—	45	ns
tOE	Output Enable Access Time	—	15	—	20	—	25	—	30	ns
tOH	Output Hold From Address Change	0	—	0	—	0	—	0	—	ns
tCLZ ⁽¹⁾	Chip Select to Output in Low Z	5	—	5	—	5	—	10	—	ns
tCHZ ⁽¹⁾	Chip Select to Output in High Z	—	10	—	15	—	15	—	20	ns
tOHZ ⁽¹⁾	Output Enable to Output in High Z	—	10	—	15	—	15	—	30	ns
tOLZ ⁽¹⁾	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	ns
tPU ⁽¹⁾	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
tPD ⁽¹⁾	Chip Deselect to Power Down Time	—	50	—	50	—	50	—	50	ns
WRITE CYCLE										
tWC	Write Cycle Time	30	—	35	—	40	—	45	—	ns
tCW	Chip Select to End of Write	25	—	30	—	35	—	40	—	ns
tAW	Address Valid to End of Write	25	—	30	—	35	—	40	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	5	—	ns
tDW	Data Valid to End of Write	20	—	20	—	22	—	25	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	5	—	ns
tOHZ ⁽¹⁾	Output Enable to Output in High Z	—	10	—	15	—	15	—	20	ns
tWHZ ⁽¹⁾	Write Enabled to Output in High Z	—	10	—	15	—	15	—	20	ns
tOW ⁽¹⁾	Output Active From End of Write	0	—	0	—	0	—	0	—	ns
BUSY TIMING										
tBAA	$\overline{\text{BUSY}}$ Access Time to Address	—	35	—	35	—	40	—	40	ns
tBDA	$\overline{\text{BUSY}}$ Disable Time to Address	—	30	—	35	—	35	—	35	ns
tBAC	$\overline{\text{BUSY}}$ Access Time to Chip Select	—	30	—	35	—	35	—	40	ns
tBDC	$\overline{\text{BUSY}}$ Disable Time to Chip Select	—	30	—	30	—	30	—	35	ns
tBDD	$\overline{\text{BUSY}}$ Disable to Valid Data	—	20	—	25	—	30	—	30	ns
tWDD	Write Pulse to Data Delay	—	50	—	55	—	60	—	65	ns
tDDD	Write Data Valid to Read Data	—	25	—	30	—	35	—	40	ns
tAPS	Arbitration Priority Set-up Time	10	—	10	—	10	—	10	—	ns

NOTE:

1. This parameter is guaranteed by design, but not tested.

AC ELECTRICAL CHARACTERISTICS (Continued)

(VCC = 5.0V ± 10%, TA = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	IDTM134S50 IDTM135S50		IDTM134S60 IDTM135S60		IDTM134S70 IDTM135S70 (Mil. Only)		IDTM134S90 IDTM135S90 (Mil. Only)		IDTM134S100 IDTM135S100 (Mil. Only)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
tRC	Read Cycle Time	50	—	60	—	70	—	90	—	100	—	ns
tAA	Address Access Time	—	50	—	60	—	70	—	90	—	100	ns
tACs	Chip Select Access Time	—	50	—	60	—	70	—	90	—	100	ns
tOE	Output Enable Access Time	—	35	—	40	—	40	—	45	—	50	ns
tOH	Output Hold From Address Change	0	—	0	—	5	—	10	—	10	—	ns
tCLZ ⁽¹⁾	Chip Select to Output in Low Z	10	—	10	—	10	—	15	—	15	—	ns
tCHZ ⁽¹⁾	Chip Select to Output in High Z	—	25	—	35	—	35	—	45	—	50	ns
tOHZ ⁽¹⁾	Output Enable to Output in High Z	—	40	—	40	—	30	—	40	—	40	ns
tOLZ ⁽¹⁾	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tPU ⁽¹⁾	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD ⁽¹⁾	Chip Deselect to Power Down Time	—	50	—	50	—	50	—	50	—	50	ns
WRITE CYCLE												
tWC	Write Cycle Time	50	—	60	—	70	—	90	—	100	—	ns
tCW	Chip Select to End of Write	45	—	50	—	60	—	80	—	95	—	ns
tAW	Address Valid to End of Write	45	—	50	—	60	—	80	—	95	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	40	—	45	—	45	—	50	—	55	—	ns
tWR	Write Recovery Time	5	—	5	—	5	—	5	—	5	—	ns
tDW	Data Valid to End of Write	25	—	25	—	30	—	40	—	40	—	ns
tDH	Data Hold Time	5	—	5	—	10	—	10	—	10	—	ns
tOHZ ⁽¹⁾	Output Enable to Output in High Z	—	25	—	35	—	35	—	40	—	40	ns
tWHZ ⁽¹⁾	Write Enabled to Output in High Z	—	25	—	35	—	35	—	40	—	40	ns
tOW ⁽¹⁾	Output Active From End of Write	0	—	0	—	0	—	0	—	0	—	ns
BUSY TIMING												
tBAA	BUS \bar{Y} Access Time to Address	—	40	—	45	—	45	—	45	—	50	ns
tBDA	BUS \bar{Y} Disable Time to Address	—	40	—	45	—	45	—	45	—	50	ns
tBAC	BUS \bar{Y} Access Time to Chip Select	—	40	—	40	—	40	—	40	—	50	ns
tBOC	BUS \bar{Y} Disable Time to Chip Select	—	35	—	35	—	35	—	35	—	50	ns
tBDD	BUS \bar{Y} Disable to Valid Data	—	35	—	40	—	50	—	50	—	60	ns
tWDD	Write Pulse to Data Delay	—	75	—	85	—	90	—	100	—	120	ns
tDDD	Write Data Valid to Read Data	—	50	—	60	—	70	—	80	—	100	ns
tAPS	Arbitration Priority Set-up Time	10	—	10	—	10	—	10	—	10	—	ns

NOTE:

1. This parameter is guaranteed by design, but not tested.

8

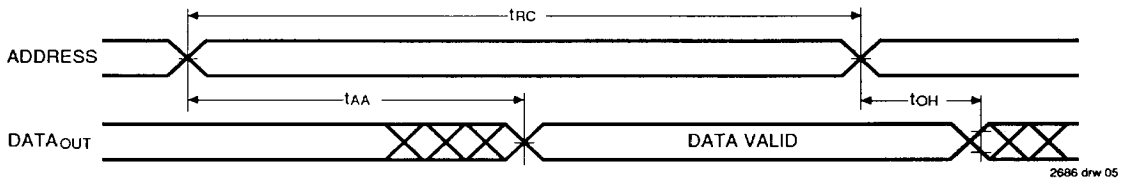
CAPACITANCE^(1,2) (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	IDT7M134S	IDT7M135S	Unit
CIN(D)	Input Capacitance (Data)	VIN = 0V	50	95	pF
CIN(A)	Input Capacitance (Address)	VIN = 0V	50	100	pF
CIN(C)	Input Capacitance (\overline{CS})	VIN = 0V	14	14	pF
CIN(C)	Input Capacitance (\overline{BUSY} , \overline{OE})	VIN = 0V	50	95	pF
CIN(C)	Input Capacitance (R/W)	VIN = 0V	50	95	pF
COU	Output Capacitance	VOU = 0V	50	95	pF

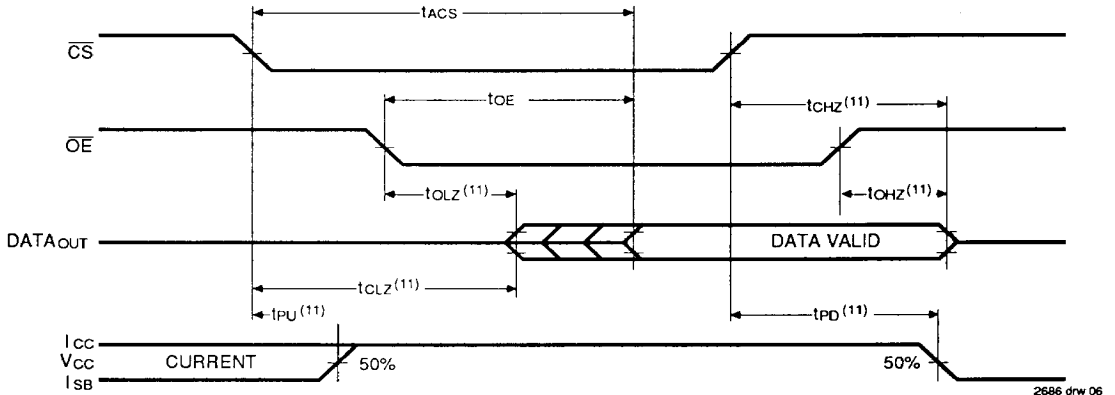
NOTES:

1. This parameter is guaranteed by design but not tested.
2. Typical values.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE^(1,2,6)



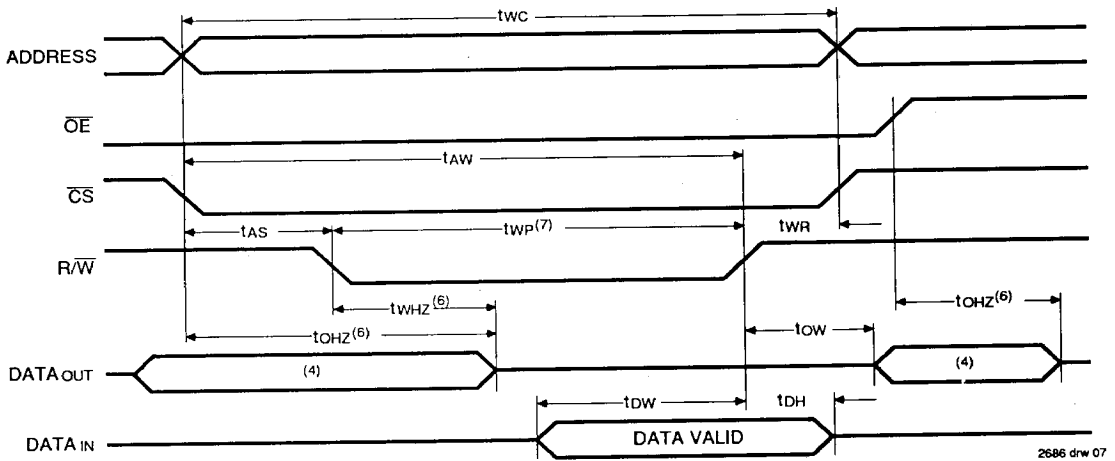
TIMING WAVEFORM OF READ CYCLE NO. 2 EITHER SIDE^(1,3)



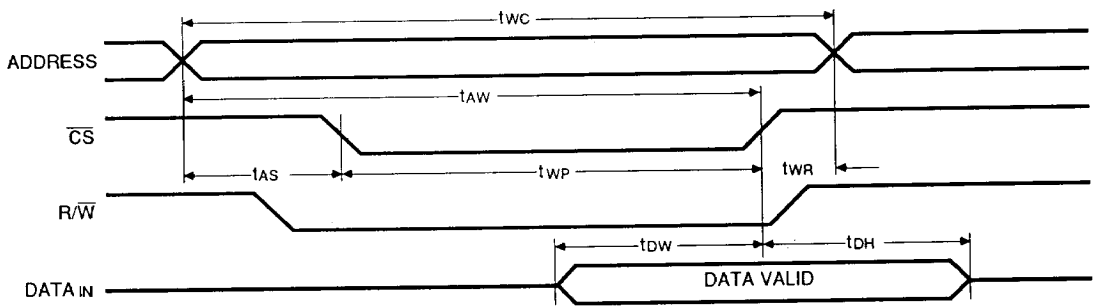
NOTES:

1. R/W is high for Read Cycles.
2. Device is continuously enabled, $\overline{CS} = V_{IL}$.
3. Addresses valid prior to or coincident with \overline{CS} transition low.
4. If \overline{CS} goes high simultaneously with R/W high, the outputs remain in the high impedance state.
5. $\overline{CS}_L = \overline{CS}_R \leq V_{IL}$.
6. $\overline{OE} = V_{IL}$.
7. R/W = V_{IH} during address transition.
8. Transition is measured at +500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
9. For SLAVE port (IDT7M144/IDT7M145) only.
10. Port-to-port delay through RAM cells from writing port to reading port.
11. This parameter guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/W CONTROLLED TIMING)^(1,2,3,7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (CS CONTROLLED TIMING)^(1,2,3,5)



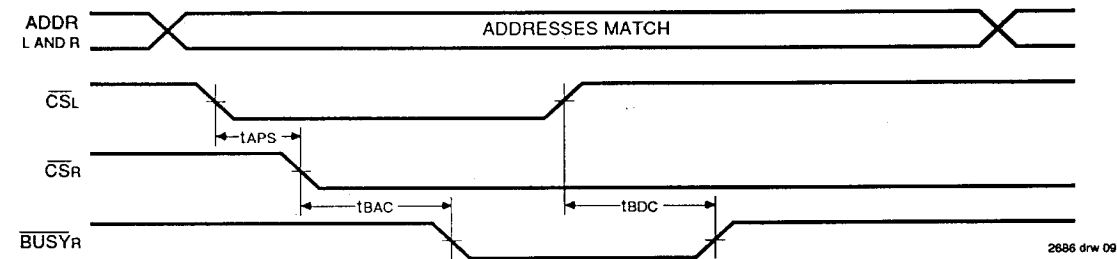
NOTES:

1. R/W or CS must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low CS and a low R/W.
3. t_{WR} is measured from the earlier of CS or R/W going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CS low transition occurs simultaneously with or after the R/W low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a R/W controlled write cycle, write pulse (t_{WP} > t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If OE is high during a R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

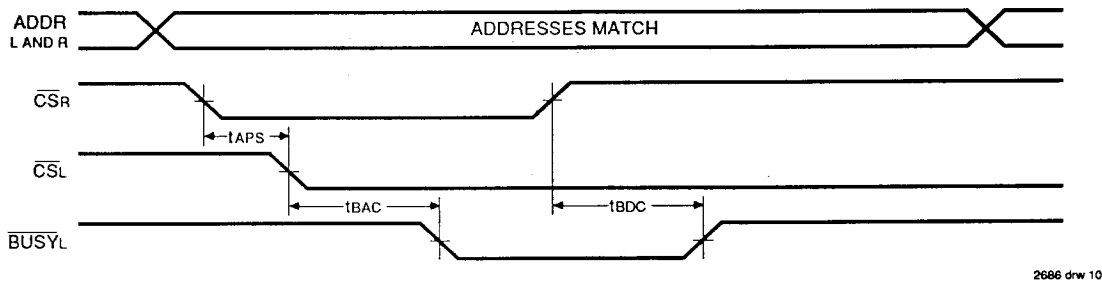
8

TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, \overline{CS} ARBITRATION

\overline{CSL} VALID FIRST:

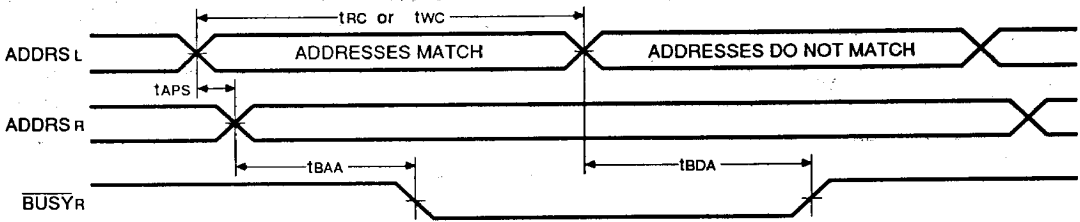


\overline{CSR} VALID FIRST:



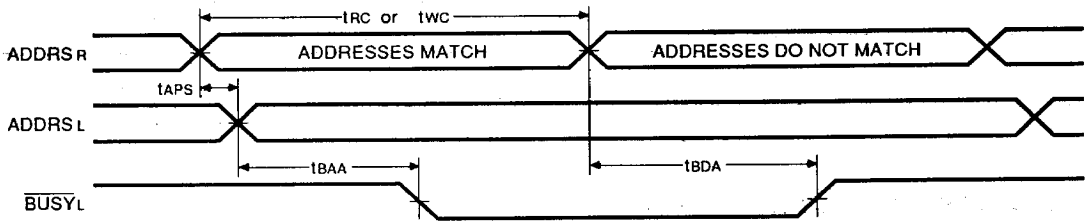
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION⁽⁵⁾

LEFT ADDRESS VALID FIRST:



2686 drw 11

RIGHT ADDRESS VALID FIRST:

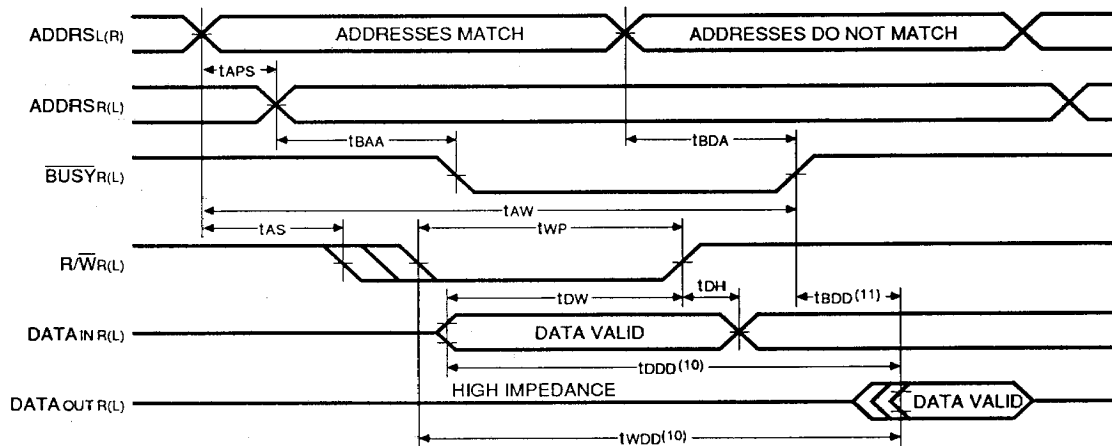


2686 drw 12

NOTES:

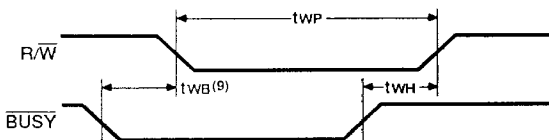
1. R/\bar{W} is high for Read Cycles.
2. Device is continuously enabled, $\bar{CS} = V_{IL}$.
3. Addresses valid prior to or coincident with \bar{CS} transition low.
4. If \bar{CS} goes high simultaneously with R/\bar{W} high, the outputs remain in the high impedance state.
5. $\bar{CS}_L = \bar{CS}_R \leq V_{IL}$
6. $\bar{OE} = V_{IL}$
7. $R/\bar{W} = V_{IH}$ during address transition.
8. Transition is measured at +500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
9. For SLAVE port (IDT7M144/IDT7M145) only.
10. Port-to-port delay through RAM cells from writing port to reading port.
11. This parameter guaranteed by design, but not tested.

TIMING WAVEFORM OF READ WITH BUSY⁽⁵⁾



2686 drw 13

TIMING WAVEFORM OF WRITE WITH BUSY⁽⁵⁾



2686 drw 14

NOTES:

1. R/W is high for Read Cycles.
2. Device is continuously enabled, CS = VIL.
3. Addresses valid prior to or coincident with CS transition low.
4. If CS goes high simultaneously with R/W high, the outputs remain in the high impedance state.
5. CSL = CSR ≤ VIL.
6. OE = VIL.
7. R/W = VIH during address transition.
8. Transition is measured at +500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
9. For SLAVE port (IDT7M144/IDT7M145) only.
10. Port-to-port delay through RAM cells from writing port to reading port.
11. This parameter guaranteed by design, but not tested.

FUNCTIONAL DESCRIPTION

The IDT7M134/IDT7M135 provide two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7M134/IDT7M135 have an automatic power down feature controlled by CS. The CS controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected (CS high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control (\overline{OE}). In the read mode, the port's \overline{OE} turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION

The arbitration logic will resolve an address match or a chip select match down to 10ns minimum and determine which port has access. In all cases, an active BUSY flag will be set for the delayed port.

The BUSY flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and set the delayed port's \overline{BUSY} flag. \overline{BUSY} is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has \overline{BUSY} set LOW. The delayed port will have access when \overline{BUSY} goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before CS, on-chip control logic arbitrates between \overline{CSL} and \overline{CSR} for access; or (2) if the CSs are low before

an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table III, Address Arbitration). In either mode of arbitration, the delayed port's \overline{BUSY} flag is set and will reset when the port granted access complete its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION

Expanding the data bus width to sixteen-or-more-bits in a dual-port static RAM system implies that several modules will be active at the same time. If each module includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its \overline{BUSYL} while another activates its \overline{BUSYR} signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "busy lock-out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has \overline{BUSY} inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port static RAMs in width, the writing of the SLAVE modules must be delayed until after the \overline{BUSY} input has settled. Otherwise, the SLAVE module may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past \overline{BUSY} to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems when more than one module is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to \overline{BUSY} from the MASTER.

TRUTH TABLES

TABLE I — NON-CONTENTION
READ/WRITE CONTROL,
LEFT OR RIGHT PORT⁽¹⁾

R/W	CS	OE	I/O ₀₋₇	FUNCTION
X	H	X	Z	Port Disabled and in Power Down Mode, \overline{ISB}
X	H	X	Z	$\overline{CSR} = \overline{CSL} = H$, Power Down Mode, \overline{ISB} or $\overline{ISB2}$
L	L	X	DATAIN	Data on Port Written into Memory ⁽²⁾
H	L	L	DATAOUT	Data in Memory Output on Port ⁽³⁾
H	L	H	Z	High Impedance Outputs

NOTES:

1. A_{0L}-A_{13L}≠A_{0R}-A_{13R}
2. If $\overline{BUSY} = L$, data is not written.
3. If $\overline{BUSY} = L$, data may not be valid, see t_{WDD} and t_{OOD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

TABLE III — ARBITRATION

LEFT PORT		RIGHT PORT		FLAGS ⁽¹⁾		FUNCTION
CSL	A0L-A13L	CSR	A0R-A13R	BUSYL	BUSYR	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	≠A0R-A13R	L	≠A0L-A13L	H	H	No Contention
ADDRESS ARBITRATION WITH CS LOW BEFORE ADDRESS MATCH						
L	LV10R	L	LV10R	H	L	Left-Port Wins
L	RV10L	L	LV10L	L	H	Right-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
CS ARBITRATION WITH ADDRESS MATCH BEFORE CS						
LL10R	= A0R-A13R	LL10R	= A0L-A13L	H	L	Left-Port Wins
RL10L	= A0R-A13R	RL10R	= A0L-A13L	L	H	Right-Port Wins
LW10R	= A0R-A13R	LW10R	= A0L-A13L	H	L	Arbitration Resolved
LW10R	= A0R-A13R	LW10R	= A0L-A13L	L	H	Arbitration Resolved

NOTE:

- X = DON'T CARE, L = LOW, H = HIGH, Same = Left and Right Addresses match within 10ns of each other.
 LV10R = Left Address Valid ≥ 10ns before Right Address.
 RV10L = Right Address Valid ≥ 10ns before Left Address.
 LL10R = Left CS = LOW ≥ 10ns before Right CS.
 RL10L = Right CS = LOW ≥ 10ns before left CS.
 LW10R = Left and Right CS = LOW within 10ns of each other.

ORDERING INFORMATION

