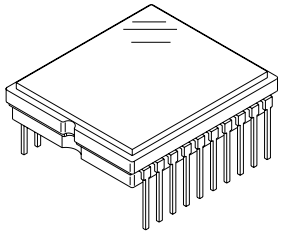
SONY

ICX267AL

Diagonal 8mm (Type 1/2) Progressive Scan CCD Image Sensor with Square Pixel for B/W Cameras

20 pin DIP (Plastic)



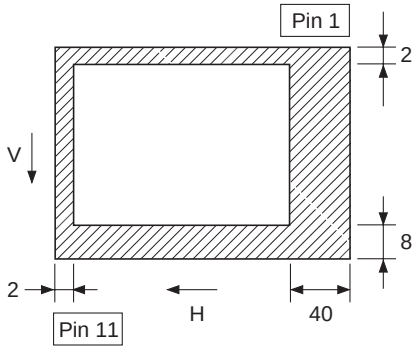
Description

The ICX267AL is a diagonal 8mm (Type 1/2) interline CCD solid-state image sensor with a square pixel array and 1.45M effective pixels. Progressive scan allows all pixels' signals to be output independently. Also, the adoption of high frame rate readout mode supports 30 frames per second. This chip features an electronic shutter with variable charge-storage time which makes it possible to realize full-frame still image without a mechanical shutter. High resolution and high low dark current are achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.

This chip is suitable for applications such as electronic still cameras, PC input cameras, etc.

Features

- Progressive scan allows individual readout of the image signals from all pixels.
- High horizontal and vertical resolution (both approx. 1024TV-lines) still image without a mechanical shutter.
- Supports high frame rate readout mode (effective 512 lines output, 30 frames/s)
- Square pixel
- Horizontal drive frequency: 28.636MHz
- No voltage adjustments (reset gate and substrate bias are not adjusted.)
- High resolution, high color reproductivity, high sensitivity, low dark current
- Low smear, excellent antiblooming characteristics
- Continuous variable-speed shutter



Optical black position (Top view)

Device Structure

- Interline CCD image sensor
- Image size: Diagonal 8mm (Type 1/2)
- Total number of pixels: 1434 (H) × 1050 (V) approx. 1.50M pixels
- Number of effective pixels: 1392 (H) × 1040 (V) approx. 1.45M pixels
- Number of active pixels: 1360 (H) × 1024 (V) approx. 1.40M pixels (7.959mm diagonal)
- Chip size: 7.60mm (H) × 6.20mm (V)
- Unit cell size: 4.65µm (H) × 4.65µm (V)
- Optical black: Horizontal (H) direction: Front 2 pixels, rear 40 pixels
  Vertical (V) direction: Front 8 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 20
  Vertical 3
- Substrate material: Silicon

Wfine CCD®

* Wfine CCD is a registered trademark of Sony Corporation.
Represents a CCD adopting progressive scan, primary color filter and square pixel.

E01Y03B43

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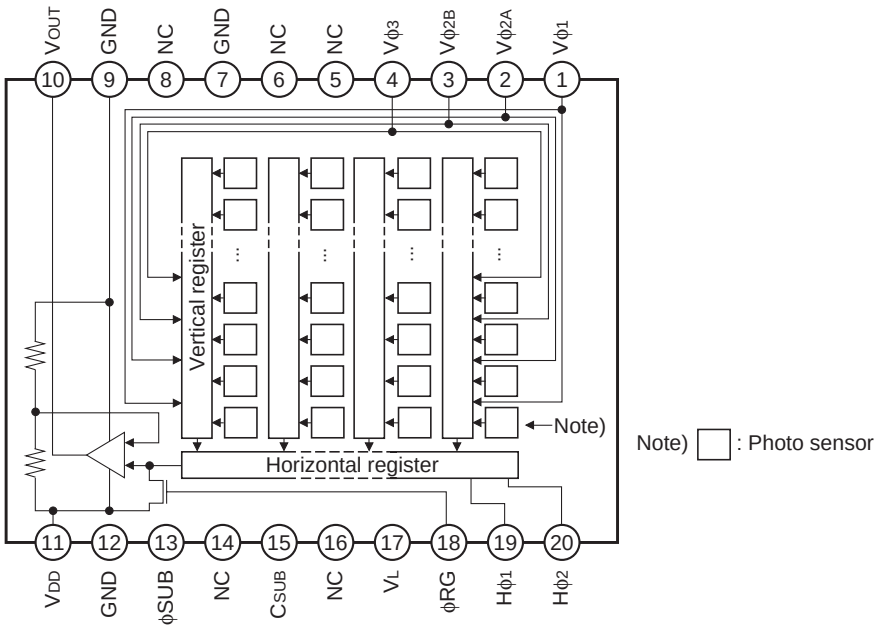
Block Diagram and Pin Configuration

(Top View)



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vφ1	Vertical register transfer clock	11	VDD	Supply voltage
2	Vφ2A	Vertical register transfer clock	12	GND	GND
3	Vφ2B	Vertical register transfer clock	13	φSUB	Substrate clock
4	Vφ3	Vertical register transfer clock	14	NC	
5	NC		15	CSUB	Substrate bias*1
6	NC		16	NC	
7	GND	GND	17	VL	Protective transistor bias
8	NC		18	φRG	Reset gate clock
9	GND	GND	19	Hφ1	Horizontal register transfer clock
10	VOUT	Signal output	20	Hφ2	Horizontal register transfer clock

*1 DC bias is generated within the CCD, so that this pin should be grounded externally through a capacitance of 0.1µF.

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Against φSUB	V_{DD}, V_{OUT}, φRG – φSUB	–40 to +10	V	
	$V\phi_{2A}$, $V\phi_{2B}$ – φSUB	–50 to +15	V	
	$V\phi_1$, $V\phi_3$, V_L – φSUB	–50 to +0.3	V	
	$H\phi_1$, $H\phi_2$, GND – φSUB	–40 to +0.3	V	
	C_{SUB} – φSUB	–25 to	V	
Against GND	V_{DD}, V_{OUT}, φRG, C_{SUB} – GND	–0.3 to +18	V	
	$V\phi_1$, $V\phi_{2A}$, $V\phi_{2B}$, $V\phi_3$ – GND	–10 to +18	V	
	$H\phi_1$, $H\phi_2$ – GND	–10 to +15	V	
Against V_L	$V\phi_{2A}$, $V\phi_{2B}$ – V_L	–0.3 to +28	V	
	$V\phi_1$, $V\phi_3$, $H\phi_1$, $H\phi_2$, GND – V_L	–0.3 to +15	V	
Between input clock pins	Voltage difference between vertical clock input pins	to +15	V	*1
	$H\phi_1$ – $H\phi_2$	–16 to +16	V	
	$H\phi_1$, $H\phi_2$ – $V\phi_3$	–16 to +16	V	
Storage temperature		–30 to +80	°C	
Operating temperature		–10 to +60	°C	

*1 +24V (Max.) when clock width < 10µs, clock duty factor < 0.1%.
+16V (Max.) is guaranteed for turning on or off power supply.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Power Supply voltage	V_{DD}	14.55	15.0	15.45	V	
Protective transistor bias	V_L	*1				
Substrate clock	φSUB	*2				
Reset gate clock	φRG	*2				

*1 V_L setting is the V_{VL} voltage of the vertical transfer clock waveform, or the same power supply as the V_L power supply for the V driver should be used.

*2 Do not apply a DC bias to the substrate clock and reset gate clock pins, because a DC bias is generated within the CCD.

DC Characteristics

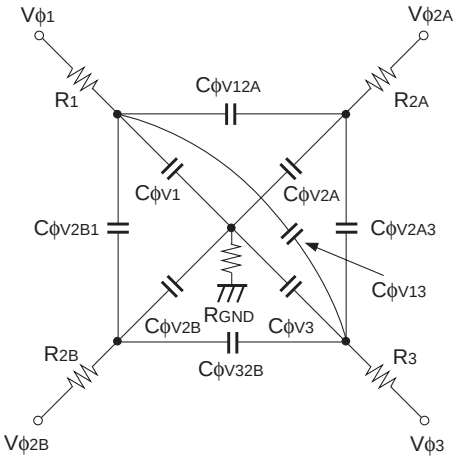
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Power supply current	I_{DD}		7.7		mA	

Clock Voltage Conditions

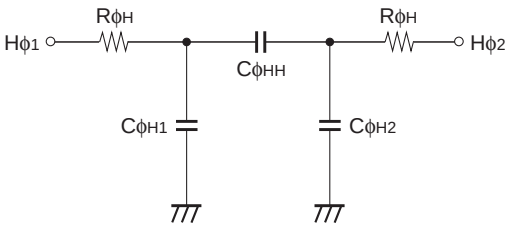
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH02A}	–0.05	0	0.05	V	2	$V_{VH} = V_{VH02A}$
	V_{VH1}, V_{VH2A}, V_{VH2B}, V_{VH3}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2A}, V_{VL2B}, V_{VL3}	–8.4	–8.0	–7.6	V	2	$V_{VL} = (V_{VL1} + V_{VL3})/2$
	$V\phi_1$, $V\phi_{2A}$, $V\phi_{2B}$, $V\phi_3$	7.6	8.0	8.4	V	2	
	$\lvert V_{VL1} - V_{VL3} \rvert$			0.1	V	2	
	V_{VHH}			0.9	V	2	High-level coupling
	V_{VHL}			1.3	V	2	High-level coupling
	V_{VLH}			1.0	V	2	Low-level coupling
	V_{VLL}			0.9	V	2	Low-level coupling
Horizontal transfer clock voltage	$V\phi_H$	4.75	5.0	5.25	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
Reset gate clock voltage	$V\phi_{RG}$	3.0	3.3	5.5	V	4	
	$V_{RGLH} - V_{RGLL}$			0.4	V	4	Low-level coupling
	$V_{RGL} - V_{RGLm}$			0.5	V	4	Low-level coupling
Substrate clock voltage	$V\phi_{SUB}$	22.15	23.0	23.85	V	5	

Clock Equivalent Circuit Constant

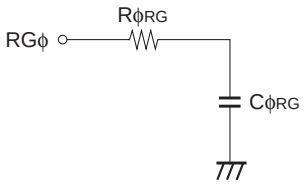
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$		2200		pF	
	$C_{\phi V2A}$		3300		pF	
	$C_{\phi V2B}$		3300		pF	
	$C_{\phi V3}$		3300		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12A}$, $C_{\phi V2B1}$		1200		pF	
	$C_{\phi V2A3}$, $C_{\phi V32B}$		1200		pF	
	$C_{\phi V13}$		2200		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		47		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		100		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		8		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		680		pF	
Vertical transfer clock series resistor	R_1		36		Ω	
	R_{2A}, R_3		56		Ω	
	R_{2B}		56		Ω	
Vertical transfer clock ground resistor	R_{GND}		30		Ω	
Horizontal transfer clock series resistor	$R_{\phi H}$		15		Ω	
Reset gate clock series resistor	$R_{\phi RG}$		20		Ω	



Vertical transfer clock equivalent circuit



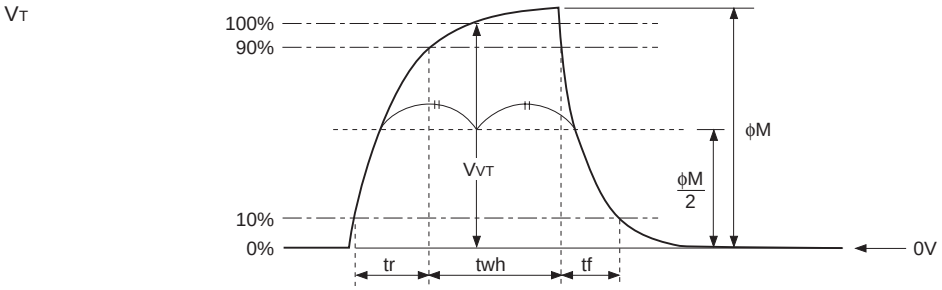
Horizontal transfer clock equivalent circuit



Reset gate clock equivalent circuit

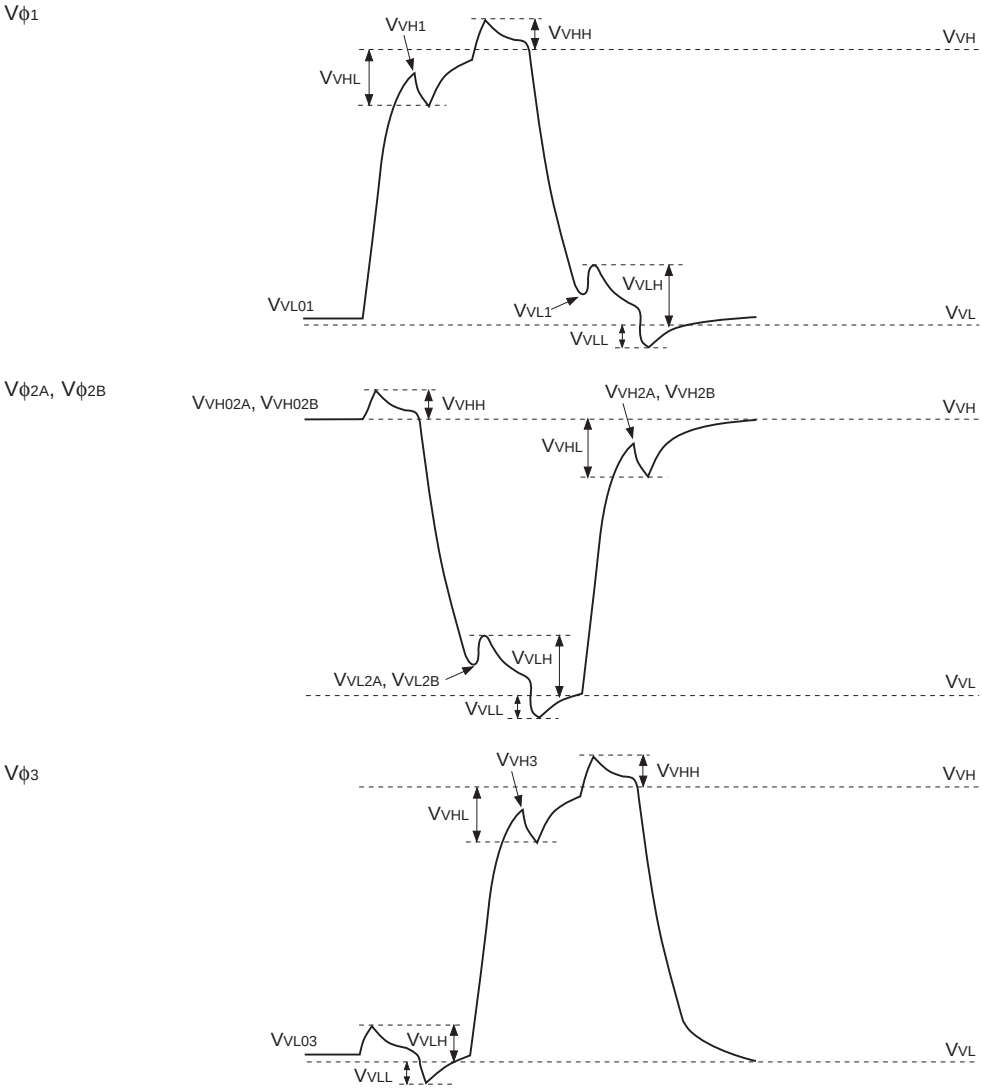
Drive Clock Waveform Conditions

(1) Readout clock waveform



Note) Readout clock is used by composing vertical transfer clocks Vϕ2A and Vϕ2B.

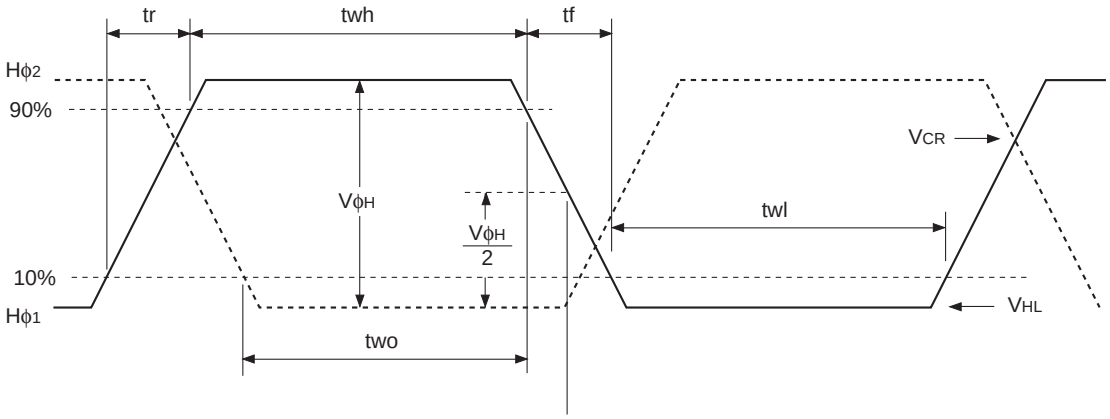
(2) Vertical transfer clock waveform



$V_{VH} = V_{VH02A}$
$V_{VL} = (V_{VL01} + V_{VL03})/2$
$V_{VL3} = V_{VL03}$

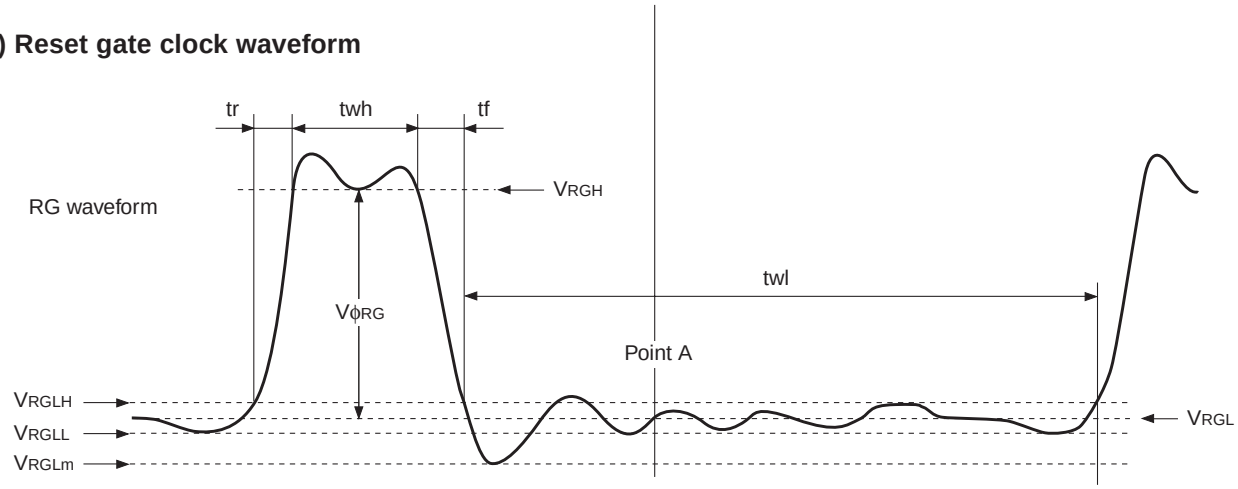
$V_{\phi V1} = V_{VH1} - V_{VL01}$
$V_{\phi V2A} = V_{VH02A} - V_{VL2A}$
$V_{\phi V2B} = V_{VH02B} - V_{VL2B}$
$V_{\phi V3} = V_{VH3} - V_{VL03}$

(3) Horizontal transfer clock waveform



Cross-point voltage for the Hϕ1 rising side of the horizontal transfer clocks Hϕ1 and Hϕ2 waveforms is VCR.
The overlap period for twh and twl of horizontal transfer clocks Hϕ1 and Hϕ2 is two.

(4) Reset gate clock waveform



VRGLH is the maximum value and VRGLL is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.
In addition, VRGL is the average value of VRGLH and VRGLL.

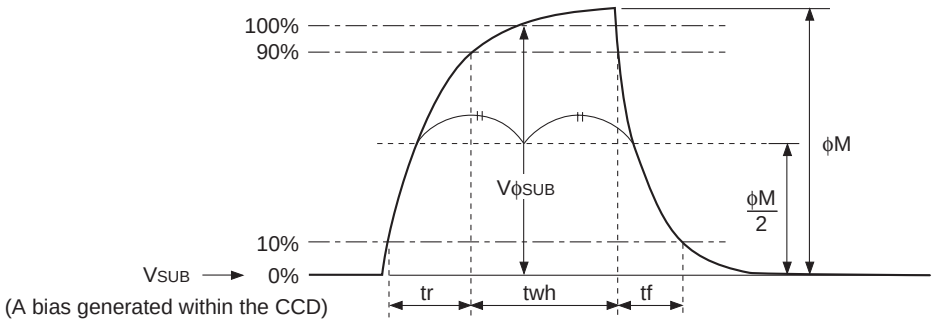
$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming VRGH is the minimum value during the interval twh, then:

$$V_{\phi RG} = V_{RGH} - V_{RGL}.$$

Negative overshoot level during the falling edge of RG is VRGLm.

(5) Substrate clock waveform



Clock Switching Characteristics

Item		Symbol	twh			twl			tr			tf			Unit	Remarks
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock		V_T	3.2	3.4						0.5			0.5		µs	During readout
Vertical transfer clock		$V\phi_1$, $V\phi_{2A}$, $V\phi_{2B}$, $V\phi_3$										15		450	ns	*1
Horizontal transfer clock	During imaging	$H\phi_1$	10	12.5		10	12.5			5	7.5		5	7.5	ns	*2
		$H\phi_2$	10	12.5		10	12.5			5	7.5		5	7.5		
	During parallel-serial conversion	$H\phi_1$								0.01			0.01		µs	
		$H\phi_2$								0.01			0.01			
Reset gate clock		ϕRG	4	8			24			2		2			ns	
Substrate clock		ϕSUB		3.9							0.5			0.5	µs	When draining charge

*1 When vertical transfer clock driver CXD1267AN × 2 is used.

*2 tf ≥ tr – 2ns, and the cross-point voltage (V_{CR}) for the $H\phi_1$ rising side of the $H\phi_1$ and $H\phi_2$ waveforms must be at least $V\phi_H/2$ [V].

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	$H\phi_1$, $H\phi_2$	8	10		ns	

Spectral Sensitivity Characteristics (excludes lens characteristics and light source characteristics)

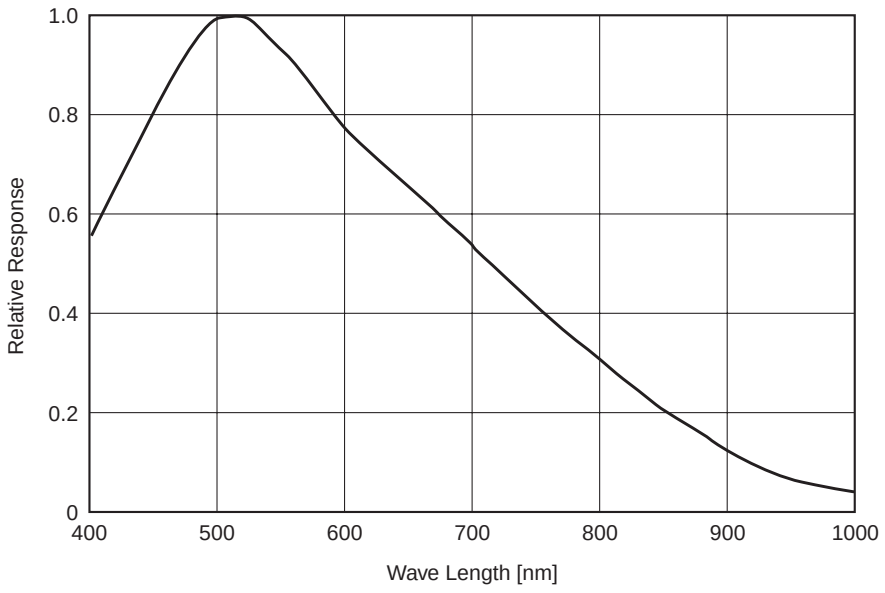


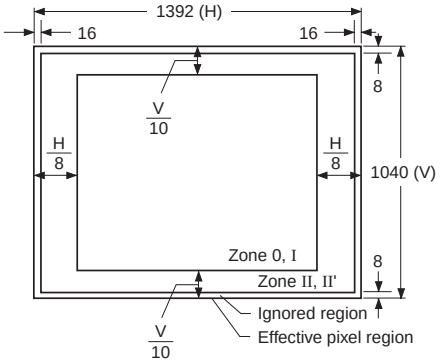
Image Sensor Characteristics (Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks	
Sensitivity	S	360	450		mV	1	1/30s accumulation	
Saturation signal	Vsat	450			mV	2	Ta = 60°C	Progressive scan readout mode
	Vsat2	380			mV	2		High frame rate readout mode
	Vsat4	380			mV	2		High frame rate readout two pixels addition*1
Smear	Sm		0.001	0.0025	%	3	Progressive scan readout, high frame rate readout two pixels addition	
			0.002	0.005	%	3	High frame rate readout mode	
Video signal shading	SHg			20	%	4	Zone 0 and I	
				25	%	4	Zone 0 to I'	
Dark signal	Vdt			8	mV	5	Ta = 60°C, 15 frames/s	
Dark signal shading	ΔVdt			2	mV	6	Ta = 60°C, 15 frames/s*2	
Lag	Lag			0.5	%	7		

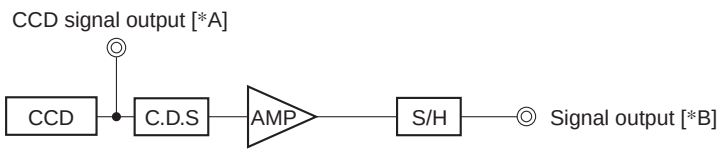
*1 Vsat4 is the saturation signal amount at two pixels addition, and it is 190mV per one pixel. VSUB internal generation value ensures 190mV per one pixel of the saturation signal amount in high frame rate two pixels addition mode.

*2 Eliminates the dark signal shading in the vertical direction by the high-speed transfer of the vertical register.

Zone Definition of Video Signal Shading



Measurement System

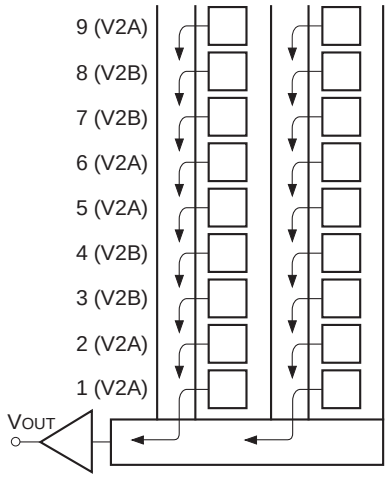
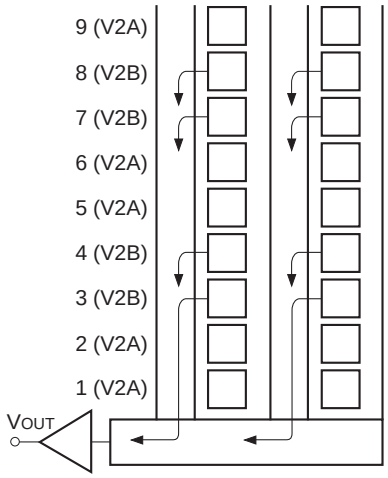
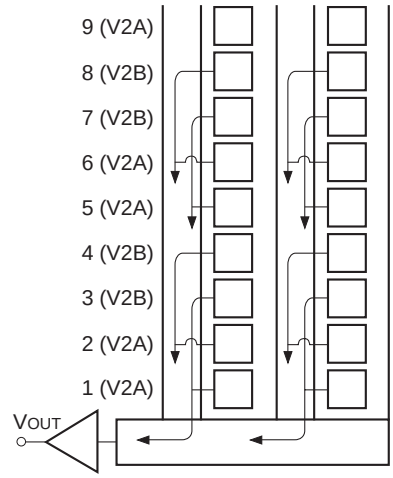


Note) Adjust the amplifier gain so that the gain between [*A] and [*B] equals 1.

Image Sensor Characteristics Measurement Method

◎ **Readout modes**

The diagram below shows the output methods for the following three readout modes.

Progressive scan mode	High frame rate readout mode	High frame rate readout two pixels addition mode
		

1. Progressive scan mode
   In this mode, all pixels signals are output in non-interlace format in 1/15s.
   The vertical resolution is approximately 800 TV-lines and all pixels signals within the same exposure period are read out simultaneously, making this mode suitable for high resolution image capturing.

2. High frame rate readout mode
   All effective areas are scanned in approximately 1/30s by reading out two out of four lines (3rd and 4th lines, 7th and 8th lines). The vertical resolution is approximately 400 TV-lines.
   This readout mode emphasizes processing speed over vertical resolution.

3. High frame rate readout two pixels addition mode
   All effective areas are scanned in approximately 1/30s by reading out two out of four lines (3rd and 4th lines, 7th and 8th lines), and by reading out two out of the remaining four lines (1st and 2nd lines, 5th and 6th lines) after shifting the vertical register by 2 bits, and adding them in the vertical register.

◎ **Measurement conditions**

1) In the following measurements, the device drive conditions are at the typical values of the progressive scan mode, bias and clock voltage conditions.

2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, and the value measured at point [*B] in the measurement system is used.

◎ **Definition of standard imaging conditions**

1) Standard imaging condition Ⅰ
Use a pattern box (luminance: 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

2) Standard imaging condition **Ⅰ**:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity
Set to standard imaging condition Ⅰ After selecting the electronic shutter mode with a shutter speed of 1/250s, measure the signal output (V_S) at the center of the screen, and substitute the values into the following formulas.

$$S = Vs \times \frac{250}{30} \text{ [mV]}$$

2. Saturation signal
Set to standard imaging condition **Ⅰ**. After adjusting the luminous intensity to 10 times the intensity with the average value of the signal output, 150mV, measure the minimum value of the signal output.

3. Smear
Set to standard imaging condition **Ⅰ**. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity to 500 times the intensity with the average value of the signal output, 150mV. When the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (Vsm [mV]) of the signal output and substitute the value into the following formula.

$$Sm = 20 \times \log\left(\frac{VSm}{150} \times \frac{1}{500} \times \frac{1}{10}\right) \text{ [dB] (1/10V method conversion value)}$$

4. Video signal shading
Set to standard imaging condition **Ⅰ**. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the signal output is 150mV. Then measure the maximum (Vrmax [mV]) and minimum (Vrmin [mV]) values of the signal output and substitute the values into the following formula.

$$SH = (Vrmax - Vrmin)/150 \times 100 \text{ [\%]}$$

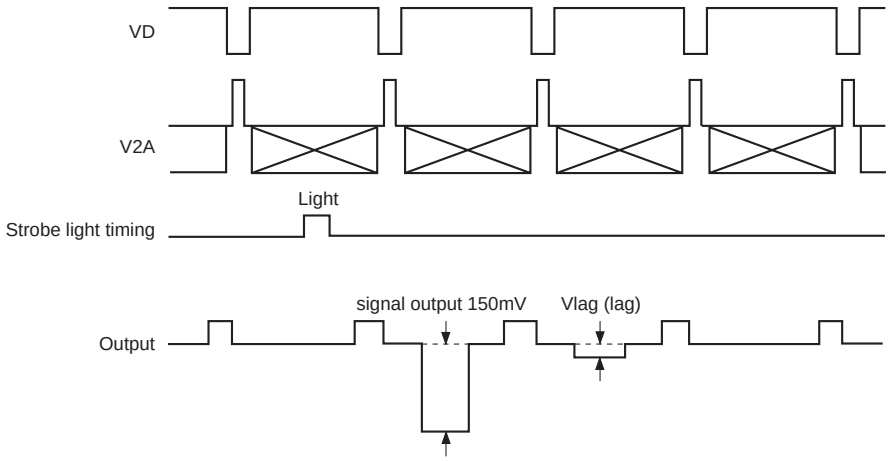
5. Dark signal
   Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

6. Dark signal shading
   After measuring 5, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

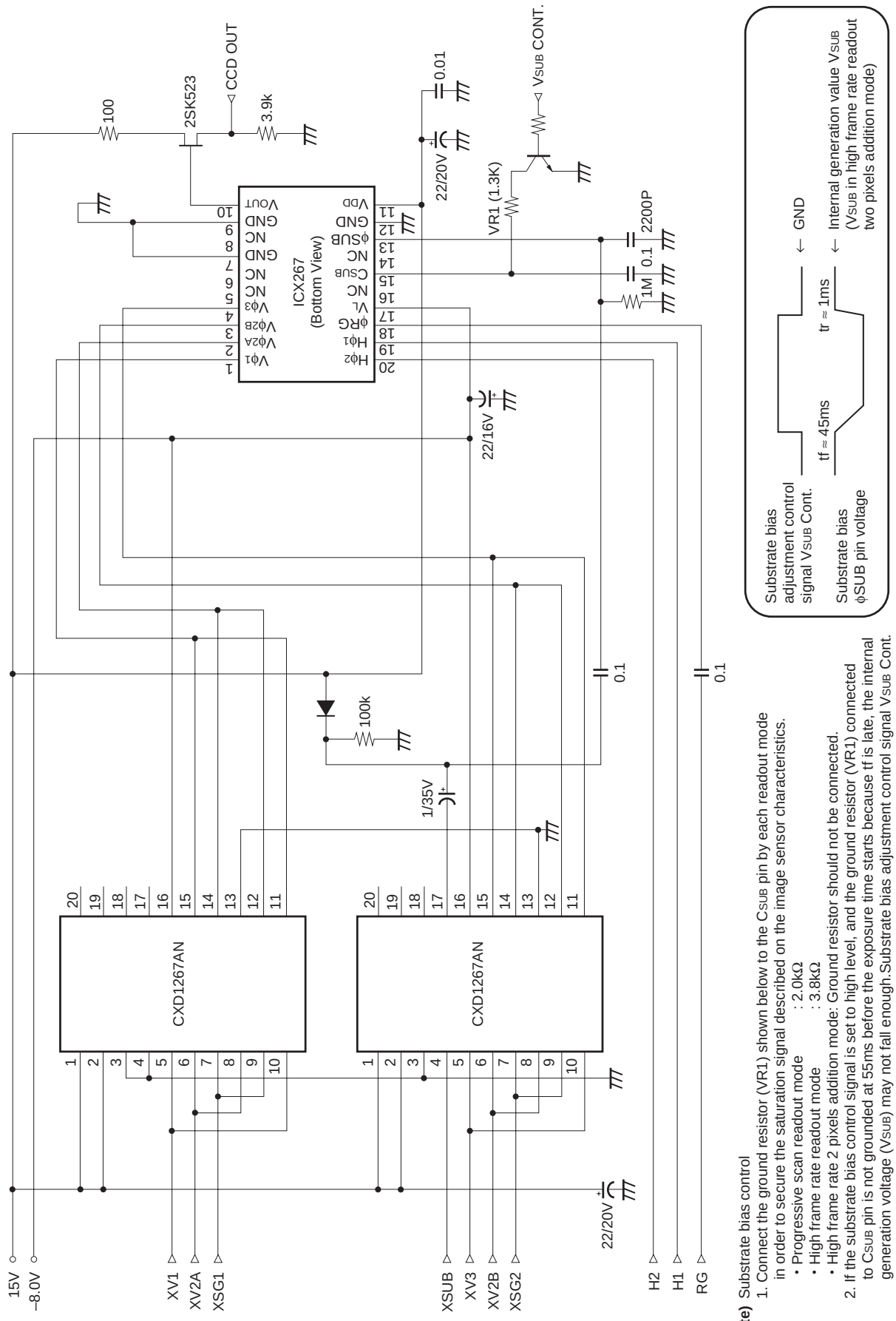
   $\Delta Vdt = Vdmax - Vdmin$ [mV]

7. Lag
   Adjust the signal output value generated by strobe light to 150mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

   $Lag = (Vlag/150) \times 100$ [%]



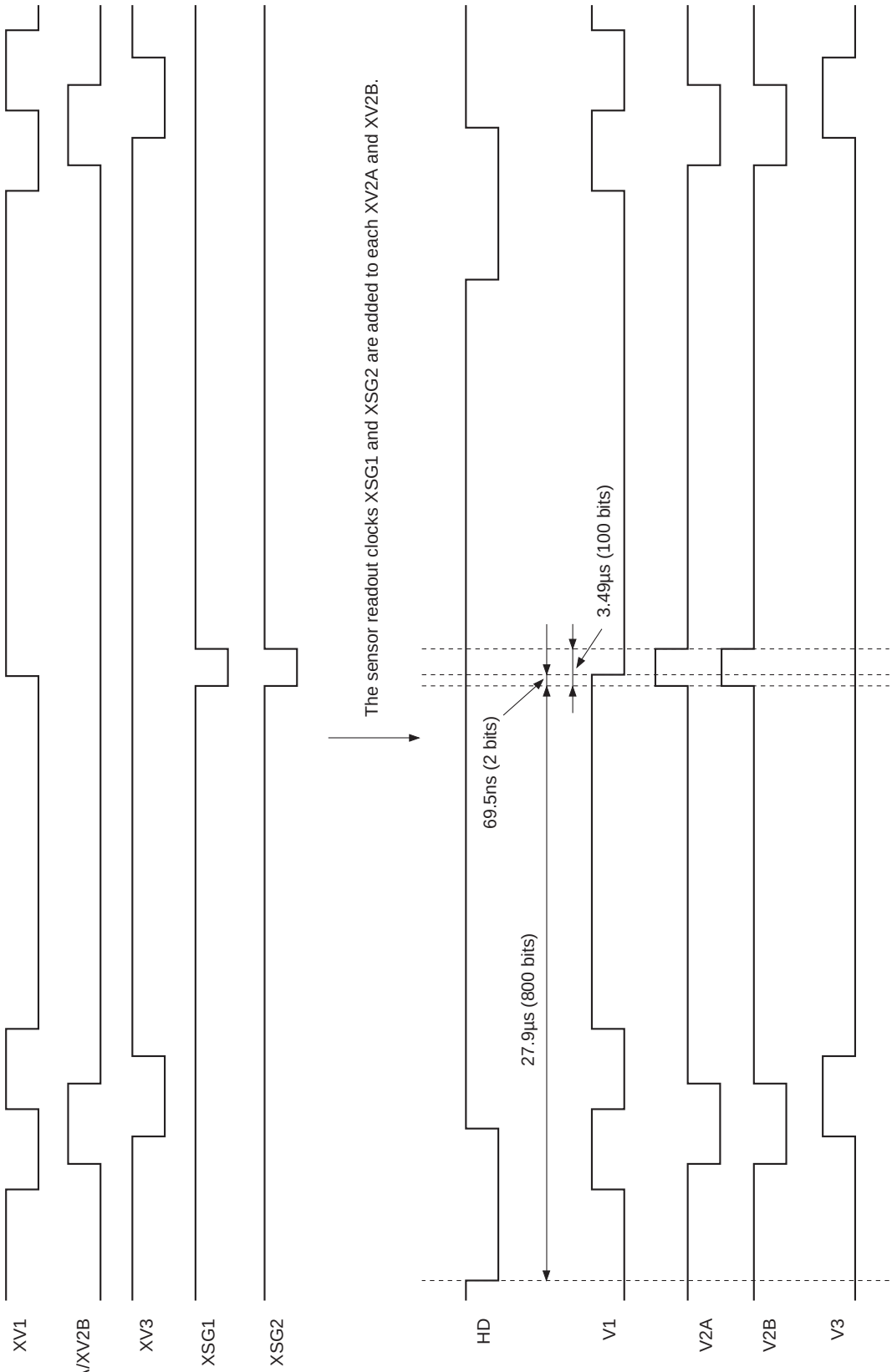
Drive Circuit



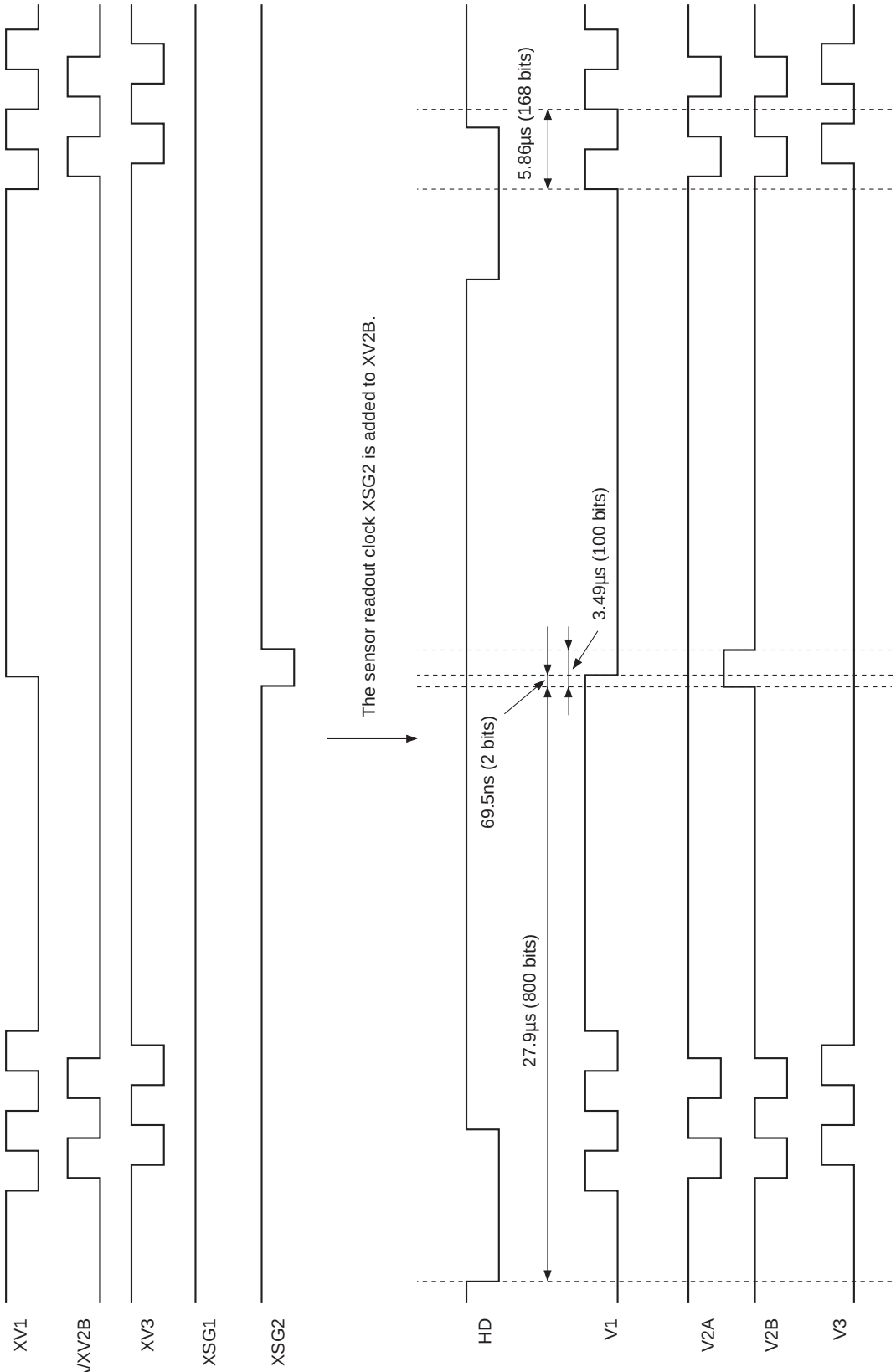
Note) Substrate bias control

1. Connect the ground resistor (VR1) shown below to the CSUB pin by each readout mode in order to secure the saturation signal described on the image sensor characteristics.
   - Progressive scan readout mode : 2.0kΩ
   - High frame rate readout mode : 3.8kΩ
   - High frame rate 2 pixels addition mode: Ground resistor should not be connected.
2. If the substrate bias control signal is set to high level, and the ground resistor (VR1) connected to CSUB pin is not grounded at 55ms before the exposure time starts because tf is late, the internal generation voltage (VSUB) may not fall enough.Substrate bias adjustment control signal VSUB Cont.

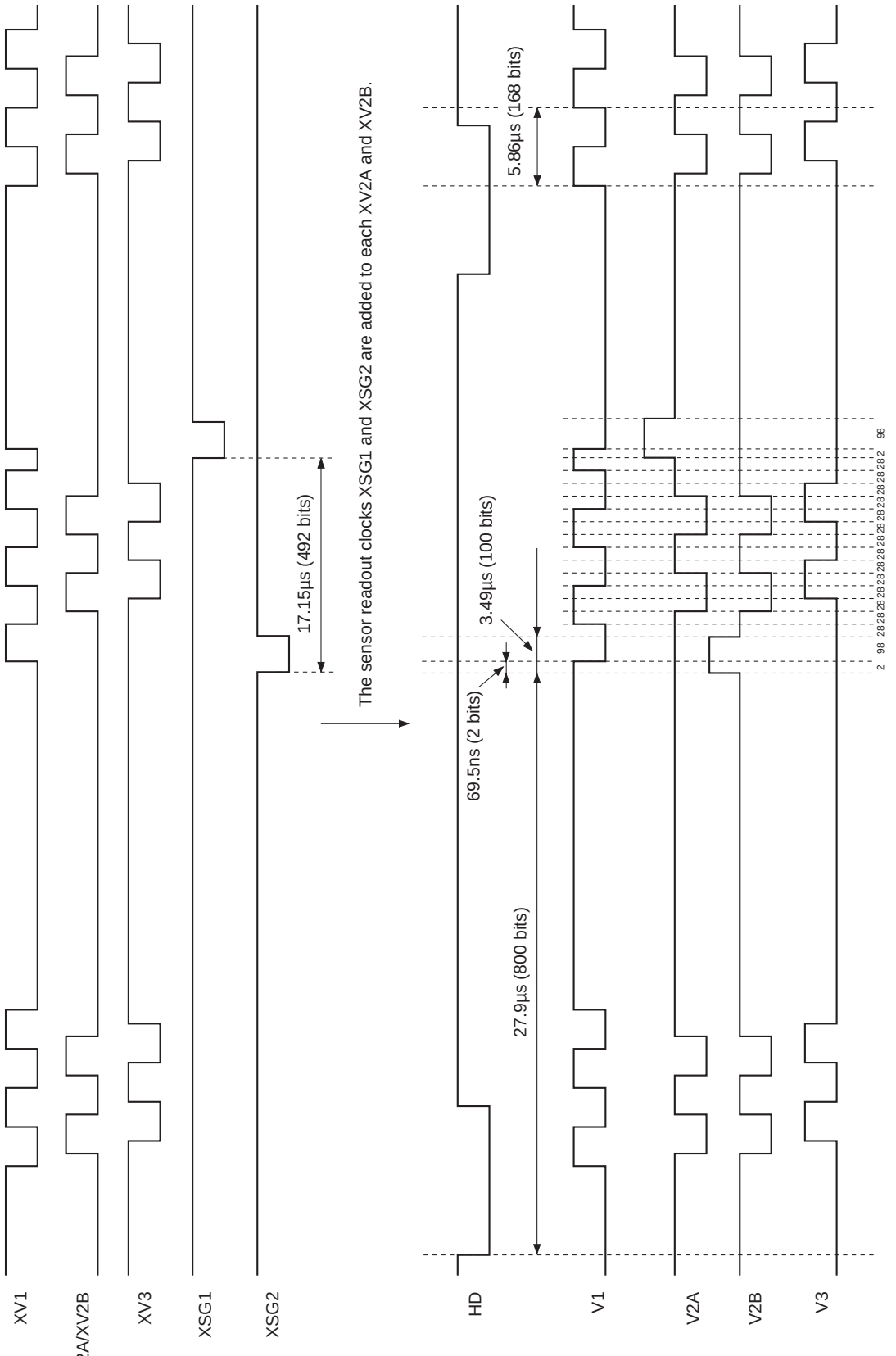
Sensor Readout Clock Timing Chart **Progressive Scan Mode**



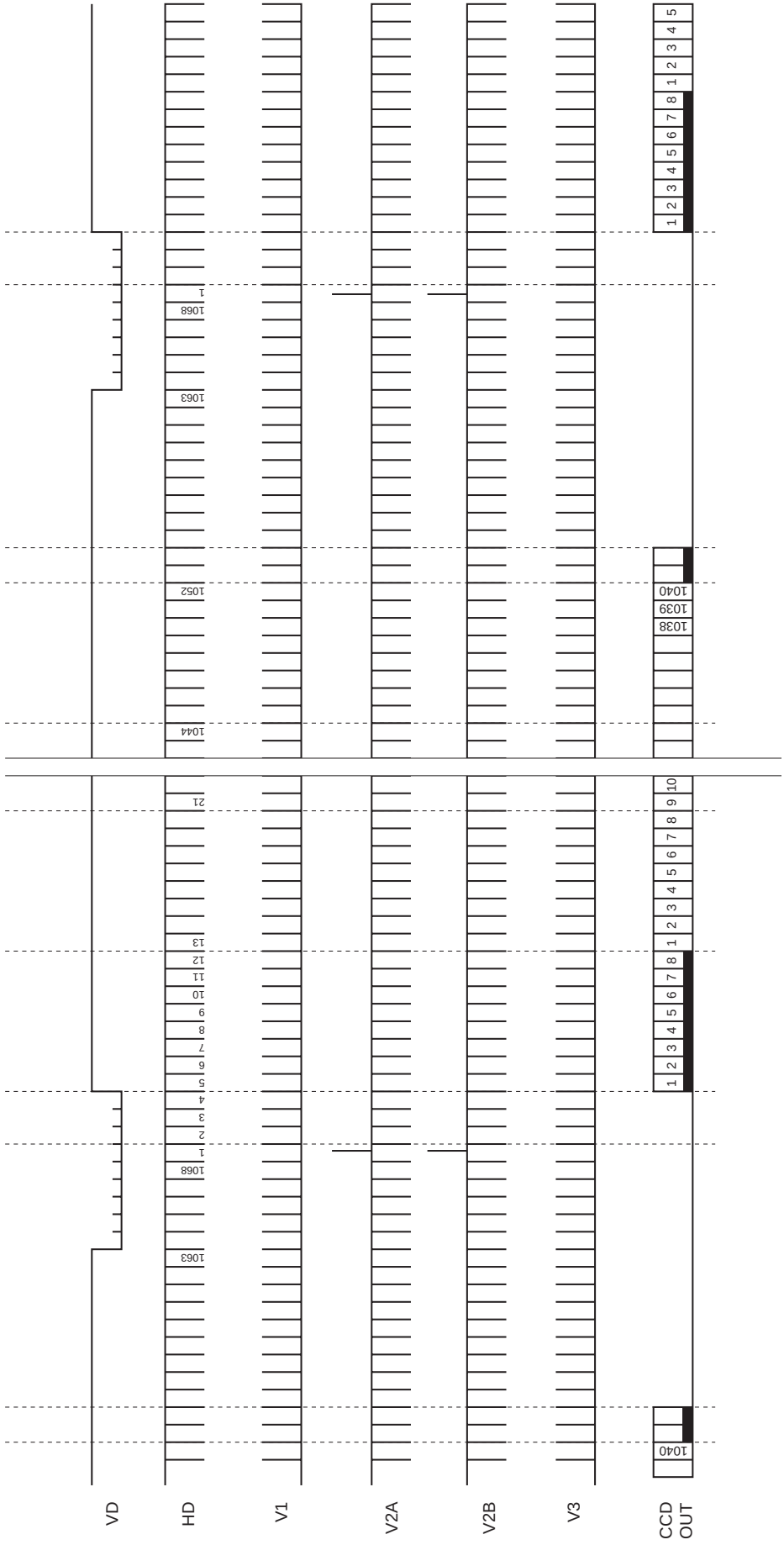
Sensor Readout Clock Timing Chart **High Frame Rate Readout Mode**



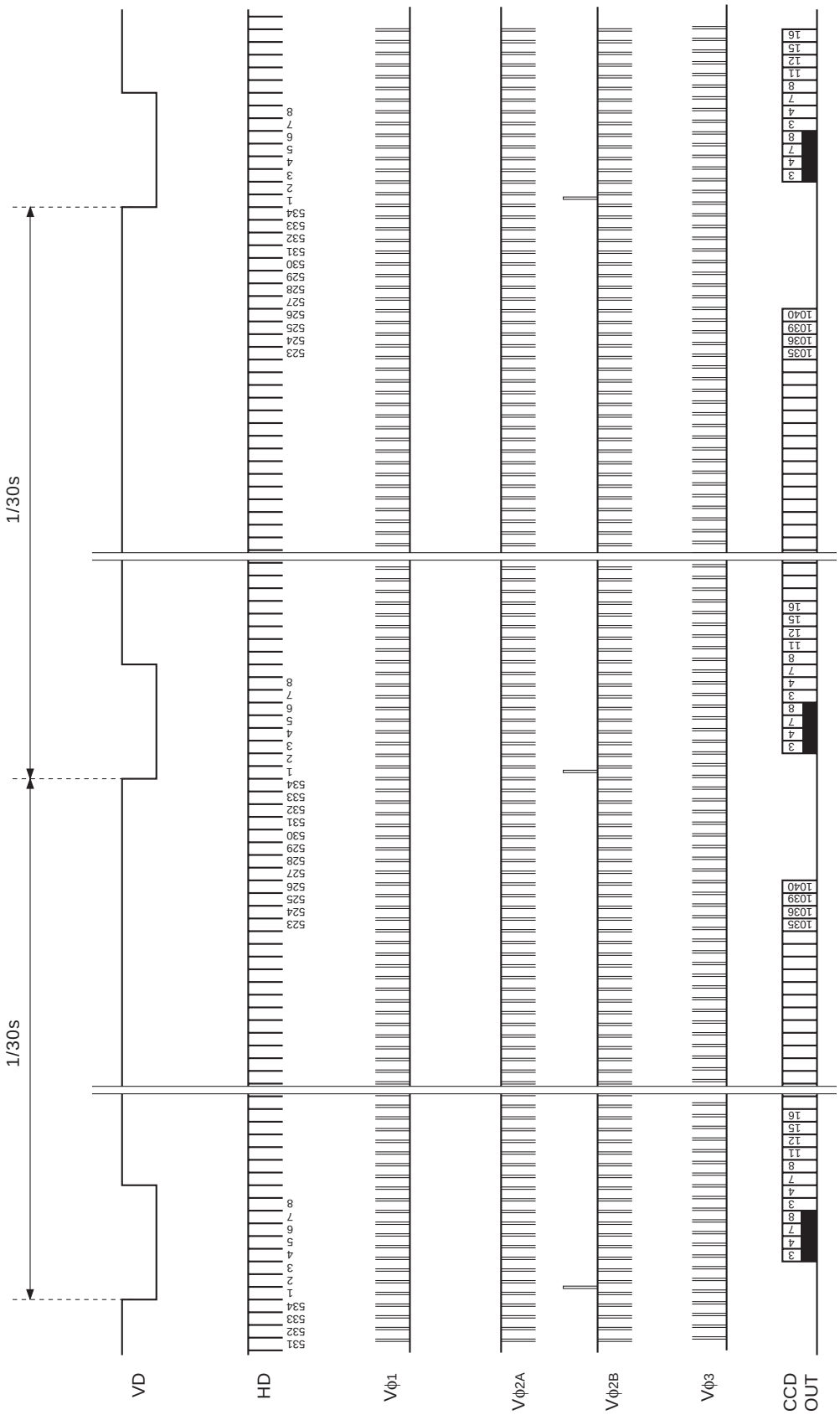
Sensor Readout Clock Timing Chart **High Frame Rate Readout Two Pixels Addition Mode**



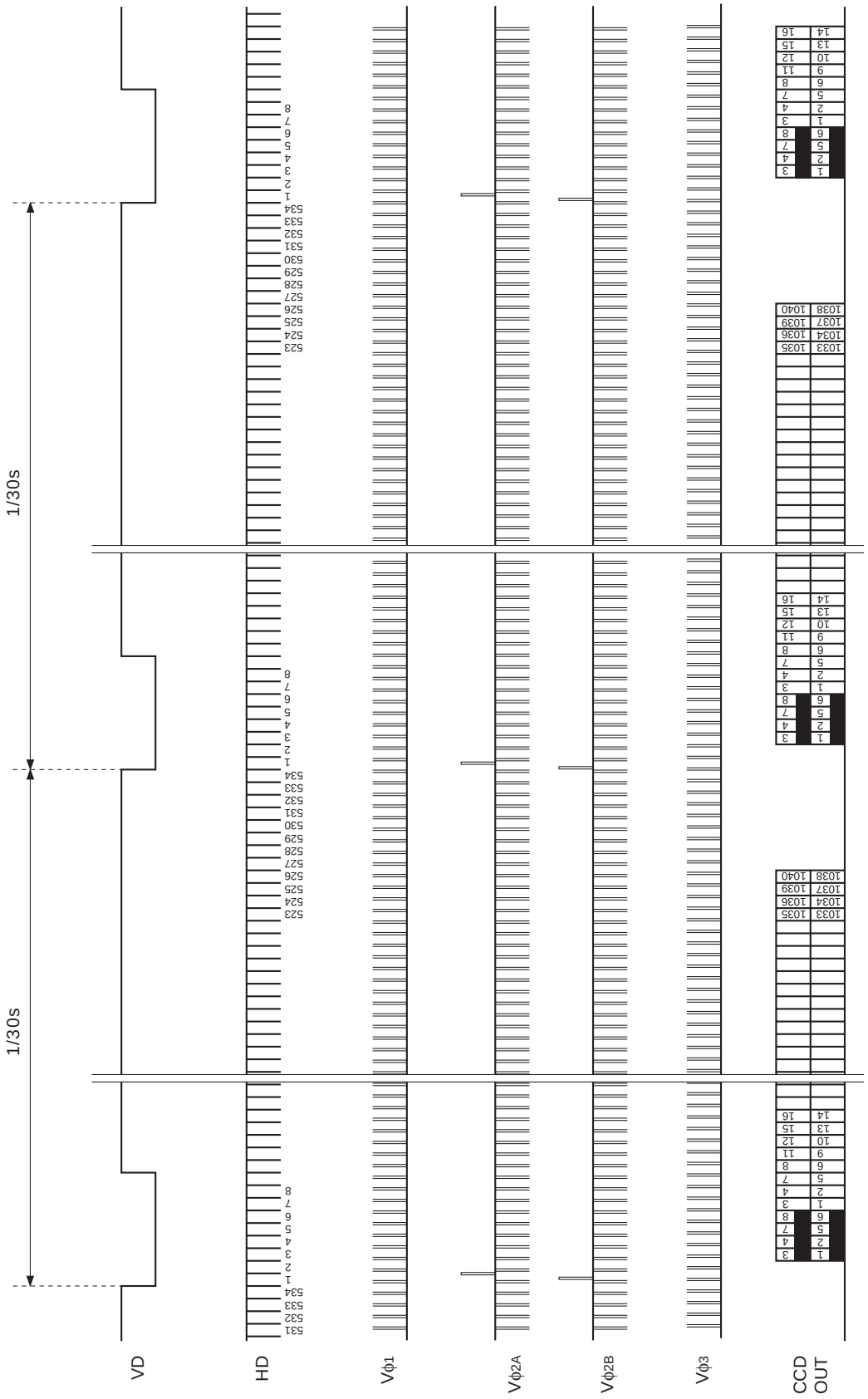
Drive Timing Chart (Vertical Sync) Progressive Scan Mode



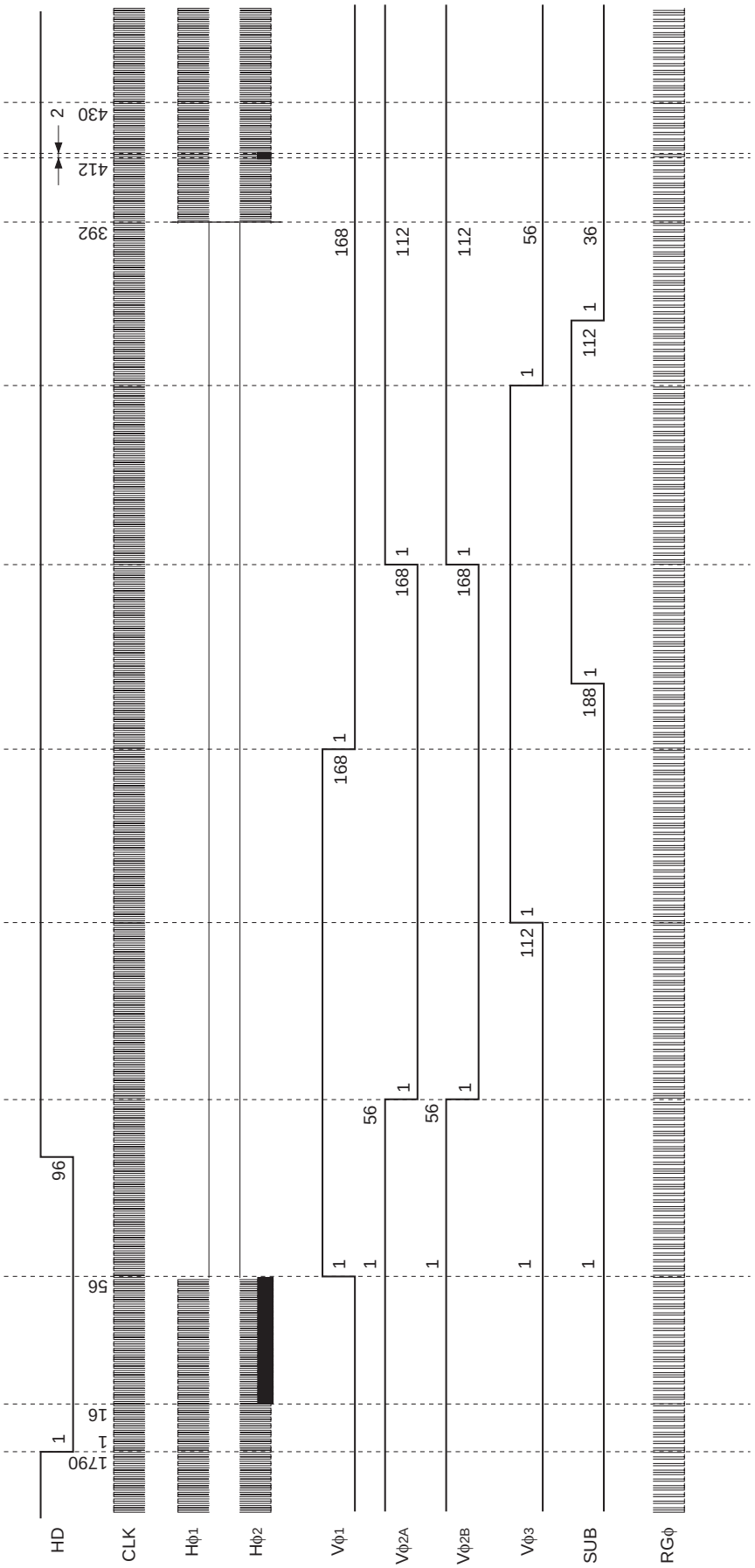
Drive Timing Chart (Vertical Sync) **High Frame Rate Readout Mode**



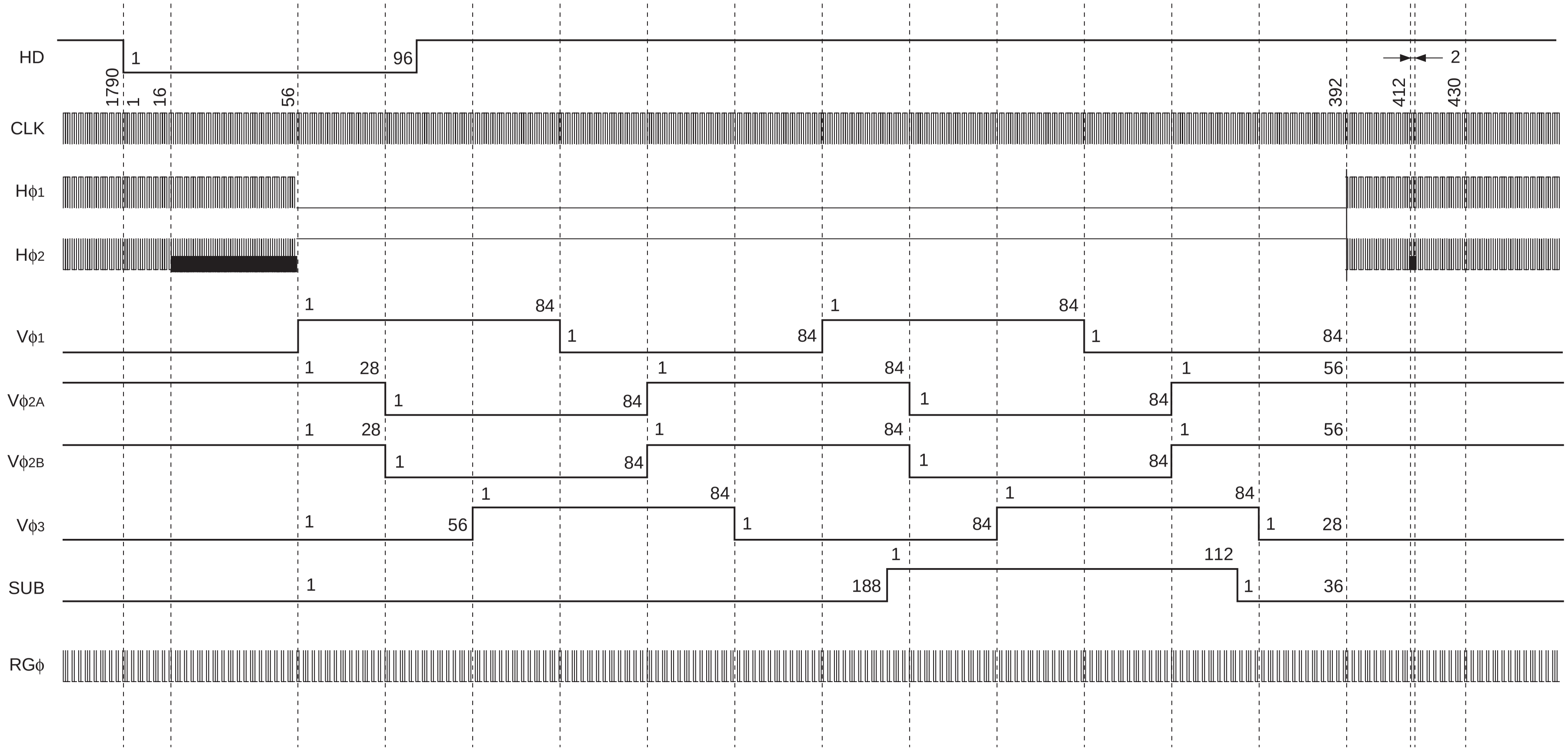
Drive Timing Chart (Vertical Sync) **High Frame Rate Readout Two Pixels Addition Mode**



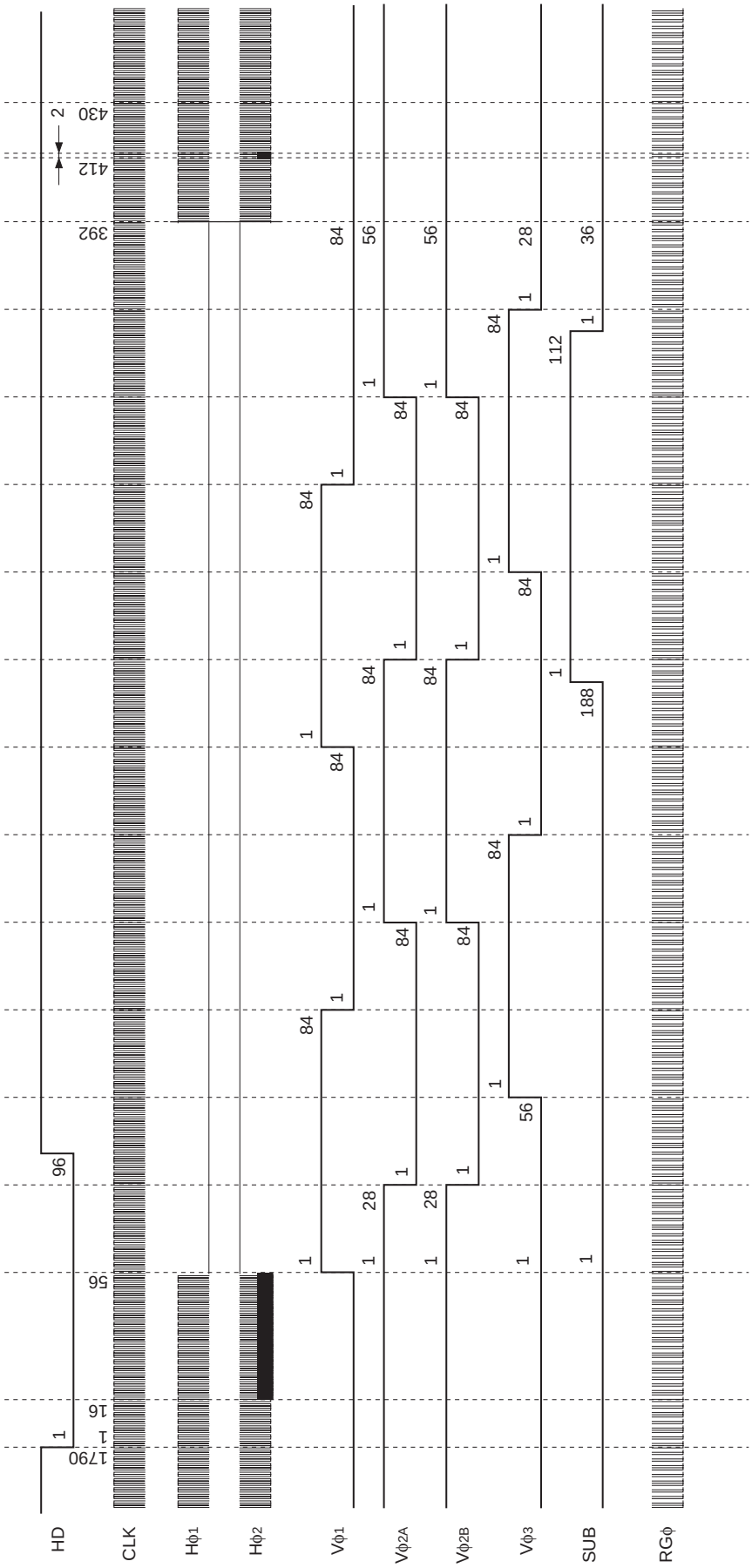
Drive Timing Chart (Horizontal Sync) **Progressive Scan Mode**



Drive Timing Chart (Horizontal Sync) High Frame Rate Readout Mode



Drive Timing Chart (Horizontal Sync) **High Frame Rate Readout Two Pixels Addition Mode**



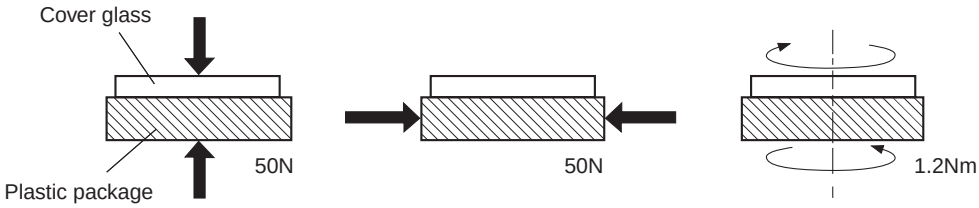
Notes on Handling

1) Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non-chargeable gloves, clothes or material.
      Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

3) Dust and dirt protection
   Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operation as required, and use them.
   a) Perform all assembly operations in a clean room (class 1000 or less).
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Installing (attaching)
   a) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)



Compressive strength **Torsional strength**

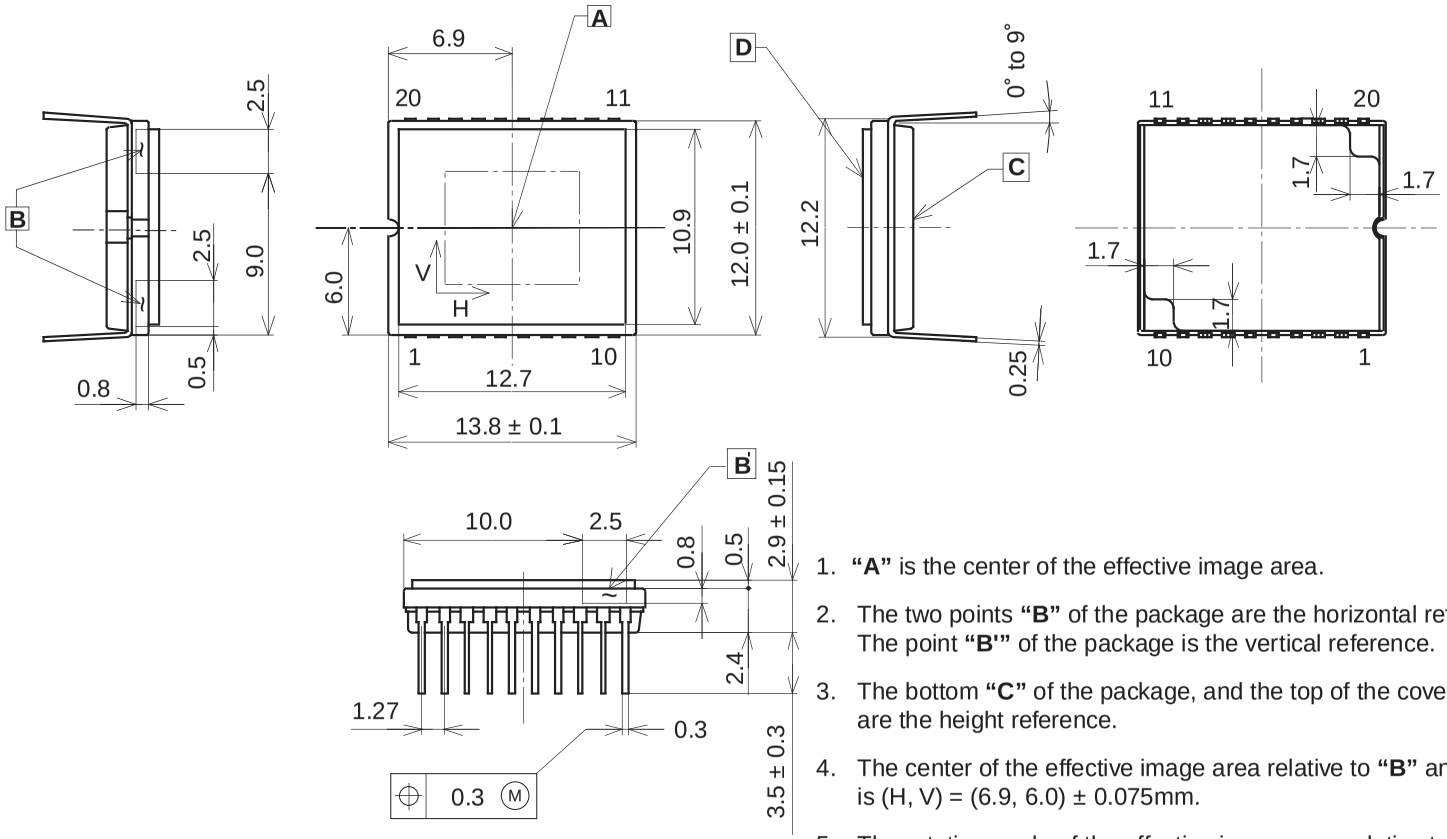
   b) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.

c) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to the other locations as a precaution.
d) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.
e) If the lead bend repeatedly and the metal, etc., clash or rub against the package, the dust may be generated by the fragments of resin.
f) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyano-acrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

5) Others
a) Do not expose to strong light (sun rays) for long periods. For continuous using under cruel condition exceeding the normal using condition, consult our company.
b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
c) The brown stain may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.

Package Outline Unit: mm

20 pin DIP



PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.95g
DRAWING NUMBER	AS-B6-04(E)

1. **"A"** is the center of the effective image area.
2. The two points **"B"** of the package are the horizontal reference.
   The point **"B'"** of the package is the vertical reference.
3. The bottom **"C"** of the package, and the top of the cover glass **"D"** are the height reference.
4. The center of the effective image area relative to **"B"** and **"B'"** is (H, V) = (6.9, 6.0) ± 0.075mm.
5. The rotation angle of the effective image area relative to H and V is ± 1°.
6. The height from the bottom **"C"** to the effective image area is 1.41 ± 0.10mm.
   The height from the top of the cover glass **"D"** to the effective image area is 1.49 ± 0.15mm.
7. The tilt of the effective image area relative to the bottom **"C"** is less than 50µm.
   The tilt of the effective image area relative to the top **"D"** of the cover glass is less than 50µm.
8. The thickness of the cover glass is 0.5mm, and the refractive index is 1.5.
9. The notches on the bottom of the package are used only for directional index, they must not be used for reference of fixing.