Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 16K (16K x 1-BIT) SRAM

PRELIMINARY
IDT10480
IDT100480
IDT101480

FEATURES:

- 16,384 x 1-bit organization
- Address access time: 3/3.5/4/5/7/8/10/12/15 ns
- Low power dissipation: 1000mW (typ.)
- Guaranteed Output Hold time
- Fully compatible with ECL logic levels
- Separate data input and output
- JEDEC standard through-hole package
- Guaranteed-performance die available for MCMs/hybrids

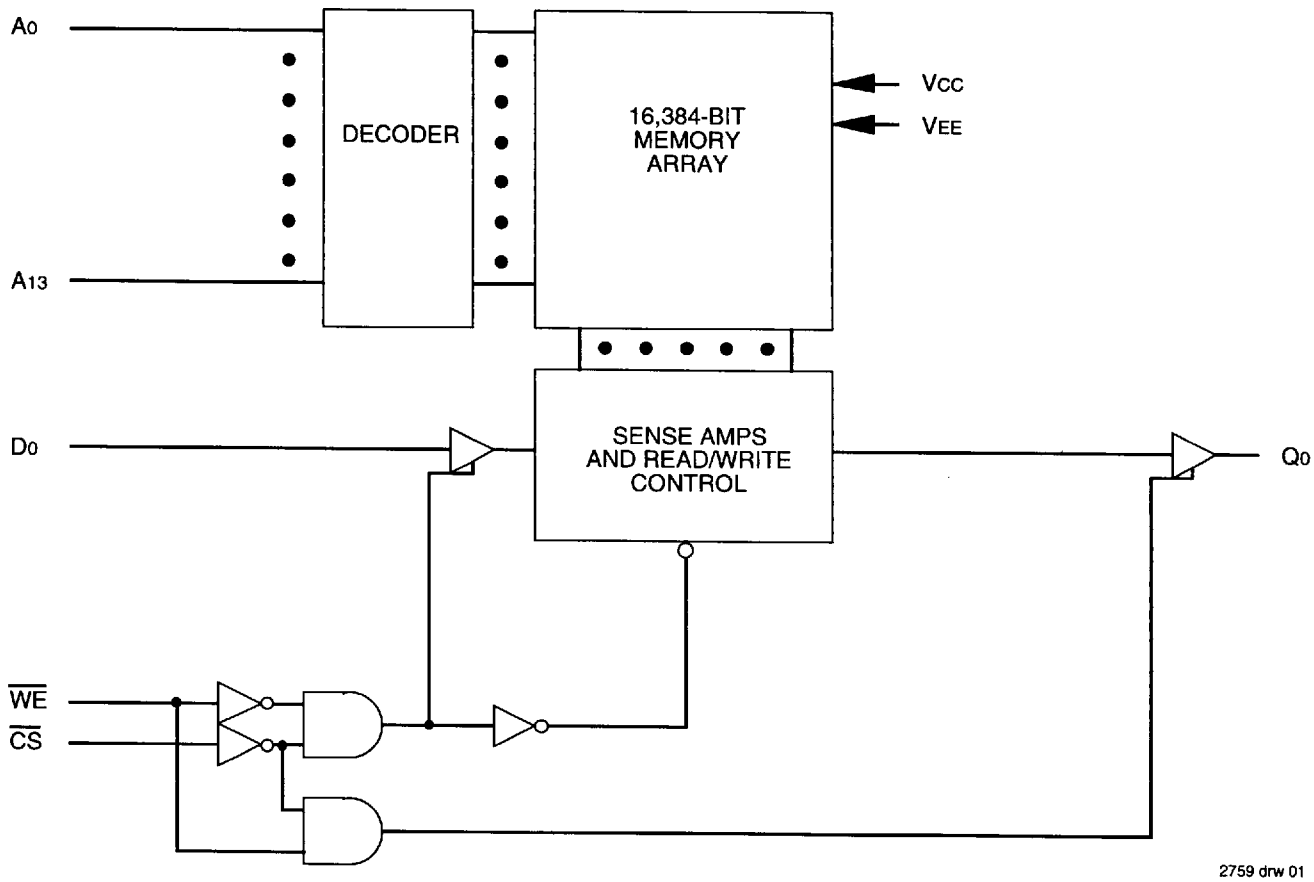
DESCRIPTION:

The IDT10480, IDT100480 and IDT101480 are 16,384-bit high-speed BiCMOS ECL static random access memories organized as 16K x 1, with separate data input and output. All I/Os are fully compatible with ECL levels.

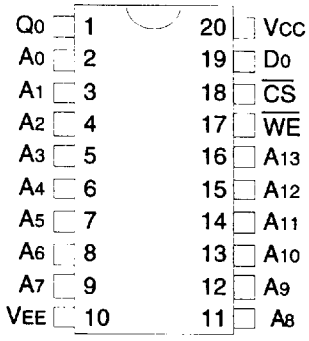
These devices are part of a family of asynchronous one-bit-wide ECL SRAMs. The device has been configured to follow the standard ECL SRAM JEDEC pinout. Because they are manufactured in BiCMOS technology, power dissipation is greatly reduced over equivalent bipolar devices.

The fast access time and guaranteed Output Hold time allow greater margin for system timing variation. DataIN setup time specified with respect to the trailing edge of Write Pulse eases write timing allowing balanced Read and Write cycle times.

FUNCTIONAL BLOCK DIAGRAM



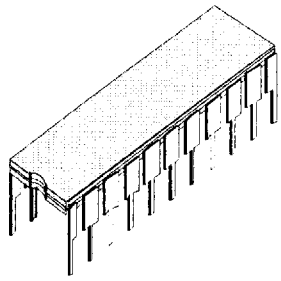
PIN CONFIGURATIONS



TOP VIEW

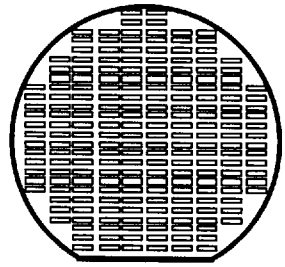
2759 drw 02

PACKAGES



2759 drw 04

300-Mil-Wide CERDIP PACKAGE D20-1



Hi-Rel Die For Hybrid and MCM Applications

2759 drw 05

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A13	Address Inputs
D0	Data Input
Q0	Data Output
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage

2759 tbl 01

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	DIP		
		Typ.	Max.	Unit
CIN	Input Capacitance	4	—	pF
COUT	Output Capacitance	6	—	pF

2759 tbl 02

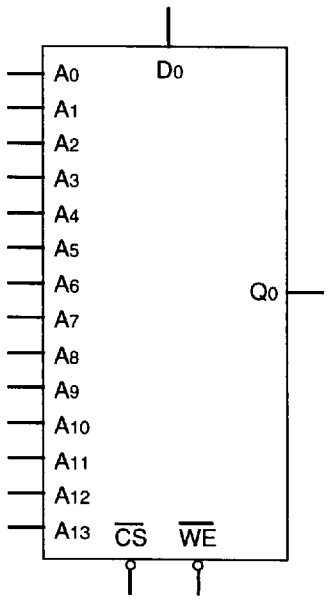
TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	DataOUT	Function
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

NOTE:
1. H = HIGH, L = LOW, X = Don't Care

2759 tbl 03

LOGIC SYMBOL



2759 drw 06

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to –7.0	V
T_A	Operating Temperature	10K 100K 101K	0 to +75 0 to +85 0 to +75	°C
T_{BIAS}	Temperature Under Bias		–55 to +125	°C
T_{STG}	Storage Temperatuure	Ceramic Plastic	–65 to +150 –55 to +125	°C
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		–50	mA

NOTE:
2759 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC ELECTRICAL OPERATING RANGES

I/O	V_{EE}	T_A
10K	–5.2V ± 5%	0 to +75°C, air flow exceeding 2 m/sec
100K	–4.5V ± 5%	0 to +85°C, air flow exceeding 2 m/sec
101K	–4.75V to –5.46V	0 to +75°C, air flow exceeding 2 m/sec

2759 tbl 05

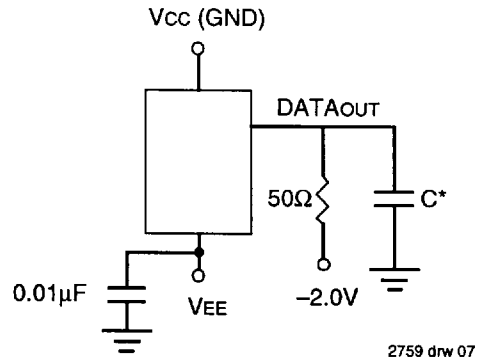
DC ELECTRICAL CHARACTERISTICS (1)

Symbol	Parameter		10K Min.	10K Max.	TA	100K/101K Min.	100K/101K Max.	Unit
V_{OH}	Output HIGH Voltage (V_{IN}= $V_{IH(Max)}$ or $V_{IL(Min)}$)		–1000 –960 –900	–840 –810 –720	0°C 25°C 75°C	–1025	–880	mV
V_{OL}	Output LOW Voltage (V_{IN}= $V_{IH(Max)}$ or $V_{IL(Min)}$)		–1870 –1850 –1830	–1665 –1650 –1625	0°C 25°C 75°C	–1810	–1620	mV
V_{OHC}	Output Threshold HIGH Voltage (V_{IN}= $V_{IH(Min)}$ or $V_{IL(Max)}$)		–1020 –980 –920	— — —	0°C 25°C 75°C	–1035	—	mV
V_{OLC}	Output Threshold LOW Voltage (V_{IN}= $V_{IH(Min)}$ or $V_{IL(Max)}$)		— — —	–1645 –1630 –1605	0°C 25°C 75°C	—	–1610	mV
V_{IH}	Input HIGH Voltage (Guaranteed Input Voltage High for All Inputs)		–1145 –1105 –1045	–840 –810 –720	0°C 25°C 75°C	–1165	–880	mV
V_{IL}	Input LOW Voltage (Guaranteed Input Voltage Low for All Inputs)		–1870 –1850 –1830	–1490 –1475 –1450	0°C 25°C 75°C	–1810	–1475	mV
I_{IH}	Input HIGH Current							
	V_{IN}= $V_{IH(Max)}$	CS Others	— —	220 110	— —	— —	220 110	µA µA
I_{IL}	Input LOW Current							
	V_{IN}= $V_{IL(Min)}$	CS Others	0.5 –50	170 90	— —	0.5 50	170 90	µA µA
I_{EE}	Supply Current		–210	—	—	–190 (100K) –210 (101K)	— —	mA

NOTE:
1. RL = 50Ω to –2V, air flow exceeding 2m/sec.

2759 tbl 05

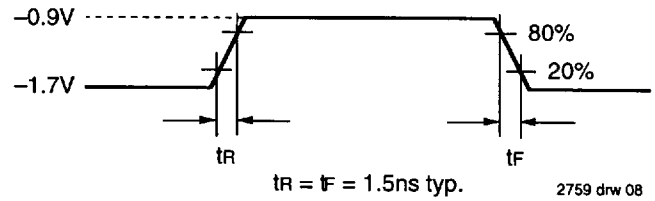
AC TEST LOAD CONDITION



2759 drw 07

NOTE:
1. "*" includes probe and jig capacitance.
   C <5pF (3, 3.5ns speed grades)
   C <30pF (all other speed grades.)

AC TEST INPUT PULSE



2759 drw 08

NOTE:
1. All timing measurements are referenced to 50% input levels.

RISE/FALL TIME

Symbol	Parameter	Min.	Typ.	Max.	Unit
tR	Output Rise Time	—	1.5	—	ns
tF	Output Fall Time	—	1.5	—	ns

2759 tbl 06

FUNCTIONAL DESCRIPTION

The IDT10480, IDT100480, and IDT101480 BiCEMOS ECL static RAMs provide high speed with low power dissipation typical of BiCMOS ECL. These devices follow the conventional pinout and functionality for 16K x 1 ECL SRAMs.

READ TIMING

The read timing on these asynchronous devices is straightforward. DataOUT is held LOW until the device is selected by Chip Select (CS). The Address (ADDR) settles and data appears on the output after time tAA. Note that DataOUT is held for a short time (tOH) after the address begins to change for the next access, then ambiguous data is on the bus until a new time tAA.

WRITE TIMING

To write data to the device, a Write Pulse need be formed on the Write Enable input (WE) to control the write to the SRAM array.

While CS and ADDR must be set-up when WE goes LOW, DataIN can settle after the falling edge of WE, giving the data path extra margin. Data is written to the memory cell at the end of the Write Pulse, and addresses and Chip Select must be held after the rising edge of the Write Pulse to ensure satisfactory completion of the cycle.

DataOUT is disabled (held LOW) during the Write Cycle. If CS is held LOW (active) and addresses remain unchanged, the DataOUT pin will output the written data after "Write Recovery time" (tWR).

Because of the very short Write Pulse requirement, these devices can be cycled as quickly for Writes as for Reads.

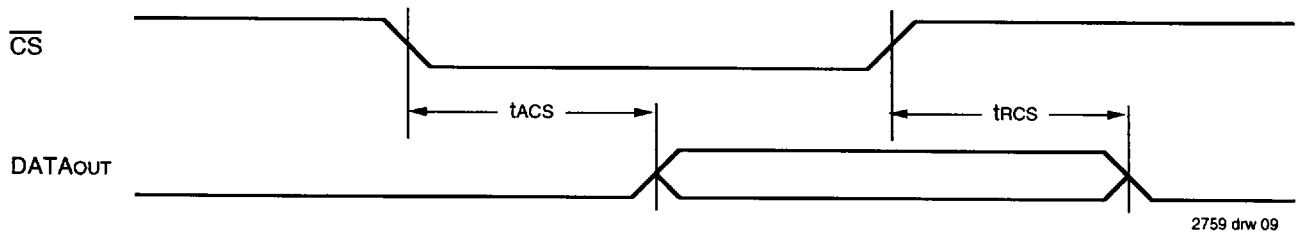
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	S3		S3.5		S4		S5		S7 to S15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tACS	Chip Select Access Time	—	2.0	—	2.5	—	2.5	—	2.5	—	3.0	ns
tRCS	Chip Select Recovery Time	—	2.0	—	2.5	—	2.5	—	2.5	—	3.0	ns
tAA	Address Access Time	—	3.0	—	3.5	—	4.0	—	5.0	—	7.0	ns
tOH	Data Hold from Address Change	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns

NOTE:
2759 tbl 07

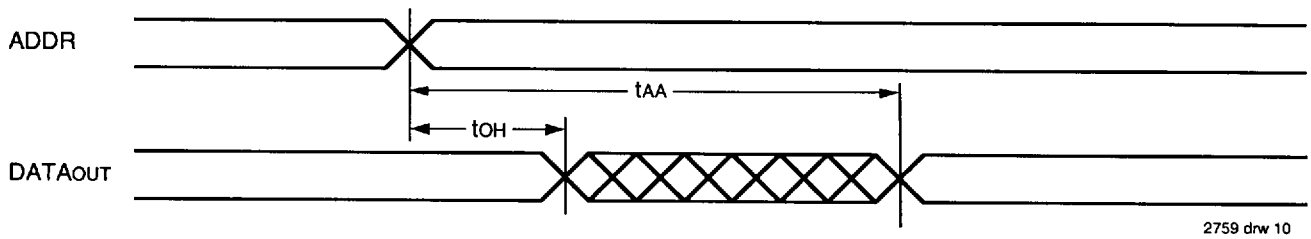
1. Input and Output reference level is 50% point of waveform.
2. Output load capacitance, C < 5pF (3, 3.5ns speed grades only), see "AC Test Load Condition" on previous page.

READ CYCLE GATED BY CHIP SELECT (1, 2)



2759 drw 09

READ CYCLE GATED BY ADDRESS (1, 3)



2759 drw 10

NOTES:
1. WE is HIGH for read cycle.
2. Address valid prior to or minimum tAA–tACS before CS active.
3. CS active prior to or minimum tAA–tACS before address valid.

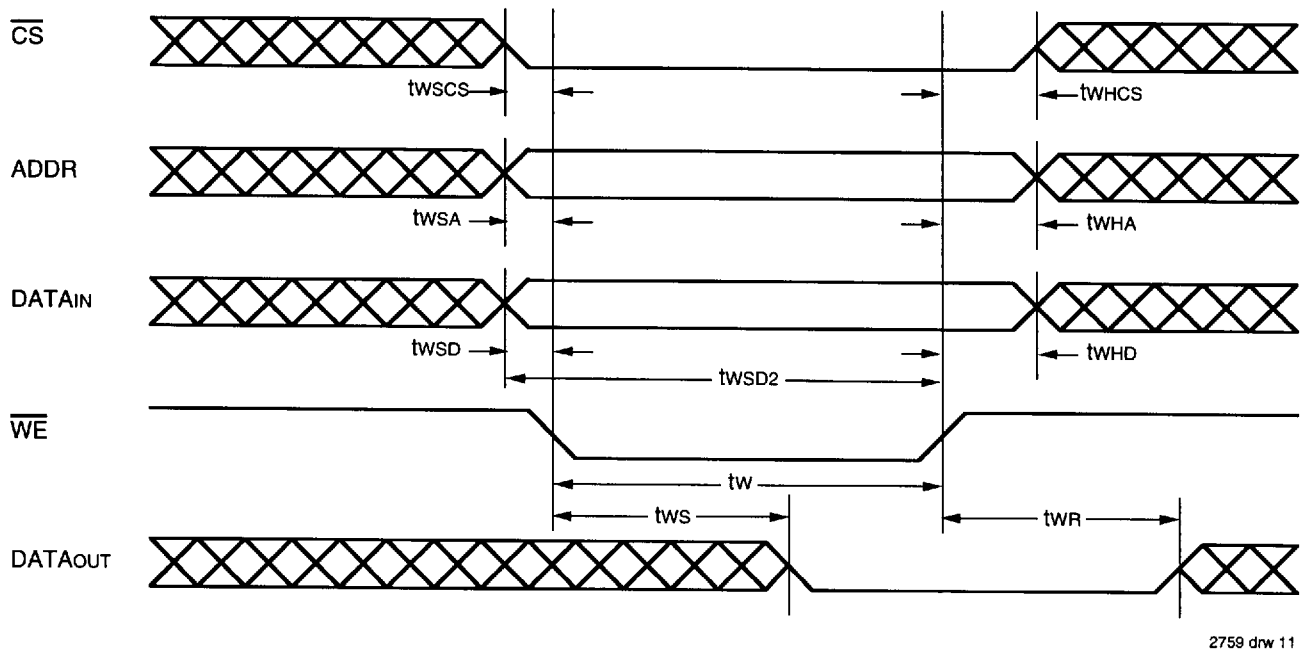
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	S3		S3.5		S4		S5		S7 to S15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_W	Write Pulse Width (t_{WSA} = minimum)	2.5	—	3.0	—	3.0	—	4.0	—	6.0	—	ns
t_{WSD}	Data Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WSD2}[2]	Data Set-up Time to $\overline{WE}$ High	2.0	—	2.0	—	2.0	—	3.0	—	5.0	—	ns
t_{WSA}	Address Set-up Time (t_W = minimum)	0	—	0	—	0	—	0	—	0	—	ns
t_{WSCS}	Chip Select Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHD}	Data Hold Time	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
t_{WHA}	Address Hold Time	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
t_{WHCS}	Chip Select Hold Time	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
t_{WS}	Write Disable Time	—	3.0	—	3.0	—	3.0	—	3.0	—	5.0	ns
t_{WR}[3]	Write Recovery Time	—	3.0	—	3.0	—	3.0	—	3.0	—	5.0	ns

2759 tbl 08

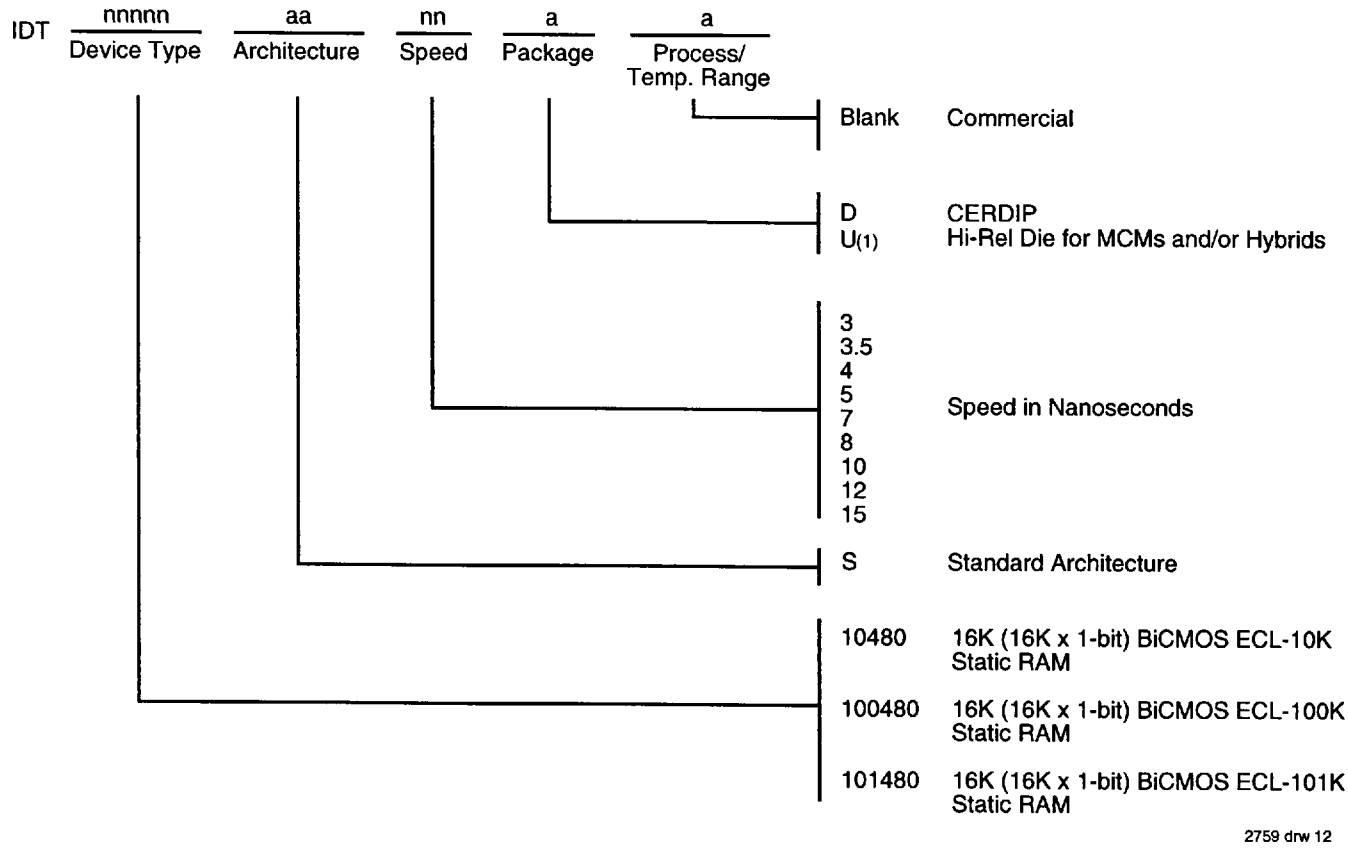
NOTE:
1. Input and Output reference level is 50% point of waveform.
2. t_{WSD} is specified with respect to the falling edge of $\overline{WE}$ for compatibility with bipolar part specifications, but this device actually only requires t_{WSD2} with respect to rising edge of $\overline{WE}$.
3. t_{WR} is defined as the time to reflect the newly written data on the Data Output (Q0) when no new Address Transition occurs.

WRITE CYCLE TIMING DIAGRAM



2759 drw 11

ORDERING INFORMATION(1)



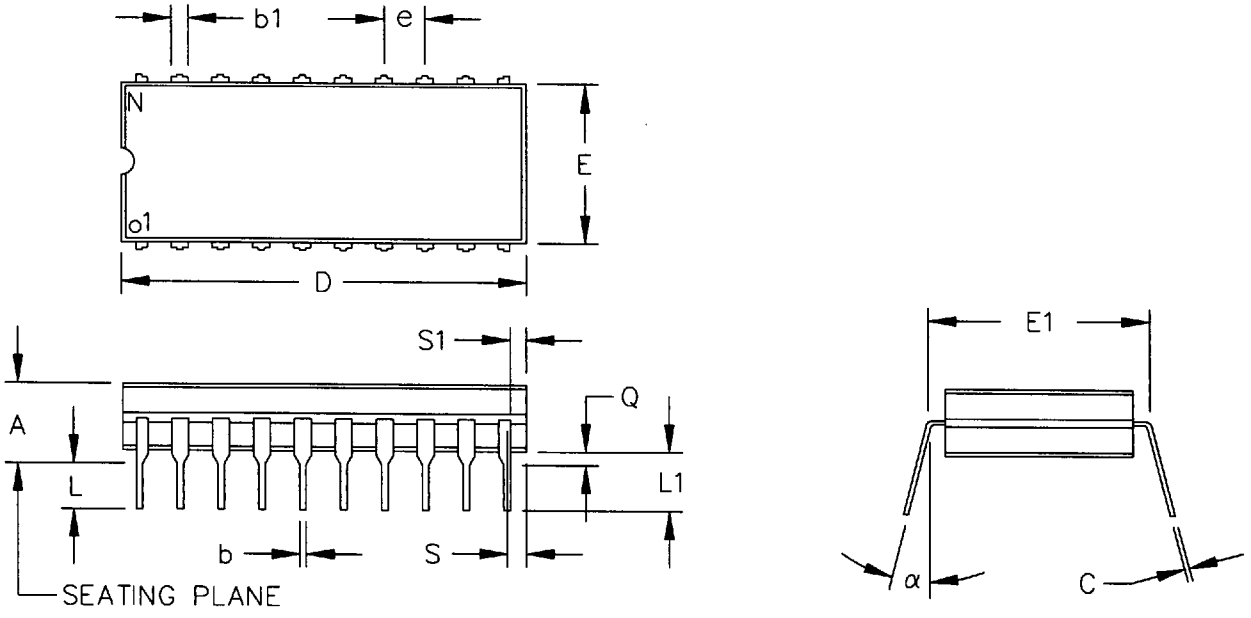
NOTE:
1. Please contact your IDT Sales Representative for more information on specifications and availability of Die products.

Integrated Device Technology, Inc.

2975 Stender Way, Santa Clara, CA 95054-3090 Telephone: (408) 727-6116 FAX 408-492-8674

CERDIP (Continued)

REV	DCN	DESCRIPTION	DATE	APPROVED
07	17515	UPDATED TO STANDARDIZE DWG	6/20/90	D Guilhamet
08	18086	REVISED A, Q, & S DIMENSIONS	8/17/90	D Guilhamet
09	22233	CHANGED b1 MIN DIMENSION		



NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "N" REPRESENTS THE NUMBER OF LEADS.

DWG #	D20-1	
SYMBOL	MIN	MAX
A	.140	.200
b	.015	.021
b1	.045	.060
C	.009	.012
D	.935	1.060
E	.285	.310
E1	.290	.320
e	.100 BSC	
L	.125	.175
L1	.150	–
Q	.015	.060
S	.020	.080
S1	.005	–
α	0°	15°
N	20	

MIL-M-38510	CONFIGURATION	EXCEPTIONS
JEDEC	D-8	NONE
	NOT REGISTERED	

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRAC DEC ANGLES
± – ± – ± –

APPROVALS	DATE
DRAWN AA	08/90
CHECKED	

Integrated Device Technology, Inc.
3236 Scott Blvd., Santa Clara, CA 95051
(408) 727-6116 FAX: (408) 727-2328

20 LD CERDIP MKT DWG

SCALE	SIZE	DRAWING NO.	REV
N/A	A	PSC-2015	09

DO NOT SCALE DRAWING | SHEET 64