REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
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SHEET	15	16	17	18	19	20	21												

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
92/02/28

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, BINARY FILTER AND TEMPLATE MATCHER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-90504
A	67268	

SHEET 1 OF 21 1

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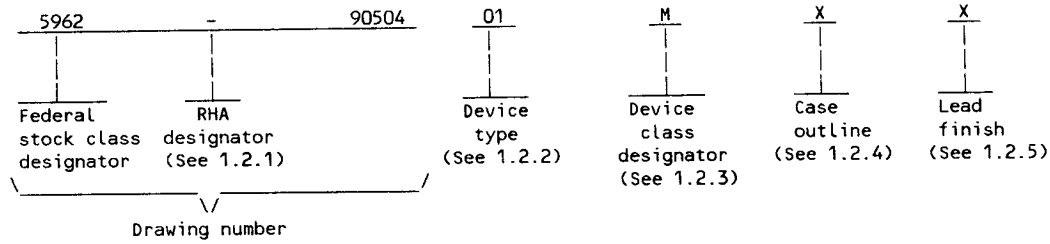
5962-E1581

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	L64230-12	1024 tap binary correlator and template matcher (12 MHz)
02	L64230-16	1024 tap binary correlator and template matcher (16 MHz)

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). For device classes M, B, and S, case outline(s) shall meet the requirements in appendix C of MIL-M-38510 and as listed below. For device classes Q and V, case outline(s) shall meet the requirements of MIL-I-38535, appendix C of MIL-M-38510, and as listed below.

Outline letter	Case outline
X	P-AH (155-pin, 1.680" x 1.680" x.345"), pin grid package
Y	C-G7 (132-pin, .960" x .960" x .140"), ceramic leaded chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

DC supply voltage	-0.3 V dc to +7 V dc
Input voltage	-0.3 V dc to V_{DD} + 0.3 V dc
DC input current	±10 mA
Ambient storage temperature	-65°C to +150°C
Maximum power dissipation (P_D) 2/	≤ 1.0 W
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-M-38510, appendix C
Lead temperature range (soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions.

DC supply voltage (V_{DD})	4.5 V dc to 5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block and logic diagrams. The block and logic diagrams shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

TABLE I. Electrical performance characteristics. 1 /2 /3 /4/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input high voltage	V_{IH}		1,2,3	All	2.25		V
Input low voltage	V_{IL}		1,2,3	All		0.8	V
Input high current	I_{IH}	$V_{IN} = 5.5\ V$ $V_{DD} = 5.5\ V$	1,2,3	All	0	200	µA
Input low current	I_{IIL}	$V_{IN} = 0\ V$ $V_{DD} = 5.5\ V$	1,2,3	All	-150	0	µA
Output high voltage	V_{OH}	$V_{IN} = 0\ V$ or $4.5\ V$ $V_{DD} = 4.5\ V$ $I_{OH} = -3.2\ mA$	1,2,3	All	2.4		V
Output low voltage	V_{OL}	$V_{IN} = 0\ V$ or $4.5\ V$ $V_{DD} = 4.5\ V$ $I_{OL} = 3.2\ mA$	1,2,3	All		0.4	V
Output short circuit current 5/	I_{OS}	$V_{DD} = 5.5\ V$, $V_o = 5.5\ V$		All	15	130	mA
		$V_{DD} = 5.5\ V$, $V_o = 0.0\ V$			-5	-100	mA
Supply current dynamic	I_{DD}	$C_{LK} = 20\ MHz$ $V_{DD} = 5.5\ V$ $C_L = 50\ pF$	1,2,3	All		300	mA
Supply current static	I_{DDQ}	$V_{DD} = 5.5\ V$ $V_{IN} = V_{DD}$ or $0\ V$	1,2,3	All		10	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/ 3/ 4/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output capacitance	C_{OUT}	See 4.4.1c	4	All		20	pF
Input capacitance	C_{IN}	See 4.4.1c	4	All		15	pF
Functional tests		See 4.4.1b	7,8	All			
Minimum clock cycle time	t_{CYCLE}			01 02	75 60		ns
Minimum clock (CLK) pulse width high	t_{PWH}		9,10,11	01 02	30 25		ns
Minimum clock (CLK) pulse width low	t_{PWL}		9,10,11	01 02	30 25		ns
CLK ↓ before $\overline{WE}$ ↓	t_{CLW}		9,10,11	01 02	30 25		ns
CLK ↑ after $\overline{WE}$ ↑	t_{WCL}		9,10,11	01 02	30 25		ns
Input data (DI) setup time	t_{DIS}		9,10,11	01 02	25 20		ns ns
Input data (DI) hold time	t_{DIH}			01 02	15 7		ns ns
Output delay (DO) from CLK ↑	t_{OUT}		9,10,11	01 02		25 20	ns ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/ 3/ 4/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output delay ($\overline{SRO}$, BNKLDO) from CLK ↑	t_{OD}		9,10,11	01 02		25 20	ns ns
BNKLDI setup time with respect CLK ↑	t_{LS}		9,10,11	01 02	25 20		ns ns
BNKLDI hold time with respect to CLK ↑	t_{LH}		9,10,11	01 02	15 07		ns ns
$\overline{WE}$ setup time with respect to BNKLDI ↑	t_{WL}		9,10,11	01 02	15 7		ns ns
$\overline{WE}$ hold time with respect to BNKLDI ↓	t_{LW}		9,10,11	01 02	t_{PWH} + 25 t_{PWH} + 20		ns ns
Minimum $\overline{WE}$ pulse width low	t_{WW}		9,10,11	01 02	30 25		ns ns
Minimum $\overline{WE}$ cycle time	t_{WC}		9,10,11	01 02	75 60		ns ns
$\overline{SELALL}$ setup time with respect to BNKLDI ↑	t_{SSB}		9,10,11	01 02	200 150		ns ns
$\overline{SELALL}$ hold time with respect to BNKLDI ↓	t_{HSB}		9,10,11	01 02	200 150		ns ns
$\overline{SELALL}$ cycle time	t_{SC}		9,10,11	01 02	400 300		ns ns
$\overline{SELALL}$ pulse width low	t_{WS}		9,10,11	01 02	200 150		ns ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/ 3/ 4/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
REGADR setup time with respect to WE ↓	t_{RS}		9,10,11	01 02	20 15		ns ns
REGADR hold time with respect to WE ↑	t_{RH}		9,10,11	01 02	20 15		ns ns
CI setup time with respect to WE ↓	t_{CS}		9,10,11	01 02	20 15		ns ns
CI hold time with respect to WE ↑	t_{CH}		9,10,11	01 02	20 15		ns ns
CI setup time with SELALL ↓	t_{CSS}		9,10,11	01 02	200 150		ns ns
CI hold time with SELALL ↑	t_{CHS}		9,10,11	01 02	200 150		ns ns
Input partial result (PR) setup time	t_{PRS}		9,10,11	01 02	50 40		ns ns
Input partial result (PR) hold time	t_{PRH}		9,10,11	01 02	15 7		ns ns

1/ All outputs are loaded with 50 pF capacitance load during the ac timing tests.
2/ Subgroups 7 and 8 shall consist of verifying the functionality of the device. These tests form a part of the manufacturer's test tapes and will be maintained and available from the approved source of supply.
3/ See figure 3 for ac timing waveforms.
4/ All test to be performed using worst-case test conditions unless otherwise specified.
5/ Not more than one output may be shorted at a time for a maximum duration of 1 second.

Case outline X

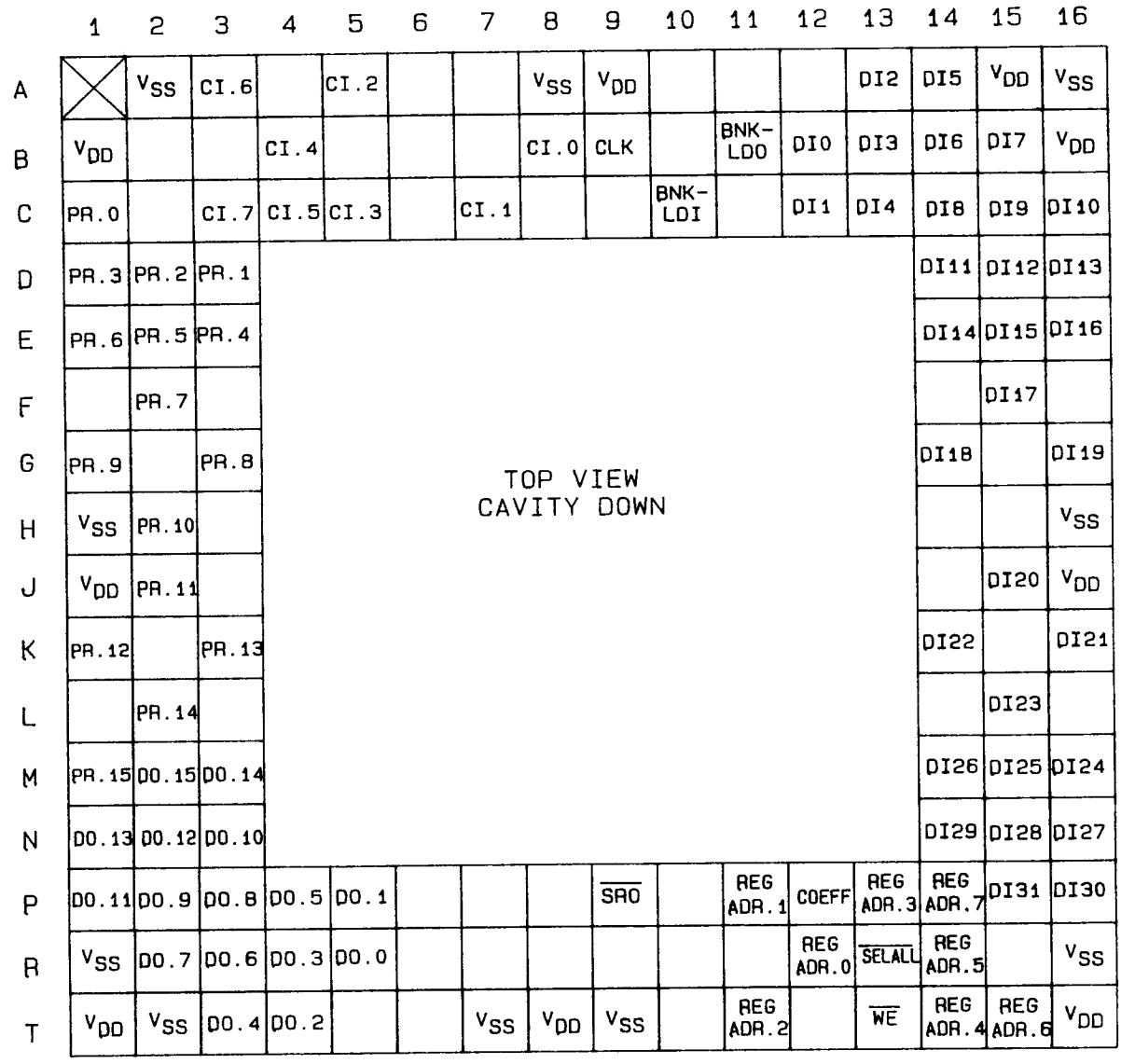


FIGURE 1. Terminal connections.

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Case outline Y

Device types 01 and 02

Terminal							
Number	Name	Number	Name	Number	Name	Number	Name
1	V_{DD}	34	CLK	67	V_{SS}	100	$\overline{SRO}$
2	V_{SS}	35	BNKLDI	68	V_{DD}	101	V_{SS}
3	PR.10	36	BNKLDO	69	DI20	102	V_{SS}
4	PR.9	37	V_{DD}	70	DI21	103	V_{DD}
5	PR.8	38	DI0	71	DI22	104	DO.0
6	PR.7	39	V_{SS}	72	DI23	105	V_{SS}
7	PR.6	40	DI1	73	DI24	106	DO.1
8	V_{DD}	41	N.C.	74	V_{DD}	107	DO.2
9	PR.5	42	DI2	75	DI25	108	DO.3
10	V_{SS}	43	V_{SS}	76	DI26	109	N.C.
11	PR.4	44	DI3	77	V_{SS}	110	DO.4
12	V_{SS}	45	DI4	78	DI27	111	V_{SS}
13	PR.3	46	V_{SS}	79	DI28	112	DO.5
14	PR.2	47	DI5	80	V_{SS}	113	DO.6
15	V_{SS}	48	DI6	81	DI29	114	DO.7
16	PR.1	49	DI7	82	DI30	115	N.C.
17	PR.0	50	V_{DD}	83	DI31	116	V_{DD}
18	V_{DD}	51	DI8	84	V_{DD}	117	DO.8
19	CI.7	52	DI9	85	REGADR.7	118	DO.9
20	V_{SS}	53	DI10	86	REGADR.6	119	V_{SS}
21	N.C.	54	DI11	87	V_{SS}	120	DO.10
22	CI.6	55	V_{SS}	88	REGADR.5	121	DO.11
23	V_{SS}	56	DI12	89	REGADR.4	122	DO.12
24	CI.5	57	V_{SS}	90	V_{SS}	123	DO.13
25	CI.4	58	DI13	91	REGADR.3	124	DO.14
26	V_{SS}	59	V_{SS}	92	SELALL	125	V_{SS}
27	CI.3	60	DI14	93	V_{SS}	126	DO.15
28	V_{DD}	61	DI15	94	$\overline{WE}$	127	V_{DD}
29	CI.2	62	V_{DD}	95	COEFF	128	PR.15
30	CI.1	63	DI16	96	V_{DD}	129	PR.14
31	CI.0	64	DI17	97	REGADR.0	130	PR.13
32	V_{DD}	65	DI18	98	REGADR.1	131	PR.12
33	V_{SS}	66	DI19	99	REGADR.2	132	PR.11

FIGURE 1. Terminal connections - Continued.

Cases X and Y

Device types 01 and 02

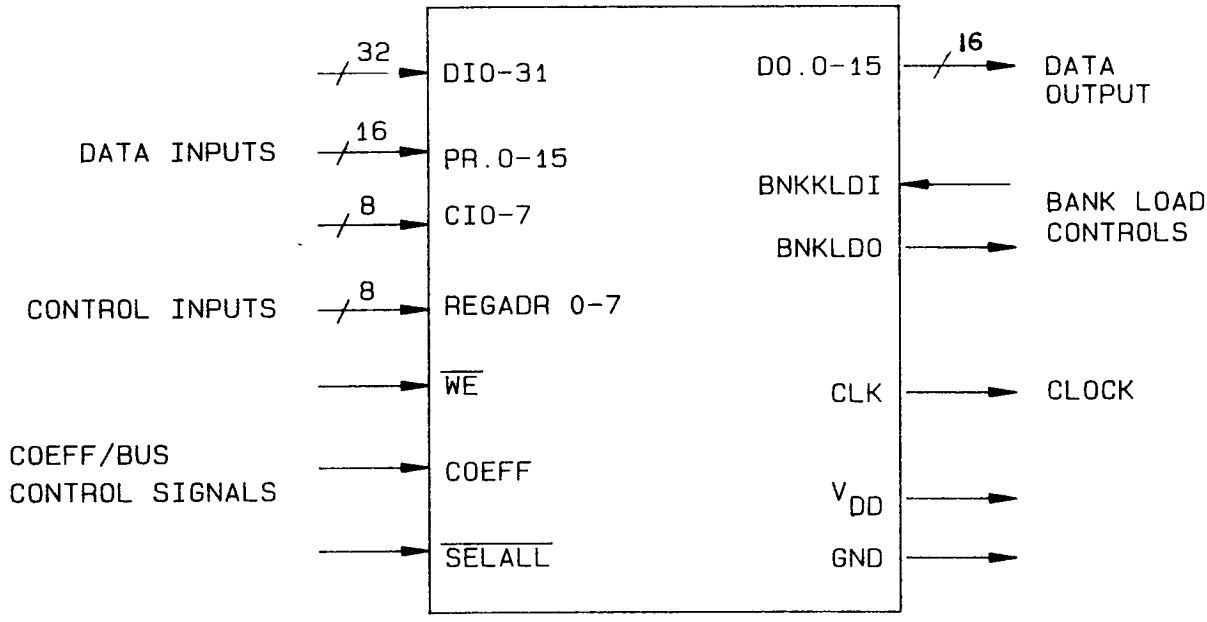
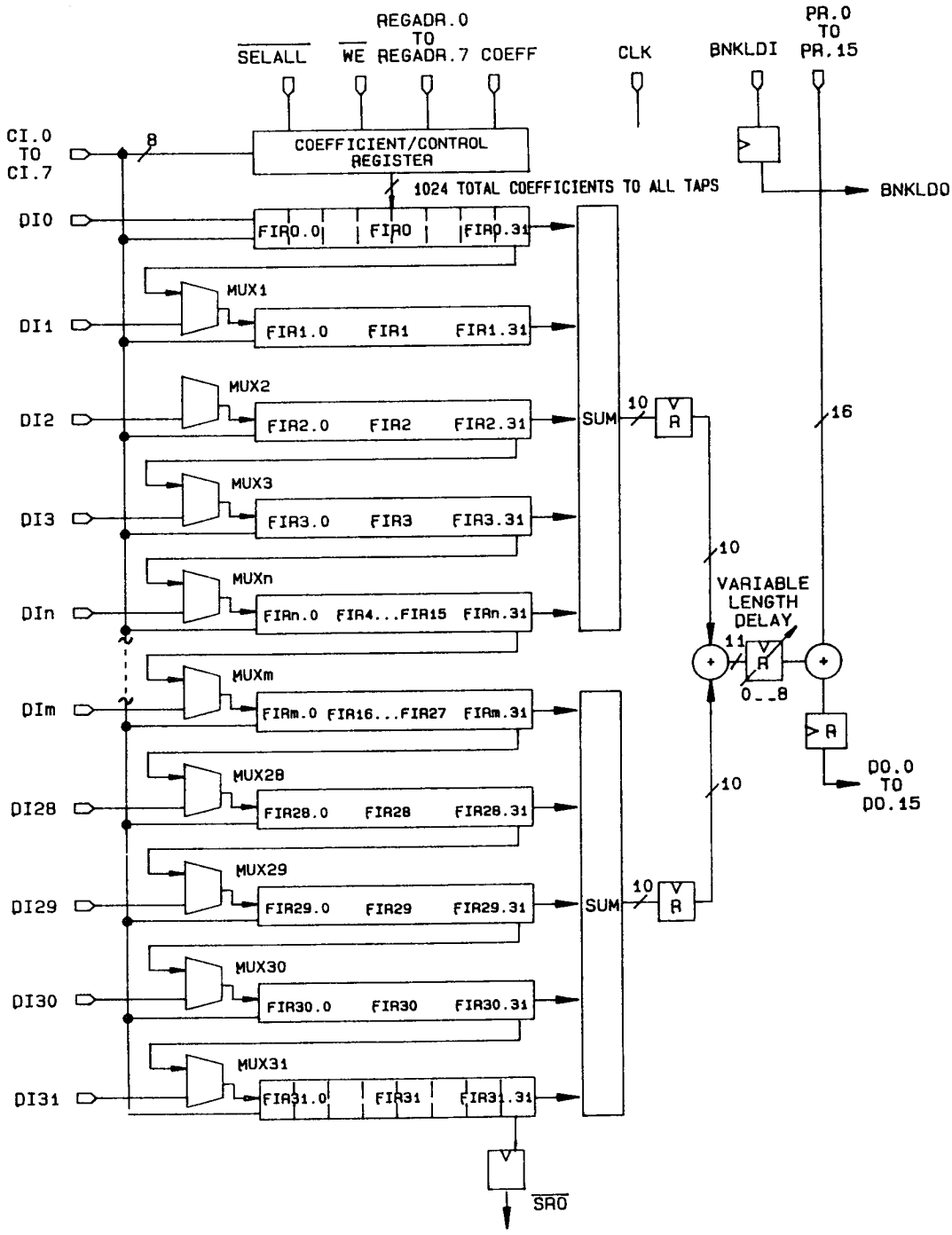


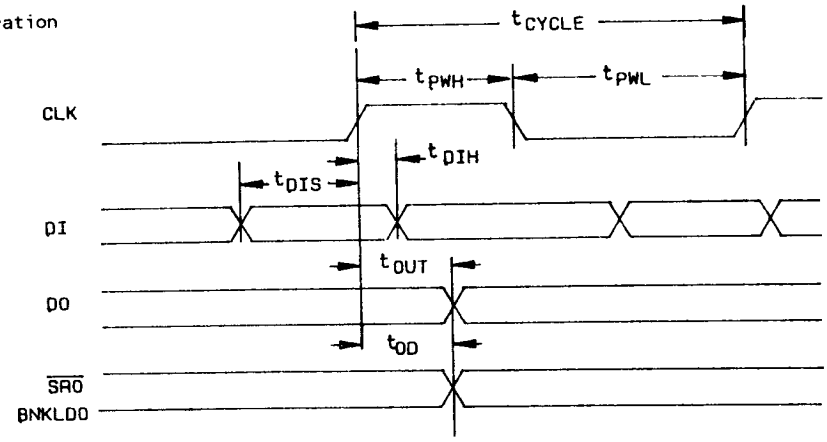
FIGURE 2. Block and logic diagrams.



NOTE: All 32 FIR filter banks contain 32 binary FIR filters.

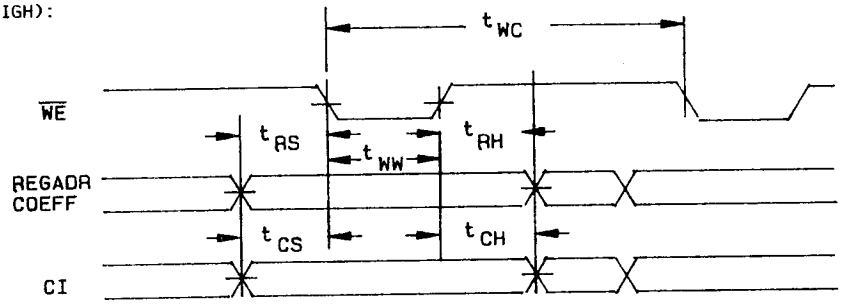
FIGURE 2. Block and logic diagrams - Continued.

Normal Filter Operation



Loading Controls into Master Section (Methods I, II, III)

Using $\overline{WE}$ ($\overline{SEALL}$ HIGH):



Using $\overline{SELALL}$ ($\overline{WE}$ HIGH):

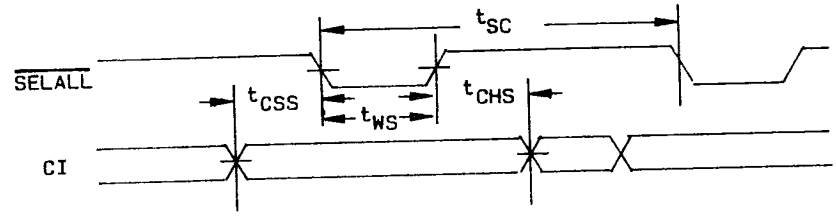
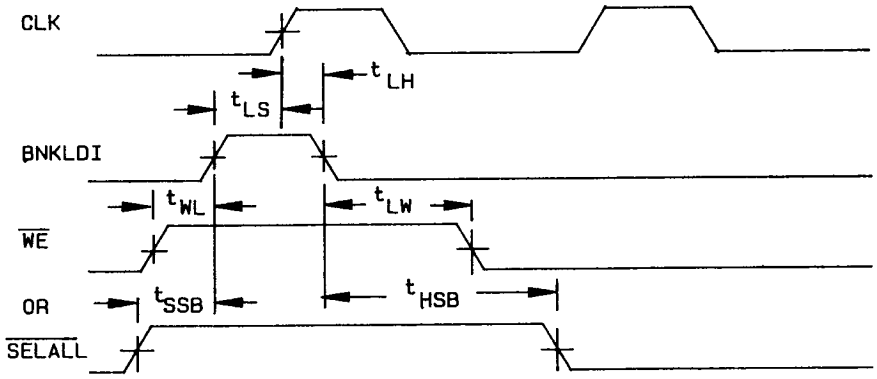
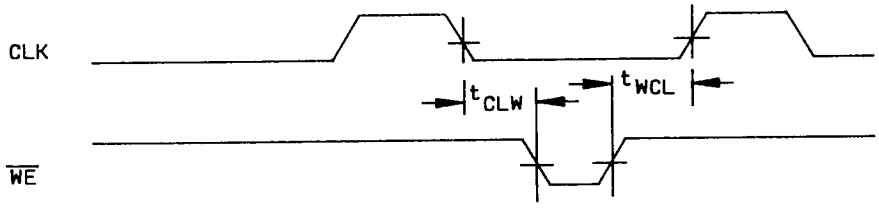


FIGURE 3. Timing waveforms.

Bank Loading of Controls-Synchronous
Transfer From Master to Slave Registers (Method I)



Synchronous Loading of Master and Synchronous
Transfer to Slave Section with $\overline{SELALL}$ HIGH (Method II)



NOTE: Minimum CLK cycle time, t_{CYCLE} = 80 ns.

Asynchronous Loading of Master Section and Asynchronous
Transfer to Slave Section with Bank Load HIGH (Method III)

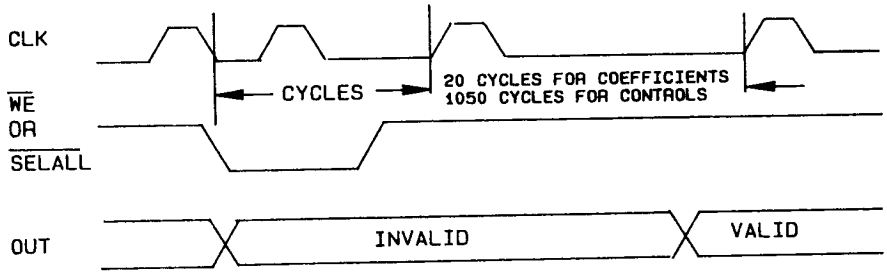


FIGURE 3. Timing waveforms - Continued.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN} and C_O measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all inputs and all input and output terminals tested.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)					
Final electrical parameters (see 4.2)	1/ 1,2,3,7, 8,9,10,11	2/ 1,2,3,7, 8,9,10,11	2/ 1,2,3,7, 8,9,10,11	1/ 1,2,3,7, 8,9,10,11	1/ 1,2,3,7, 8,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11
Group B end-point electrical parameters (see 4.4)			1,7,9		1,7,9
Group C end-point electrical parameters (see 4.4)	1,7,9	1,7,9		1,7,9	
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device classes M, B, and S. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
Reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hours at +125°C	100%
Radiographic	2012	100%

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IIA herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table IIA herein.

d. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes M, B, and S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.4 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.5 Symbols, definitions, and functional descriptions.

The logic symbol (see figure 2) defines the different pin groupings outlined in this section. The pin groups are: data inputs, data outputs, control inputs, bank load control, clock inputs and coeff/bus control signals. Figure 2 defines the pin assignments for this device. All inputs and outputs are TTL compatible.

6.5.1 Power and ground (V_{DD} and V_{SS} respectively). There are multiple V_{DD} and V_{SS} pins to distribute the power and ground requirements of the chip. These additional pins reduce noise due to typically high transient currents generated by the fast switching HCMOS output drivers. Standard TTL voltage levels can be applied (see table I).

6.5.2 Pin listing and description:

DI0 to DI31 32 single-bit data input pins. When the device is used as a 1-D processor, only pin DI0 is used. The remaining data input pins are left unconnected. When used as a 2-D filter processor with a 32 x 32 window, the device operates with all 32 data input pins active.

$\overline{SRO}$ Shift register output. In a 1-D configuration, $\overline{SRO}$ is the DI0 input delayed by 1025 cycles and inverted. Typically, this signal is connected to DI0 of the next device in a 1-D multiprocessor system. SRO is not used in 2-D processing.

CI.0 to CI.7 Coefficient/control input pins. A set of eight control bits or four sets of coefficients (both Ai, j and Bi, j) can be loaded into the master section of the coefficient/control registers.

$\overline{SELALL}$ Input signal. When LOW, $\overline{SELALL}$ enables the loading of the values at CI.0 to CI.7 into the master latches of all 256 4-tap groups in the processor simultaneously. This quickly initializes the processor. When HIGH, permists loading of those values into master latches at destinations determined by COEFF and REGADR.0 to REDADR.7.

BNKLDI Bank load input. Set HIGH to bank load coefficient/control inputs from master to slave registers. When asynchronously loading coefficients/controls with respect to CLK, BNKLDI is held LOW until bank loading occurs. When coefficient/control loading is synchronous to CLK, BNKLDI always held HIGH.

BNKLDO Bank load output. BNKLDI signal delayed by one CLK cycle. This may be used as BNKLDI for the next device in a 1-D multiprocessor system.

$\overline{WE}$ Active LOW write enable unit. Used to enable the loading of coefficients/control signals into the register location indicated by COEFF and REGADR.0 to REGADR.7.

COEFF Coefficient input indicator. When HIGH, specifies that data on the CI bus are coefficients. When LOW, data on the CI bus are control inputs.

REGADR.0 to REGADR.7 Coefficient/control register address inputs. Indicate the register location for coefficients or control signals. Loading occurs when WE is LOW. REGADR.7 is the MSB.

CLK Systems clock, positive edge triggered.

DO.0 to DO.15 16-bit data output. The value of the output is derived from the delayed sum of all the 1024 tapes and the partial result (PR.0 to PR.15). DO.15 is the MSB and DO.0 is the LSB.

PR.0 TO PR.15 16-bit partial result input. The partial results is summed with the processor results to provide the final data output value. During multiprocessor operation, the DO.0 to DO.15 outputs of the preceding processor are connected to the corresponding partial result input. When any PR pins are left unconnected, the processor assumes a LOW value. The partial results can also be used to vary the threshold when clipping the output to a single bit. PR.15 is the MSB and PR.0 is the LSB.

6.5.2.1 Pin description summary.

Signal	No. of pins	I/O	Description
DI0 - DI31	32	I	Data inputs 0 to 31
CI.0	8	I	Coefficient/control input bus
PR.0 - PR.15	16	I	Partial result input
DO.0 - DO.15	16	O	Filter output
CLK	1	I	System clock
BNKLDI	1	I	Bank loads
BNKDLO	1	O	BNKLD1 delayed by one clock cycle
$\overline{WE}$	1	I	Write enable for coefficient/control registers
REGADR.0 - REGADR.7	8	I	Address of coefficient/control registers
COEFF	1	I	Indicates if CI are coefficient or control inputs
$\overline{SELALL}$	1	I	Selects all coefficient registers

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.