Ordering Information

EM 48 1M 16 2 2 V T A – 6 L

EOREX Memory

EDO/FPM : 40
D-RAMBUS : 41
DDRSDRAM : 42
DDRSGRAM : 43
SGRAM : 46
SDRAM : 48

Density
16M : 16 Mega Bits
8M : 8 Mega Bits
4M : 4 Mega Bits
2M : 2 Mega Bits
1M : 1 Mega Bit

Organization
8 : x8
9 : x9
16 : x16
18 : x18
32 : x32

Refresh
1 : 1K, **8** : 8K
2 : 2K, **6** :16K
4 : 4K

Bank
2 : 2Bank **6** : 16Bank
4 : 4Bank **3** : 32Bank
8 : 8Bank

Interface
V: 3.3V
R: 2.5V

Package
C: CSP **B:** uBGA
T: TSOP **Q:** TQFP
P: PQFP (QFP)

Revision
A : 1st **B :** 2nd
C : 3rd **D :**4th

Min Cycle Time (Max Freq.)
-5 : 5ns (200MHz)
-6 : 6ns (167MHz)
-7 : 7ns (143MHz)
-75 : 7.5ns (133MHz)
-8 : 8ns (125MHz)
-10 : 10ns (100MHz)

Power
Blank : Standard
L : Low power
I : Industrial

F: PB free package

16Mb (2Banks) Synchronous DRAM

EM481M1622VTA (1Mx16)

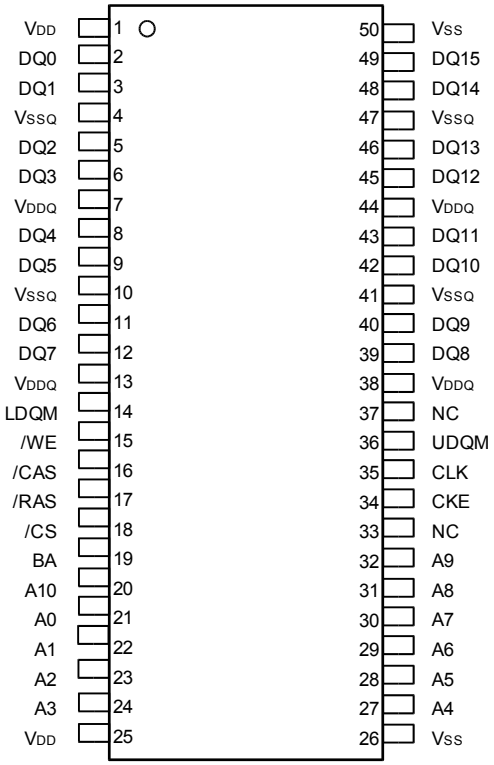
Description

The EM481M1622VTA is Synchronous Dynamic Random Access Memory (SDRAM) organized as 512K x 2 banks x 16 bits. All inputs and outputs are synchronized with the positive edge of the clock. The 16Mb SDRAM uses synchronized pipelined architecture to achieve high speed data transfer rates and is designed to operate at 3.3V low power memory system. It also provides auto refresh with power saving / down mode. All inputs and outputs voltage levels are compatible with LVTTL .

Feature

- Fully synchronous to positive clock edge
- Single 3.3V +/- 0.3V power supply
- LVTTL compatible with multiplexed address
- Programmable Burst Length (B/ L) - 1,2,4,8 or full page
- Programmable CAS Latency (C/ L) - 2 or 3
- Data Mask (DQM) for Read / Write masking
- Programmable wrap sequence - Sequential (B/ L = 1/2/4/8/full page)
  - Interleave (B/ L = 1/2/4/8)
- Burst read with single-bit write operation
- All inputs are sampled at the rising edge of the system clock.
- Auto refresh and self refresh
- 2,048 refresh cycles / 32ms

Pin Assignment (Top View)

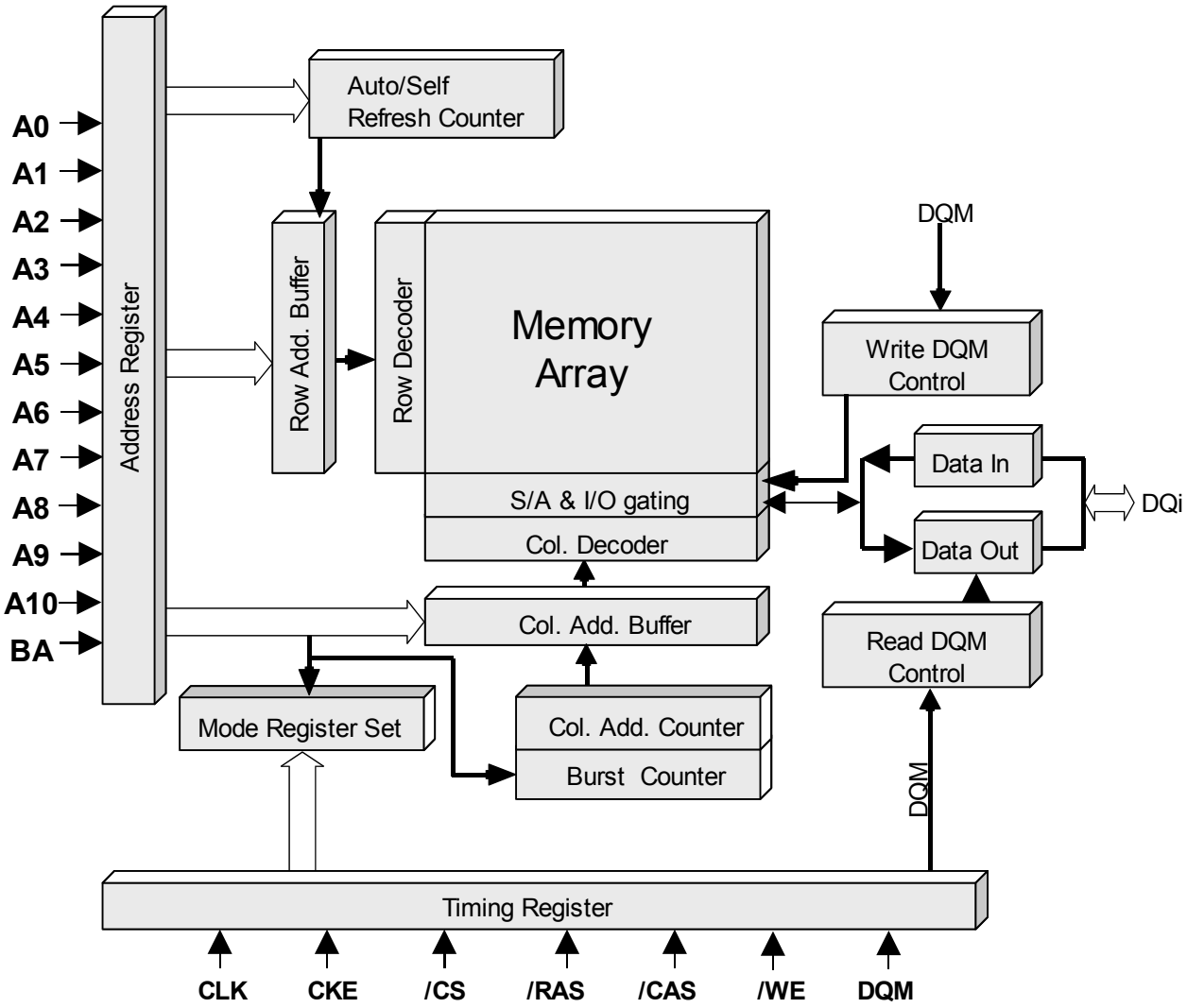


50pin TSOP-II

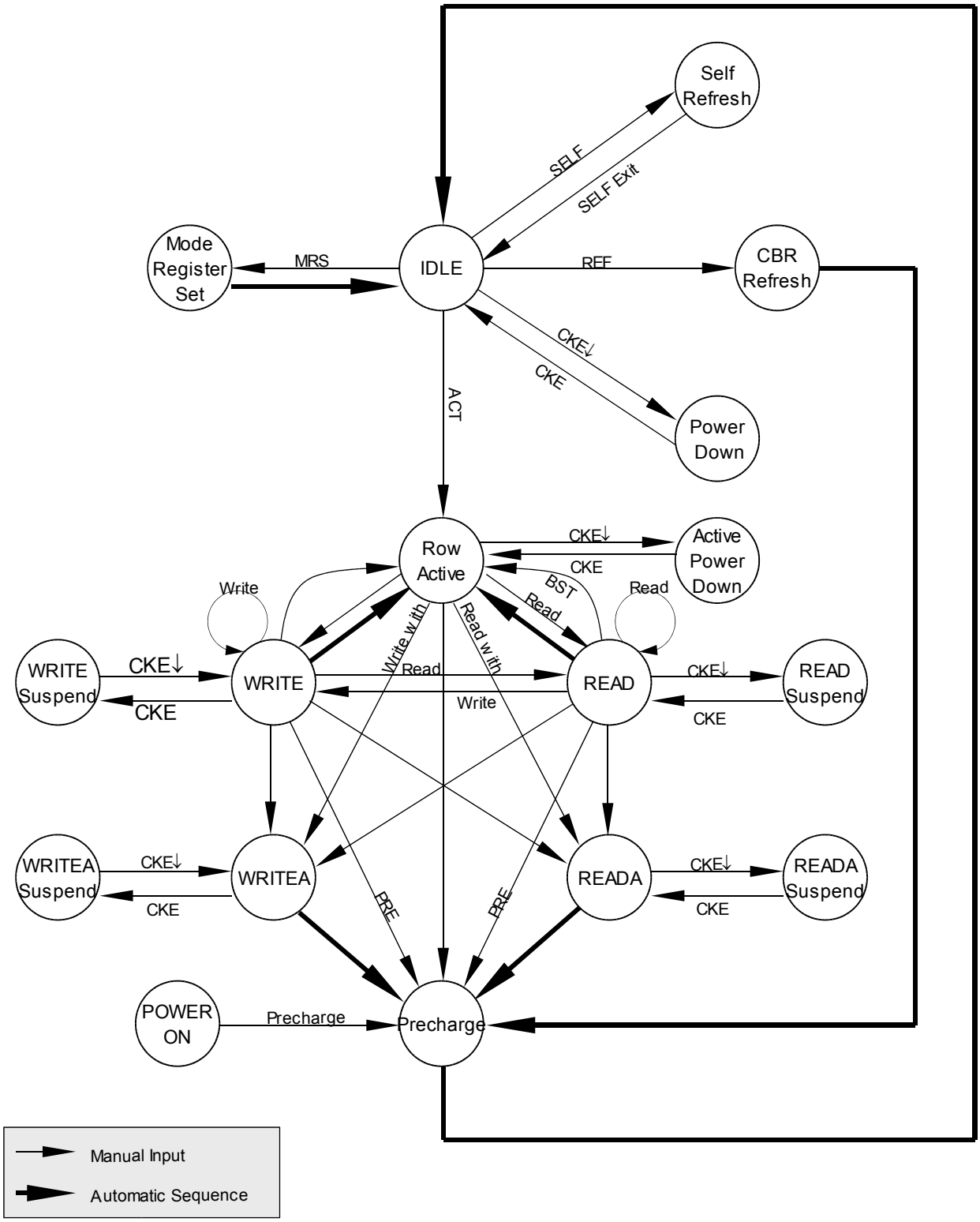
Pin Descriptions (Simplified)

Pin	Name	Pin Function
CLK	System Clock	Master Clock Input(Active on the Positive rising edge)
/CS	Chip select	Selects chip when active
CKE	Clock Enable	Activates the CLK when “H” and deactivates when “L”. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A10	Address	Row address (A0 to A10) is determined by A0 to A10 level at the bank active command cycle CLK rising edge. CA(CA0 to CA7) is determined by A0 to A7 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the pre-charge mode. When A10 = High at the pre-charge command cycle, all banks are pre-charged. But when A10 = Low at the pre-charge command cycle, only the bank that is selected by BA is pre-charged.
BA	Bank Address	Selects which bank is to be active.
/RAS	Row address strobe	Latches Row Addresses on the positive rising edge of the CLK with /RAS “L”. Enables row access & pre-charge.
/CAS	Column address strobe	Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access.
/WE	Write Enable	Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access.
UDQM /LDQM	Data input/output Mask	DQM controls I/O buffers.
DQ0 ~ 15	Data input/output	DQ pins have the same function as I/O pins on a conventional DRAM.
V_{DD}/V_{SS}	Power supply/Ground	V_{DD} and V_{SS} are power supply pins for internal circuits.
V_{DDQ}/V_{SSQ}	Power supply/Ground	V_{DDQ} and V_{SSQ} are power supply pins for the output buffers.
NC	No connection	This pin is recommended to be left No Connection on the device.

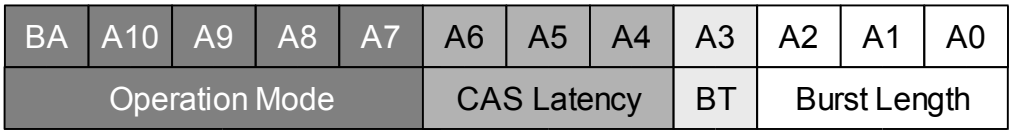
Block Diagram



Simplified State Diagram



Address Input for Mode Register Set



Burst Length				
Sequential	Interleave	A2	A1	A0
1	1	0	0	0
2	2	0	0	1
4	4	0	1	0
8	8	0	1	1
Reserved	Reserved	1	0	0
Reserved	Reserved	1	0	1
Reserved	Reserved	1	1	0
Full Page	Reserved	1	1	1

Burst Type	A3
Interleave	0
Sequential	1

CAS Latency	A6	A5	A4
Reserved	0	0	0
2	0	0	1
3	0	1	0
Reserved	0	1	1
Reserved	1	0	0
Reserved	1	0	1
Reserved	1	1	0
Reserved	1	1	1

BA	A10	A9	A8	A7	Operation Mode
0	0	0	0	0	Normal
0	0	1	0	0	Burst read with Single-bit Write

Burst Type (A3)

Burst Length	A2 A1 A0	Sequential Addressing	Interleave Addressing
2	X X 0	0 1	0 1
	X X 1	1 0	1 0
4	X 0 0	0 1 2 3	0 1 2 3
	X 0 1	1 2 3 0	1 0 3 2
	X 1 0	2 3 0 1	2 3 0 1
	X 1 1	3 0 1 2	3 2 1 0
8	0 0 0	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
	0 0 1	1 2 3 4 5 6 7 0	1 0 3 2 5 4 7 6
	0 1 0	2 3 4 5 6 7 0 1	2 3 0 1 6 7 4 5
	0 1 1	3 4 5 6 7 0 1 2	3 2 1 0 7 6 5 4
	1 0 0	4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
	1 0 1	5 6 7 0 1 2 3 4	5 4 7 6 1 0 3 2
	1 1 0	6 7 0 1 2 3 4 5	6 7 4 5 2 3 0 1
	1 1 1	7 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0
Full Page *	n n n	Cn Cn+1 Cn+2	-

* Page length is a function of I/O organization and column addressing

x16 (CA0 ~ CA7) : Full page = 256 bits

Truth Table

1. Command Truth Table

Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA	A10	A9~A0
		n-1	n							
Ignore Command	DESL	H	X	H	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X
Burst stop	BSTH	H	X	L	H	H	L	X	X	X
Read	READ	H	X	L	H	L	H	V	L	V
Read with auto pre-charge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with auto pre-charge	WRITA	H	X	L	L	H	H	V	H	V
Bank activate	ACT	H	X	L	L	H	H	V	V	V
Pre-charge select bank	PRE	H	X	L	L	H	L	V	L	X
Pre-charge all banks	PALL	H	X	L	L	H	L	X	H	X
Mode register set	MRS	H	X	L	L	L	L	L	L	V

Note : H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

2. DQM Truth Table

Command	Symbol	CKE		/CS
		n-1	n	
(EM481M1622VT)				
Data write / output enable	ENB	H	X	H
Data mask / output disable	MASK	H	X	L
(EM481M1622VT)				
Upper byte write enable / output enable	BSTH	H	X	L
Read	READ	H	X	L
Read with auto pre-charge	READA	H	X	L
Write	WRIT	H	X	L
Write with auto pre-charge	WRITA	H	X	L
Bank activate	ACT	H	X	L
Pre-charge select bank	PRE	H	X	L
Pre-charge all banks	PALL	H	X	L
Mode register set	MRS	H	X	L

Note : H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

3. CKE Truth Table

Command	Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	Addr.
			n-1	n					
Activating	Clock suspend mode entry		H	L	X	X	X	X	X
Any	Clock suspend mode		L	L	X	X	X	X	X
Clock suspend	Clock suspend mode exit		L	H	X	X	X	X	X
Idle	CBR refresh command	REF	H	H	L	L	L	H	X
Idle	Self refresh entry	SELF	H	L	L	L	L	H	X
Self refresh	Self refresh exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Idle	Power down entry		H	L	X	X	X	X	X
Power down	Power down exit		L	H	X	X	X	X	X

Remark H = High level, L = Low level, X = High or Low level (Don't care)

4. Operative Command Table

Current state	/CS	/R	/C	/W	Addr.	Command	Action	Notes
Idle	H	X	X	X	X	DESL	Nop or pow er dow n	2
	L	H	H	X	X	NOP or BST	Nop or pow er dow n	2
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA/RA	ACT	Row activating	
	L	L	H	L	BA, A10	PRE/PALL	Nop	
	L	L	L	H	X	REF/SELF	Refresh or self refresh	4
	L	L	L	L	Op-Code	MRS	Mode register accessing	
Row active	H	X	X	X	X	DESL	Nop	
	L	H	H	X	X	NOP or BST	Nop	
	L	H	L	H	BA/CA/A10	READ/READA	Begin read : Determine AP	5
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Begin w rite : Determine AP	5
	L	L	H	H	BA/RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Precharge	6
	L	L	L	H	X	REF/SELF	ILLEGAL	4
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Read	H	X	X	X	X	DESL	Continue burst to end → Row active	
	L	H	H	H	X	NOP	Continue burst to end → Row active	
	L	H	H	L	X	BST	Burst stop → Row active	
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst, new read : Determine AP	7
	L	L	L	L	BA/CA/A10	WRIT/WRITA	Terminate burst, start w rite : Determine AP	7, 8
	L	L	H	H	BA/RA	ACT	ILLEGAL	3
	L	L	H	L	BA/A10	PRE/PALL	Terminate burst, pre-charging	4
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write	H	X	X	X	X	DESL	Continue burst to end → Write recovering	
	L	H	H	H	X	NOP	Continue burst to end → Write recovering	
	L	H	H	L	X	BST	Burst stop → Row active	
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst, start read : Determine AP 7, 8	7,8
	L	L	L	L	BA/CA/A10	WRIT/WRITA	Terminate burst, new w rite : Determine AP 7	7
	L	L	H	H	BA/RA	ACT	ILLEGAL	3
	L	L	H	L	BA/A10	PRE/PALL	Terminate burst, pre-charging	9
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

Remark H = High level, L = Low level, X = High or Low level (Don't care)

Current state	/CS	/R	/C	/W	Addr.	Command	Action	Notes
Read with AP	H	X	X	X	X	DESL	Continue burst to end → Precharging	
	L	H	H	H	X	NOP	Continue burst to end → Precharging	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA/RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write with AP	H	X	X	X	X	DESL	burst to end → Write recovering with auto precharge	
	L	H	H	H	X	NOP	Continue burst to end → Write recovering with auto precharge	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA/RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Precharging	H	X	X	X	X	DESL	Nop → Enter idle after t_{RP}	
	L	H	H	H	X	NOP	Nop → Enter idle after t_{RP}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA/RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Nop → Enter idle after t_{RP}	
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Row activating	H	X	X	X	X	DESL	Nop → Enter idle after t_{RCD}	
	L	H	H	H	X	NOP	Nop → Enter idle after t_{RCD}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA/RA	ACT	ILLEGAL	3,10
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

Remark H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Precharge

Current state	/CS	/R	/C	/W	Addr.	Command	Action	Notes
Write recovering	H	X	X	X	X	DESL	Nop → Enter row active after t_{DPL}	
	L	H	H	H	X	NOP	Nop → Enter row active after t_{DPL}	
	L	H	H	L	X	BST	Nop → Enter row active after t_{DPL}	
	L	H	L	H	BA/CA/A10	READ/READA	Start read, Determine AP	
	L	H	L	L	BA/CA/A10	WRIT/WRITA	New write, Determine AP	8
	L	L	H	H	BA/RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write recovering with AP	H	X	X	X	X	DESL	Nop → Enter precharge after t_{DPL}	
	L	H	H	H	X	NOP	Nop → Enter precharge after t_{DPL}	
	L	H	H	L	X	BST	Nop → Enter precharge after t_{DPL}	
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL	3,8
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA/RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Refreshing	H	X	X	X	X	DESL	Nop → Enter idle after t_{RC}	
	L	H	H	X	X	NOP/ BST	Nop → Enter idle after t_{RC}	
	L	H	L	X	X	READ/WRIT	ILLEGAL	
	L	L	H	X	X	ACT/PRE/PALL	ILLEGAL	
	L	L	L	X	X	REF/SELF/MRS	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	DESL	Nop	
	L	H	H	H	X	NOP	Nop	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	X	X	READ/WRIT	ILLEGAL	
	L	L	X	X	X	ACT/PRE/PALL/ REF/SELF/MRS	ILLEGAL	

Remark H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Precharge

Notes 1. All entries assume that CKE was active (High level) during the preceding clock cycle.

2. If all banks are idle, and CKE is inactive (Low level), SDRAM will enter Power down mode. All input buffers except CKE will be disabled.

3. Illegal to bank in specified states;
→ Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.

4. If all banks are idle, and CKE is inactive (Low level), SDRAM will enter Self refresh mode. All input buffers except CKE will be disabled.

5. Illegal if t_{RCD} is not satisfied.

6. Illegal if t_{RAS} is not satisfied.

7. Must satisfy burst interrupt condition.

8. Must satisfy bus contention, bus turn around, and/or write recovery requirements.

9. Must mask preceding data which don't satisfy t_{DPL}.

10. Illegal if t_{RRD} is not satisfied.

5. Command Truth Table for CKE

Current state	CKE n-1	CKE n	/CS	/R	/C	/W	Addr.	Action	Notes
Self refresh	H	X	X	X	X	X	X	INVALID, CLK (n – 1) would exit self refresh	
	L	H	H	X	X	X	X	Self refresh recovery	
	L	H	L	H	H	X	X	Self refresh recovery	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	Maintain self refresh	
Self refresh recovery	H	H	H	X	X	X	X	Idle after t_{RC}	
	H	H	L	H	H	X	X	Idle after t_{RC}	
	H	H	L	H	L	X	X	ILLEGAL	
	H	H	L	L	X	X	X	ILLEGAL	
	H	L	H	X	X	X	X	ILLEGAL	
	H	L	L	H	H	X	X	ILLEGAL	
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	X	X	X	ILLEGAL	
Power down	H	X	X	X	X	X	X	INVALID, CLK(n-1) would exit power down	
	L	H	X	X	X	X	X	Exit power down → Idle	
	L	L	X	X	X	X	X	Maintain power down mode	
Both banks idle	H	H	H	X	X	X		Refer to operations in Operative Command Table	
	H	H	L	H	X	X		Refer to operations in Operative Command Table	
	H	H	L	L	H	X		Refer to operations in Operative Command Table	
	H	H	L	L	L	H	X	Refresh	
	H	H	L	L	L	L	Op-Code	Refer to operations in Operative Command Table	
	H	L	H	X	X	X		Refer to operations in Operative Command Table	
	H	L	L	H	X	X		Refer to operations in Operative Command Table	
	H	L	L	L	H	X		Refer to operations in Operative Command Table	
	H	L	L	L	L	H	X	Self refresh	1
	H	L	L	L	L	L	Op-Code	Refer to operations in Operative Command Table	
	L	X	X	X	X	X	X	Power down	1
Row active	H	X	X	X	X	X	X	Refer to operations in Operative Command Table	
	L	X	X	X	X	X	X	Power down	1
Any state other than listed above	H	H	X	X	X	X		Refer to operations in Operative Command Table	
	H	L	X	X	X	X	X	Begin clock suspend next cycle	2
	L	H	X	X	X	X	X	Exit clock suspend next cycle	
	L	L	X	X	X	X	X	Maintain clock suspend	

Remark : H = High level, L = Low level, X = High or Low level (Don't care)

Notes 1. Self refresh can be entered only from the both banks idle state.
Power down can be entered only from both banks idle or row active state.
2. Must be legal command as defined in Operative Command Table.

Absolute Maximum Ratings

Symbol	Item	Rating	Units
V_{IN}, V_{OUT}	Input, Output Voltage	-0.3 ~ 4.6	V
V_{DD}, V_{DDQ}	Power Supply Voltage	-0.3 ~ 4.6	V
T_{OP}	Operating Temperature	0 ~ 70	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C
P_D	Power Dissipation	1	W
I_{OS}	Short Circuit Current	50	mA

Note : Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operation Conditions (Ta = 0 ~ 70°C)

Symbol	Parameter	Min.	Typical	Max.	Units
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V_{DDQ}	Power Supply Voltage (for I/O Buffer)	3.0	3.3	3.6	V
V_{IH}	Input logic high voltage	2.0		V_{DD}+0.3	V
V_{IL}	Input logic low voltage	-0.3		0.8	V

Note : 1. All voltage referred to V_{SS}.
2. V_{IH} (max) = 5.6V for pulse width ≤ 3ns
3. V_{IL} (min) = -2.0V for pulse width ≤ 3ns

Capacitance (Vcc =3.3V, f = 1MHz, Ta = 25°C)

Symbol	Parameter	Min.	Max.	Units
C_{CLK}	Clock capacitance	2.5	4.0	pF
C_I	Input capacitance for CLK, CKE, Address, /CS, /RAS, /CAS, /WE, DQML,DQMU	2.5	5.0	pF
C_O	Input/Output capacitance	4.0	6.5	pF

Recommended DC Operating Conditions

(VDD = 3.3V +/- 0.3 V, Ta = 0 ~ 70 °C , Ta = -40 to 85°C for 6I)

Parameter	Symbol	Test condition		MAX 5	MAX 6/6I/6L	MAX 7/7L	Units	Notes
Operating current	I_{CC1}	Burst length = 1, $t_{RC} \geq t_{RC}$ (min), IOL = 0 mA, One bank active		100	90	80	mA	1
Precharge standby current in power down mode	I_{CC2P}	CKE ≤ V_{IL} (max.), t_{CK} = 15 ns		2 / 0.7*			mA	5
	I_{CC2PS}	CKE ≤ V_{IL} (max.), t_{CK} = ∞		2 / 0.7*			mA	5
Precharge standby current in non-power down mode	I_{CC2N}	CKE ≥ V_{IL} (min.), t_{CK} = 15 ns, /CS ≥ V_{IH} (min.) Input signals are changed one time during 30r		20			mA	
	I_{CC2NS}	CKE ≥ V_{IL} (min.), t_{CK} = ∞ Input signals are stable		8			mA	
Active standby current in power down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CK} = 15ns		5			mA	
	I_{CC3PS}	CKE ≤ V_{IL}(max), t_{CK} = ∞		5			mA	
Active standby current in non-power down mode	I_{CC3N}	CKE ≥ V_{IL}(min), t_{CK} = 15ns,/ CS ≥ V_{IH}(mi Input signals are changed one time duri 30ns		30			mA	
	I_{CC3NS}	CKE ≥ V_{IL}(min), t_{CK} = ∞ Input signals are stable		20			mA	
operating current (Burst mode)	I_{CC4}	t_{CCD} = 2CLKs , I_{OL} = 0 mA	CL=3	180	160	140	mA	2
			CL=2					
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min.)		130	120	110	mA	3
Self Refresh current	I_{CC6}	CKE ≤ 0.2V		2			mA	4
				0.3				5

Note : 1. ICC1 depends on output loading and cycle rates.
Specified values are obtained w ith the output open.
Input signals are changed only one time during tCK(min)
2. ICC4 depends on output loading and cycle rates.
Specified values are obtained w ith the output open.
Input signals are changed only one time during tCK(min)
3. Input signals are changed only one time during tCK(min)
4. Standard pow er version.
5. * Low pow er version.

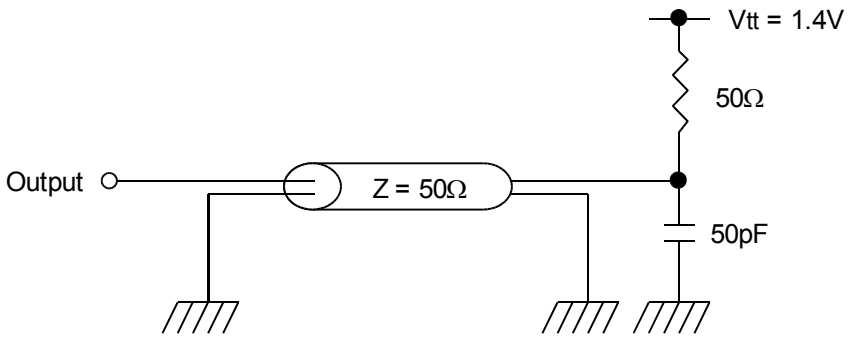
Recommended DC Operating Conditions (Continued)

Parameter	Symbol	Test condition	Min.	Max.	Unit
Input leakage current	I_{IL}	$0 \le V_I \le V_{DDQ}$, $V_{DDQ}=V_{DD}$ All other pins not under test=0 V	-0.5	+0.5	uA
Output leakage current	I_{OL}	$0 \le V_O \le V_{DDQ}$, DOUT is disabled	-0.5	+0.5	uA
High level output voltage	V_{OH}	Io = -4mA	2.4		V
Low level output voltage	V_{OL}	Io = +4mA		0.4	V

AC Operating Test Conditions

(VDD = 3.3V +/- 0.3 V, Ta = 0 ~ 70 °C , Ta = -40 to 85°C for 6I)

Output Reference Level	1.4V / 1.4V
Output Load	See diagram as below
Input Signal Level	2.4V / 0.4V
Transition Time of Input Signals	2ns
Input Reference Level	1.4V



Operating AC Characteristics

(VDD = 3.3V +/- 0.3 V, Ta = 0 ~ 70 °C , Ta = -40 to 85°C for 6I)

Parameter		Symbol	-5		-6/6I/6L		-7/7L		Units	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
Clock cycle time	CL = 3	tCK	5		6		7		ns	
	CL = 2		7		7.5		8		ns	
Access time from CLK	CL = 3	tAC		4.5		5		5.5	ns	
	CL = 2			5.5		5.5		5	ns	
CLK high level width		tCH	1.5		2		2		ns	
CLK low level width		tCL	1.5		2		2		ns	
Data-out hold time	CL = 3	tOH	1.5		2		2		ns	
	CL = 2						2		ns	
Data-out high impedance time	CL = 3	tHZ	1.5	5	2	6	2	7	ns	
	CL = 2								ns	
Data-out low impedance time		tLZ	0		0				ns	
Input hold time		tIH	1		1				ns	
Input setup time		tIS	1.5		1.5		1.5		ns	
ACTIVE to ACTIVE command period		tRC	54		60		65		ns	2
ACTIVE to PRECHARGE command period		tRAS	40	100k	42	100k	45	100k	ns	2
PRECHARGE to ACTIVE command period		tRP	18		18		18		ns	2
ACTIVE to READ/WRITE delay time		tRCD	14		18		20		ns	2
ACTIVE(one) to ACTIVE(another) command		tRRD	10		12		14		ns	2
READ/WRITE command to READ/WRITE command		tCCD	1		1		1		CLK	
Data-in to PRECHARGE command		tDPL	2		2		2		CLK	
Data-in to BURST stop command		tBDL	1		1		1		CLK	
Data-out to high impedance from PRECHARGE command	CL = 3	tROH	3		3		3		CLK	
	CL = 2						2		CLK	
Refresh time(2,048 cycle)		tREF		32		32		32	ms	

* All voltages referenced to Vss.

Note :

1. tHZ defines the time at which the output achieve the open circuit condition and is not referenced to output voltage levels.
2. These parameters account for the number of clock cycles and depend on the operating frequency of the clock, as follows :
   The number of clock cycles = Specified value of timing/clock period
   (Count fractions as a whole number)

Package Dimension