Elektronische Bauelemente

SSPS7331P

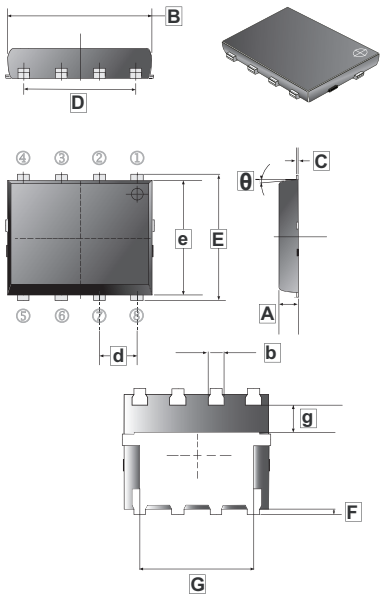
-13.4 A , -30 V , $R_{DS(ON)}$ 13 mΩ
P-Ch Enhancement Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are

DFN3x3-8PP



FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DFN3x3-8PP saves board space
- Fast switching speed
- High performance trench technology

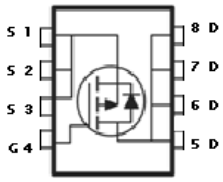
APPLICATION

DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PACKAGE INFORMATION

Package	MPQ	Leader Size
DFN3x3-8PP	3K	13 inch

Top View



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	0.70	0.90	θ	0°	12°
B	3.00BSC		b	0.20	0.40
C	0.10	0.25	d	0.65BSC	
D	1.80	2.3	e	3.00BSC	
E	3.2BSC		g	0.70(TYP.)	
F	0.01	0.02			
G	2.35BSC				

MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1]	T_A = 25℃	I_D	-13.4	A
	T_A = 70℃		-11	A
Pulsed Drain Current [2]		I_{DM}	-50	A
Continuous Source Current (Diode Conduction) [1]		I_S	-2.1	A
Total Power Dissipation [1]	T_A = 25℃	P_D	3.5	W
	T_A = 70℃		2.0	W
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55 ~ 150	℃
Thermal Resistance Ratings				
Thermal Resistance Junction-Ambient (Max.) [1]	t ≦ 10 sec	$R_{\theta JA}$	35	℃ / W
	Steady State		81	℃ / W

Notes:
1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	-1	-	-	V	V_{DS}=V_{GS}, I_D= -250μA
Gate-Body Leakage Current	I_{GSS}	-	-	±100	nA	V_{DS}=0, V_{GS}= ±25V
Zero Gate Voltage Drain Current	I_{DSS}	-	-	-1	μA	V_{DS}= -24V, V_{GS}=0
		-	-	-5		V_{DS}= -24V, V_{GS}=0, T_J=55℃
On-State Drain Current [1]	$I_{D(on)}$	-50	-	-	A	V_{DS}= -5V, V_{GS}= -10V
Drain-Source On-Resistance [1]	$R_{DS(ON)}$	-	-	13	mΩ	V_{GS}= -10V, I_D= -11.5A
		-	-	19		V_{GS}= -4.5V, I_D= -9.3A
Forward Transconductance [1]	g_{fs}	-	29	-	S	V_{DS}= -15V, I_D= -11.5A
Diode Forward Voltage	V_{SD}	-	-0.8	-	V	I_S=2.5A, V_{GS}=0
Dynamic [2]						
Total Gate Charge	Q_g	-	25	-	nC	V_{DS}= -15 V, V_{GS}= -5 V, I_D= -11.5 A
Gate-Source Charge	Q_{gs}	-	11	-		
Gate-Drain Charge	Q_{gd}	-	17	-		
Turn-On Delay Time	$T_{d(on)}$	-	15	-	nS	V_{DD}= -15V I_D= -1A V_{GEN}= -10V R_L=6Ω
Rise Time	T_r	-	13	-		
Turn-Off Delay Time	$T_{d(off)}$	-	100	-		
Fall Time	T_f	-	54	-		

Notes:
1. Pulse test：PW ≦ 300μs duty cycle ≦ 2%.
2. Guaranteed by design, not subject to production testing.

CHARACTERISTIC CURVE

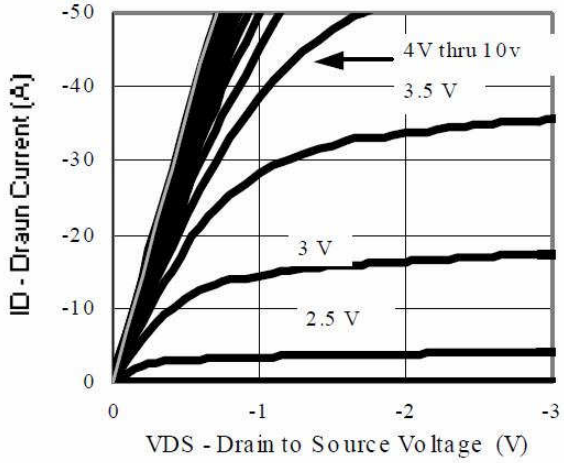


Figure 1. On-Region Characteristics

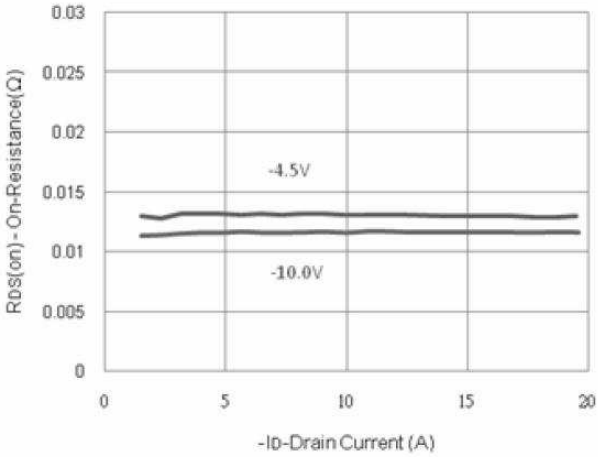


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

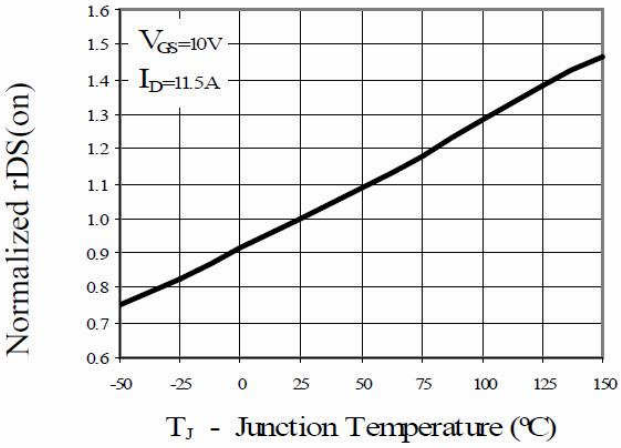


Figure 3. On-Resistance Variation with Temperature

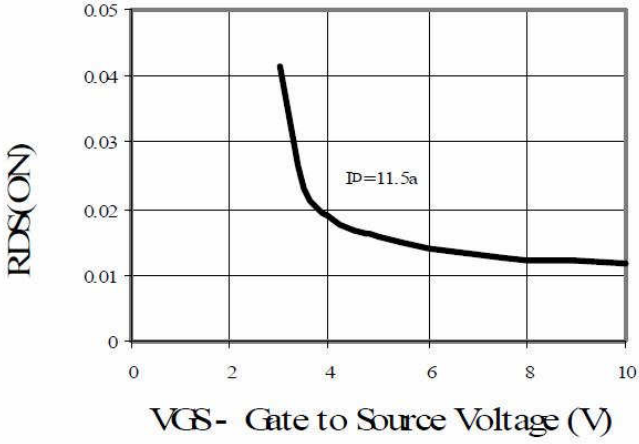


Figure 4. On-Resistance with Gate to Source Voltage

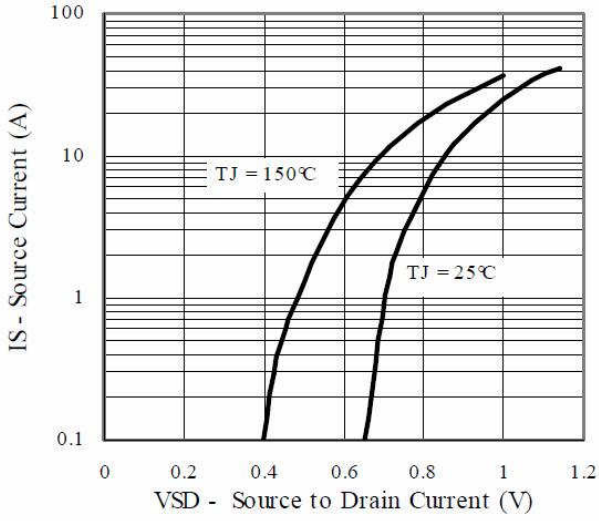


Figure 5. Transfer Characteristics

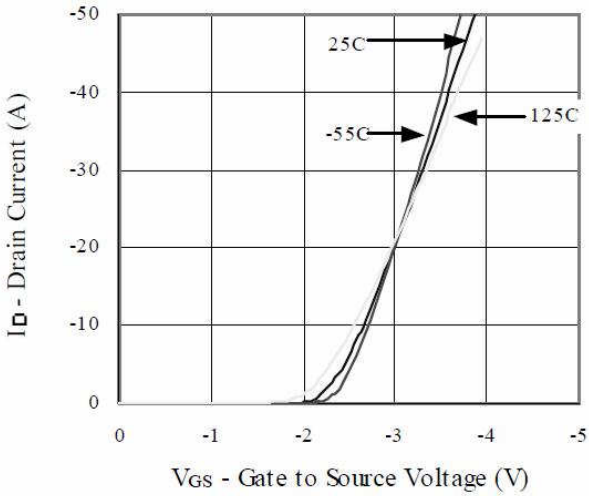


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

CHARACTERISTIC CURVE

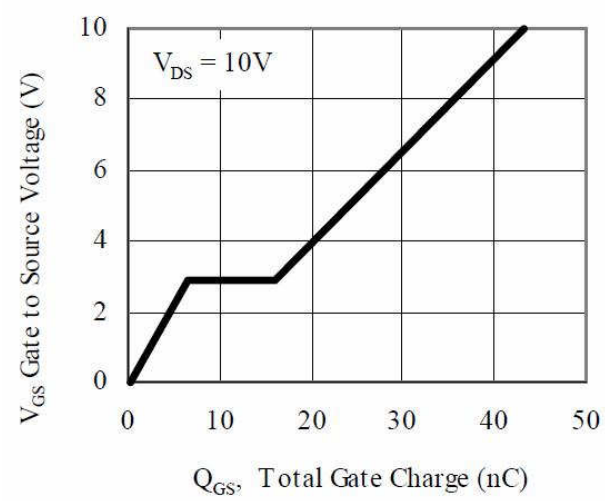


Figure 7. Gate Charge Characteristics

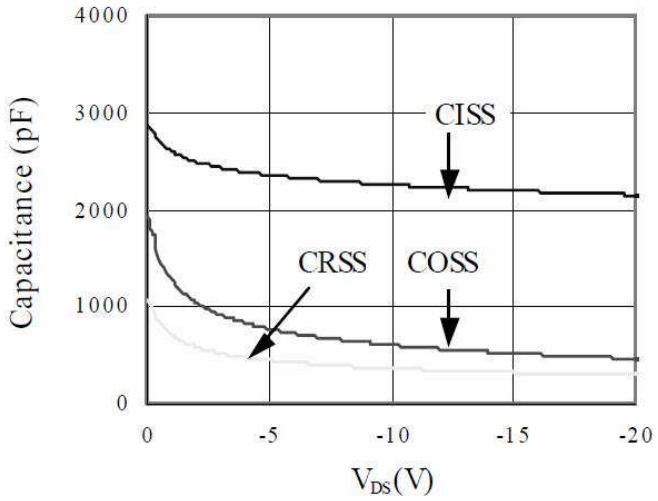


Figure 8. Capacitance Characteristics

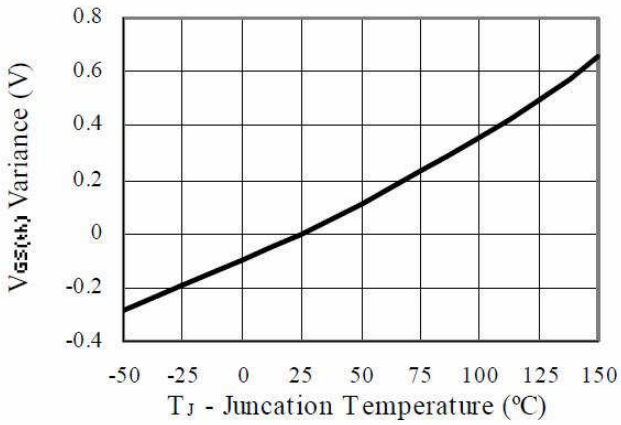


Figure 9. Maximum Safe Operating Area

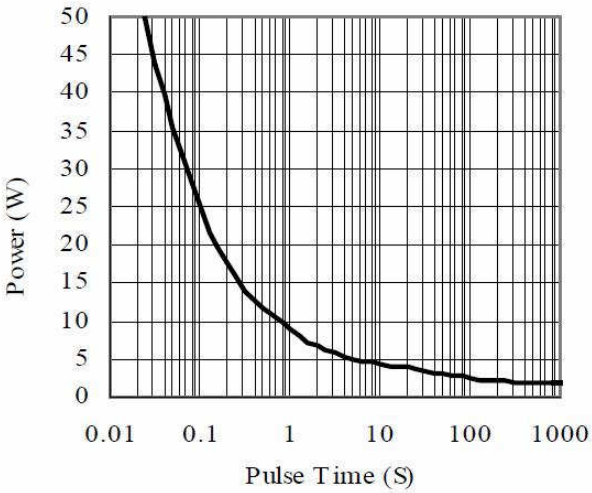


Figure 10. Single Pulse Maximum Power Dissipation

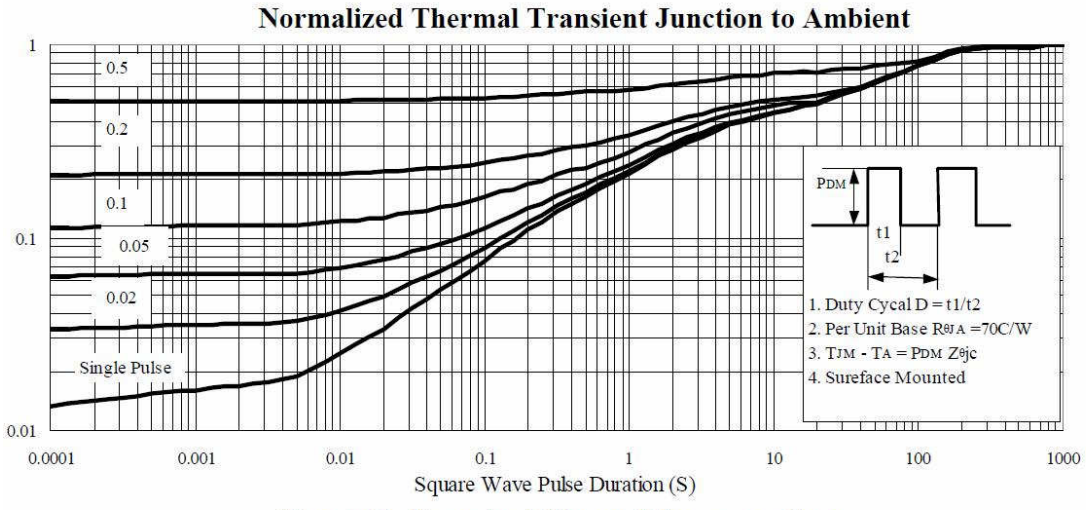


Figure 11. Transient Thermal Response Curve