Shantou Huashan Electronic Devices Co.,Ltd.

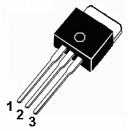
N-Channel MOSFET

HFU2N60

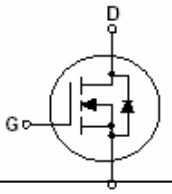
APPLICATIONSL

High-Speed Switching.

TO-251



1—G
2—D
3—S



ABSOLUTE MAXIMUM RATINGS (T_a=25℃)

T_{stg}——Storage Temperature·····-55~150℃

T_j ——Operating Junction Temperature ·····150℃

P_D —— Allowable Power Dissipation (T_c=25℃) ·····44W

V_{DSS} —— Drain-Source Voltage ····· 600V

V_{GSS} —— Gate-Source Voltage ·····±30V

I_D —— Drain Current(T_c=25℃)·····1.8A

ELECTRICAL CHARACTERISTICS (T_a=25℃)

Symbol	Characteristics	Min	Typ	Max	Unit	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	600			V	I_D=250μA ,V_{GS}=0V
I_{DSS}	Zero Gate Voltage Drain Current			10	μA	V_{DS} =600V， V_{GS}=0
I_{GSS}	Gate –Source Leakage Current			±100	nA	V_{GS}=±30V , V_{DS} =0V
$V_{GS(th)}$	Gate Threshold Voltage	2.5		4.5	V	V_{DS} = V_{GS} , I_D =250μA
$R_{DS(on)}$	Static Drain-Source On-Resistance		3.8	5.0	Ω	V_{GS}=10V, I_D =1.0A
gfs	Forward Transconductance		2.05		S	V_{DS} = 40V , I_D =1.0A *
Ciss	Input Capacitance		180	235	pF	V_{DS} =25V, V_{GS}=0,f=1MHz
Coss	Output Capacitance		20	25	pF	
Crss	Reverse Transfer Capacitance		4.3	3	pF	
$t_{d(on)}$	Turn - On Delay Time		9	28	nS	V_{DD} =300V, I_D =2A R_G= 25 Ω *
tr	Rise Time		25	60	nS	
$t_{d(off)}$	Turn - Off Delay Time		24	58	nS	
t_f	Fall Time		28	66	nS	
Qg	Total Gate Charge		8.5	12	nC	V_{DS} =480V V_{GS}=10V I_D=2A *
Qgs	Gate–Source Charge		1.3		nC	
Qgd	Gate–Drain Charge		4.1		nC	
Is	Continuous Source Current			1.8	A	
V_{SD}	Diode Forward Voltage			1.4	V	I_S =1.8A , V_{GS}=0
Rth(j-c)	Thermal Resistance, Junction-to-Case			2.87	℃/W	

*Pulse Test：Pulse Width≤300μs， Duty Cycle≤2%

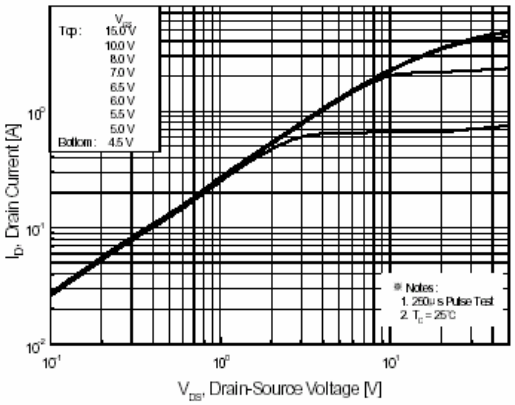


Figure 1. On-Region Characteristics

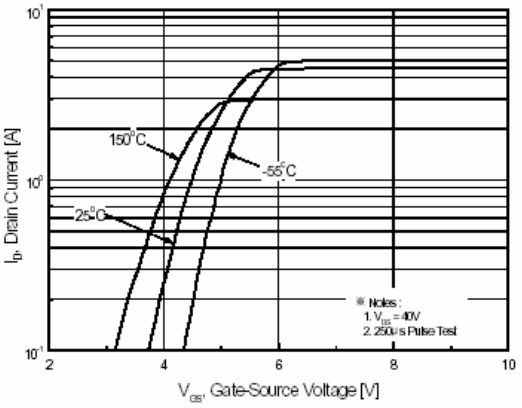


Figure 2. Transfer Characteristics

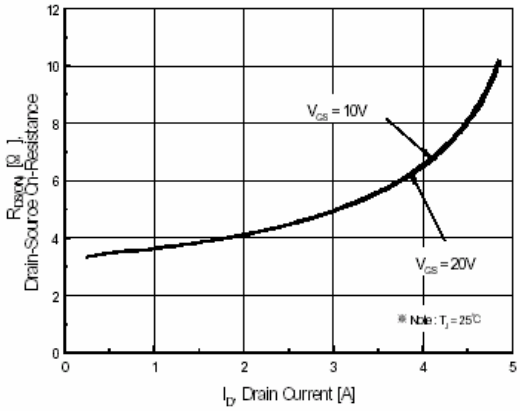


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

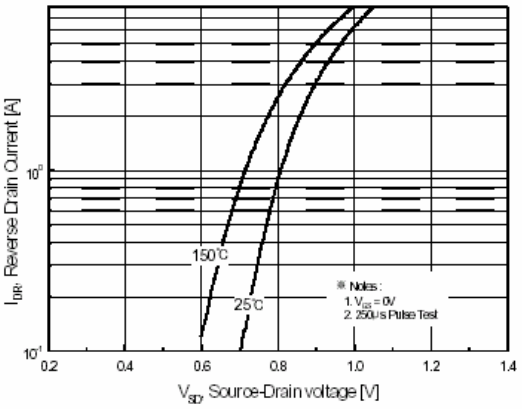


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

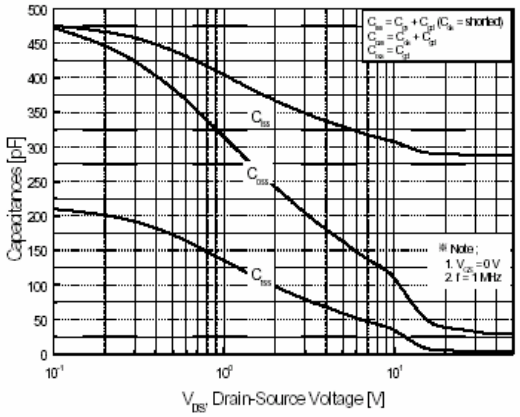


Figure 5. Capacitance Characteristics

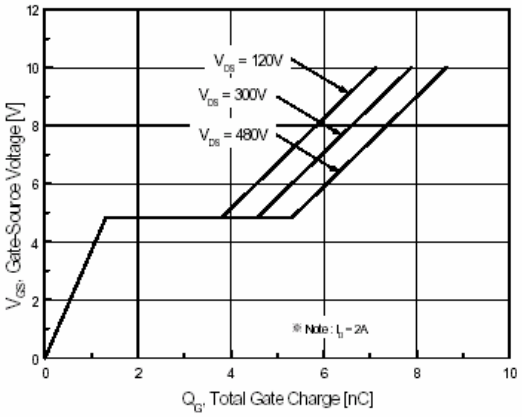


Figure 6. Gate Charge Characteristics

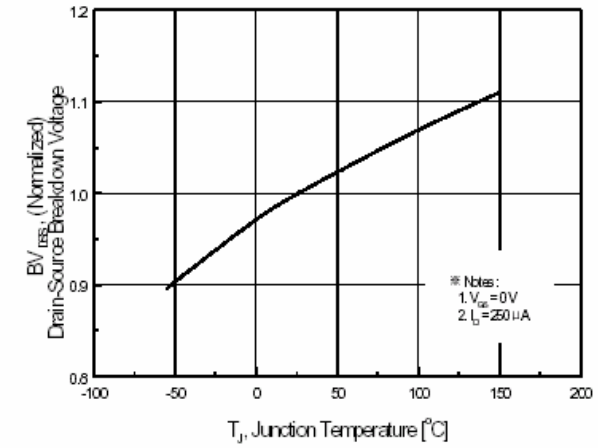


Figure 7. Breakdown Voltage Variation vs Temperature

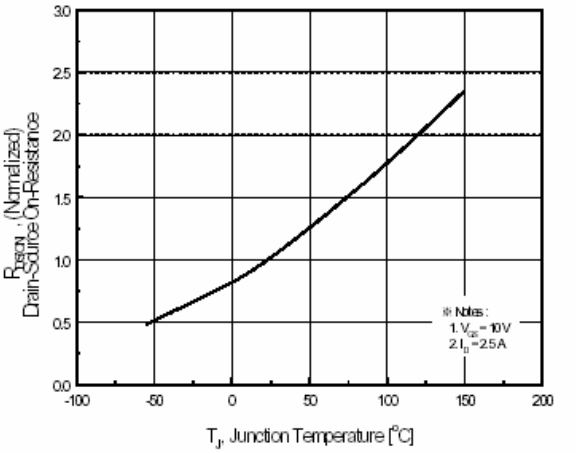


Figure 8. On-Resistance Variation vs Temperature

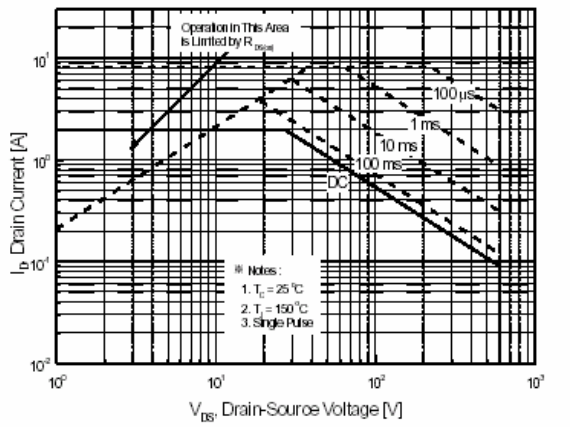


Figure 9-1. Maximum Safe Operating Area for HFU2N60

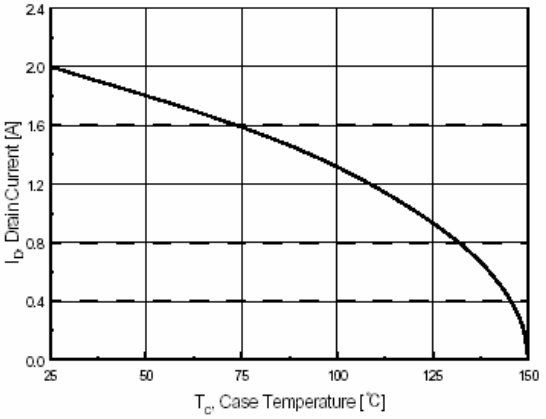


Figure 10. Maximum Drain Current vs Case Temperature

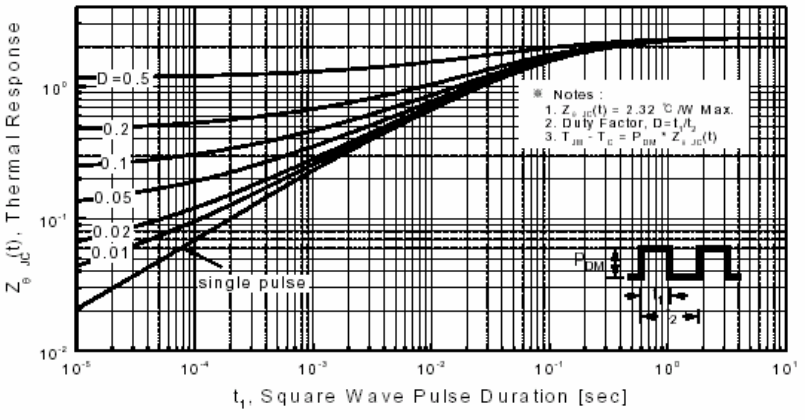
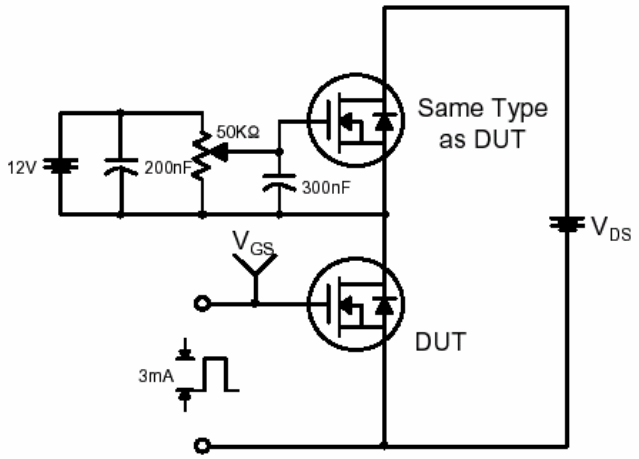
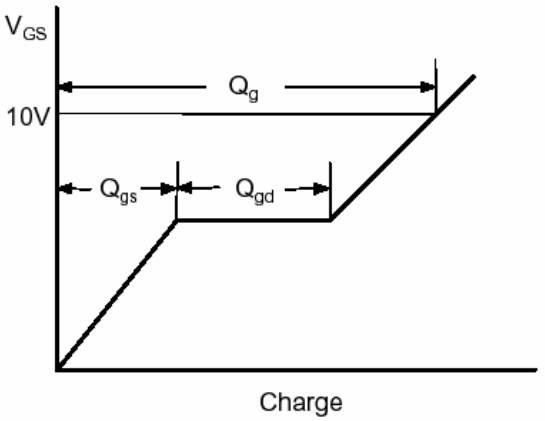


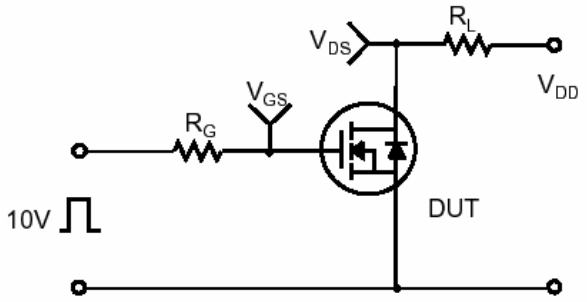
Figure 11-1. Transient Thermal Response Curve for HFU2N60

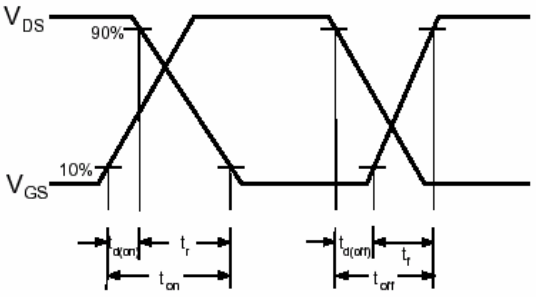
Gate Charge Test Circuit & Waveform



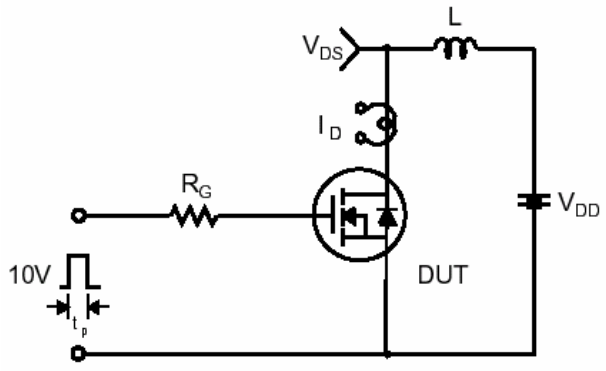


Resistive Switching Test Circuit & Waveforms

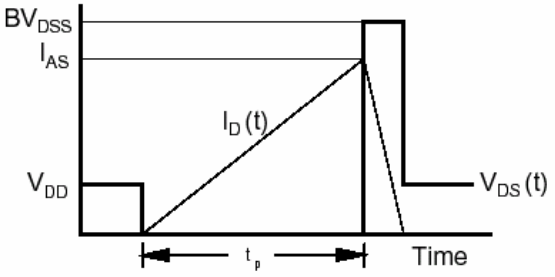




Unclamped Inductive Switching Test Circuit & Waveforms



$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



Peak Diode Recovery dv/dt Test Circuit & Waveforms