REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes to table I. Clarification made in figure 1. Technical changes to table IIA. Replaced pin description in section 6.7. Editorial changes throughout.	93-02-24	M.L. Poelking

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV		A			A	A	A													
SHEET	15	16	17	18	19	20	21													

REV STATUS OF SHEETS	REV	A				A	A			A	A				
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
92-09-04

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, MANCHESTER ENCODER/DECODER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-90549
A	67268	

SHEET 1 OF 21

DESC FORM 193
JUL 91

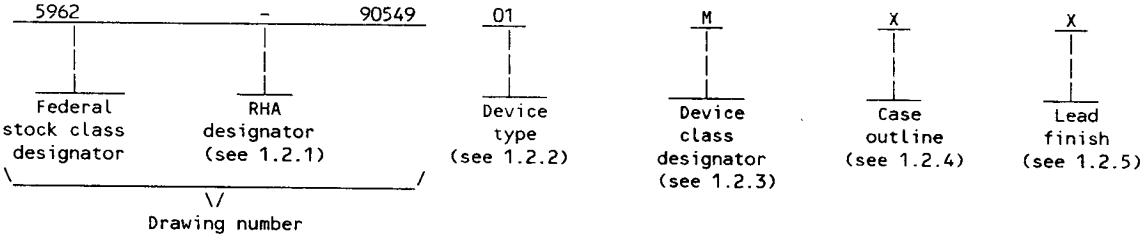
5962-E036-93

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	
01	HD1-15531	Manchester encoder/decoder	1.25 megabit/s
02	HD1-15531B	Manchester encoder/decoder	2.50 megabit/s

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage	7.0 V dc
Input, output or I/O voltage applied	GND - 0.5 V dc to V_{CC} + 0.5 V dc
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Power dissipation (P_D)	1.44 W
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (Θ_{JA})	34.8°C/W

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Encoder/decoder clock rise time (t_{ECR}, t_{DCR})	8.0 ns max
Encoder/decoder clock fall time (t_{ECF}, t_{DCF})	8.0 ns max
Sync transition span (t_{D2})	18 t_{DC} 2/
Short data transition span (t_{D4})	6.0 t_{DC} 2/
Long data transition span (t_{D5})	12 t_{DC} 2/
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Logic testing for device classes Q or V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	xx percent 3/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1553 - Aircraft Internal Time Division Command/Response Multiplex Data Bus.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ t_{DC} = decoder clock period = $1/f_{DC}$.
3/ Values will be added when they become available.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3 3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.8.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.8.2 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturers, except when Delta's are required.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}	V_{CC} = 4.5 V and 5.5 V	1,2,3	All		$0.2(V_{CC})$	V
Input high voltage	V_{IH}	V_{CC} = 4.5 V and 5.5 V	1,2,3	All	$0.7(V_{CC})$		V
Input low clock voltage	V_{ILC}	V_{CC} = 4.5 V and 5.5 V	1,2,3	All		GND +0.5	V
Input high clock voltage	V_{IHC}	V_{CC} = 4.5 V and 5.5 V	1,2,3	All	V_{CC} -0.5		V
Output low voltage	V_{OL}	I_{OL} = 1.8 mA, V_{CC} = 4.5 V 2/	1,2,3	All		0.4	V
Output high voltage	V_{OH}	I_{OH} = -3.0 mA, V_{CC} = 4.5 V 2/	1,2,3	All	2.4		V
Input leakage current	I_I	V_I = GND; V_{CC} = 5.5 V	1,2,3	All	-1.0	0	µA
		$V_I = V_{CC}$			0	+1.0	
Operating power supply current	I_{CCOP}	V_{CC} = 5.5 V, f = 1.0 MHz 5/	1,2,3	All		10	mA
Standby supply current	I_{CCSB}	$V_{IN} = V_{CC}$ = 5.5 V, output open	1,2,3	All		2.0	mA
Input capacitance	C_I	All measurements referenced to device ground, V_{CC} = open, f = 1.0 MHz, see 4.4.1b	4	All		25	pF
Input/output capacitance	$C_{I/O}$		4	All		25	pF
Functional test 3/	FT	f = 15 MHz, C_L = 50 pF, V_{CC} = 4.5 V and 5.5 V V_{IH} = .70 V_{CC}, V_{IL} = .20 V_{CC} $V_{IHC} = V_{CC}$ + -0.5 V $V_{ILC} = V_{CC}$ 0.5 V see 4.4.1c	7,8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ENCODER TIMING							
Encoder clock frequency	f_{EC}	V_{CC} = 4.5 V and 5.5 V, V_{IH} = 70 percent V_{CC}, V_{IL} = 20 percent V_{CC}, C_L = 50 pF, see figures 3 and 4	9,10,11	01		15	MHz
				02		30	
Send clock frequency	f_{ESC}		9,10,11	01		2.5	MHz
			9,10,11	02		5.0	
Encoder data rate	f_{ED}		9,10,11	01		1.25	MHz
			9,10,11	02		2.50	
Master reset pulse width	t_{MR}		9,10,11	All	150		ns
Shift clock delay	t_{E1}		9,10,11	01		125	ns
			9,10,11	02		80	
Serial data setup	t_{E2}		9,10,11	01	75		ns
			9,10,11	02	50		
Serial data hold	t_{E3}		9,10,11	01	75		ns
			9,10,11	02	50		
Enable setup	t_{E4}		9,10,11	All	90		ns
Enable pulse width	t_{E5}		9,10,11	All	100		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ENCODER TIMING - Continued							
Sync setup	t_{E6}	V_{CC} = 4.5 V and 5.5 V, V_{IH} = 70 percent V_{CC}, V_{IL} = 20 percent V_{CC}, C_L = 50 pF, see figures 3 and 4	9,10,11	All	55		ns
Sync pulse width	t_{E7}		9,10,11	All	150		ns
Send data delay	t_{E8}		9,10,11	All	0	50	ns
Bipolar output delay	t_{E9}		9,10,11	All		130	ns
Enable hold	t_{E10}		9,10,11	All	10		ns
Sync hold	t_{E11}		9,10,11	All	95		ns
DECODER TIMING							
Decoder clock frequency	f_{DC}	V_{CC} = 4.5 V and 5.5 V, V_{IH} = 70 percent V_{CC}, V_{IL} = 20 percent V_{CC}, C_L = 50 pF, see figures 3 and 4	9,10,11	01		15	MHz
			9,10,11	02		30	
Decoder sync clock	f_{DS}		9,10,11	01		2.5	MHz
			9,10,11	02		5.0	
Decoder data rate	f_{DD}		9,10,11	01		1.25	MHz
			9,10,11	02		2.50	
Decoder reset pulse width	t_{DR}		9,10,11	All	150		ns
Decoder reset setup time	t_{DRS}		9,10,11	All	75		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DECODER TIMING - Continued							
Decoder reset hold time	t_{DRH}	V_{CC} = 4.5 V and 5.5 V, V_{IH} = 70 percent V_{CC}, V_{IL} = 20 percent V_{CC} C_L = 50 pF, see figures 3 and 4	9,10,11	All	75		ns
Master reset pulse	t_{MR}		9,10,11	All	150		ns
Bipolar data pulse width	t_{D1}		9,10,11	All	TDC +10 4/		ns
One zero overlap	t_{D3}		9,10,11	All		TDC -10 4/	ns
Sync delay (ON)	t_{D6}		9,10,11	All	-20	110	ns
Take data delay (ON)	t_{D7}		9,10,11	All	0	110	ns
Serial data out delay	t_{D8}		9,10,11	All		80	ns
Sync delay (OFF)	t_{D9}		9,10,11	All	0	110	ns
Take data delay (OFF)	t_{D10}		9,10,11	All	0	110	ns
Valid word delay	t_{D11}		9,10,11	All	0	110	ns
Sync clock to shift clock delay	t_{D12}		9,10,11	All		75	ns
Sync data setup	t_{D13}		9,10,11	All	75		ns

1/ All test to be performed using worst-case test conditions, unless otherwise specified.
2/ Interchanging of force and sense conditions is permitted.
3/ Functional tests performed to verify functionality of device as a Manchester encoder/decoder as defined by MIL-STD-1553.
4/ TDC = Decoder Clock Period = $1/f_{DC}$.
5/ Guaranteed if not tested to the table I requirements.

Device type	All	Device type	All
Case outline	Q	Case outline	Q
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{CC}	21	GND
2	VALID WORD	22	MASTER RESET
3	TAKE DATA'	23	COUNT C2
4	TAKE DATA	24	DIVIDE BY 6 OUT
5	SERIAL DATA OUT	25	BIPOLAR ZERO OUT
6	SYNCHR DATA	26	OUTPUT INHIBIT
7	SYNCHR DATA SEL	27	BIPOLAR ONE OUT
8	SYNCHR CLK	28	SERIAL DATA IN
9	DECODER CLK	29	ENCODER ENABLE
10	SYNCHR CLK SEL	30	SYNC SEL
11	BIPOLAR ZERO IN	31	ENCODER PARITY SEL
12	BIPOLAR ONE IN	32	SEND DATA
13	UNIPOLAR DATA IN	33	SEND CLK IN
14	DECODER SHIFT CLK	34	ENCODER SHIFT CLK
15	TRANSITION SEL	35	NC
16	NC	36	COUNT C_3
17	COMMAND SYNC	37	ENCODER CLK
18	DECODER PARITY SEL	38	DATA SYNC
19	DECODER RESET	39	COUNT C_4
20	COUNT C_0	40	COUNT C_1

FIGURE 1. Terminal connections.

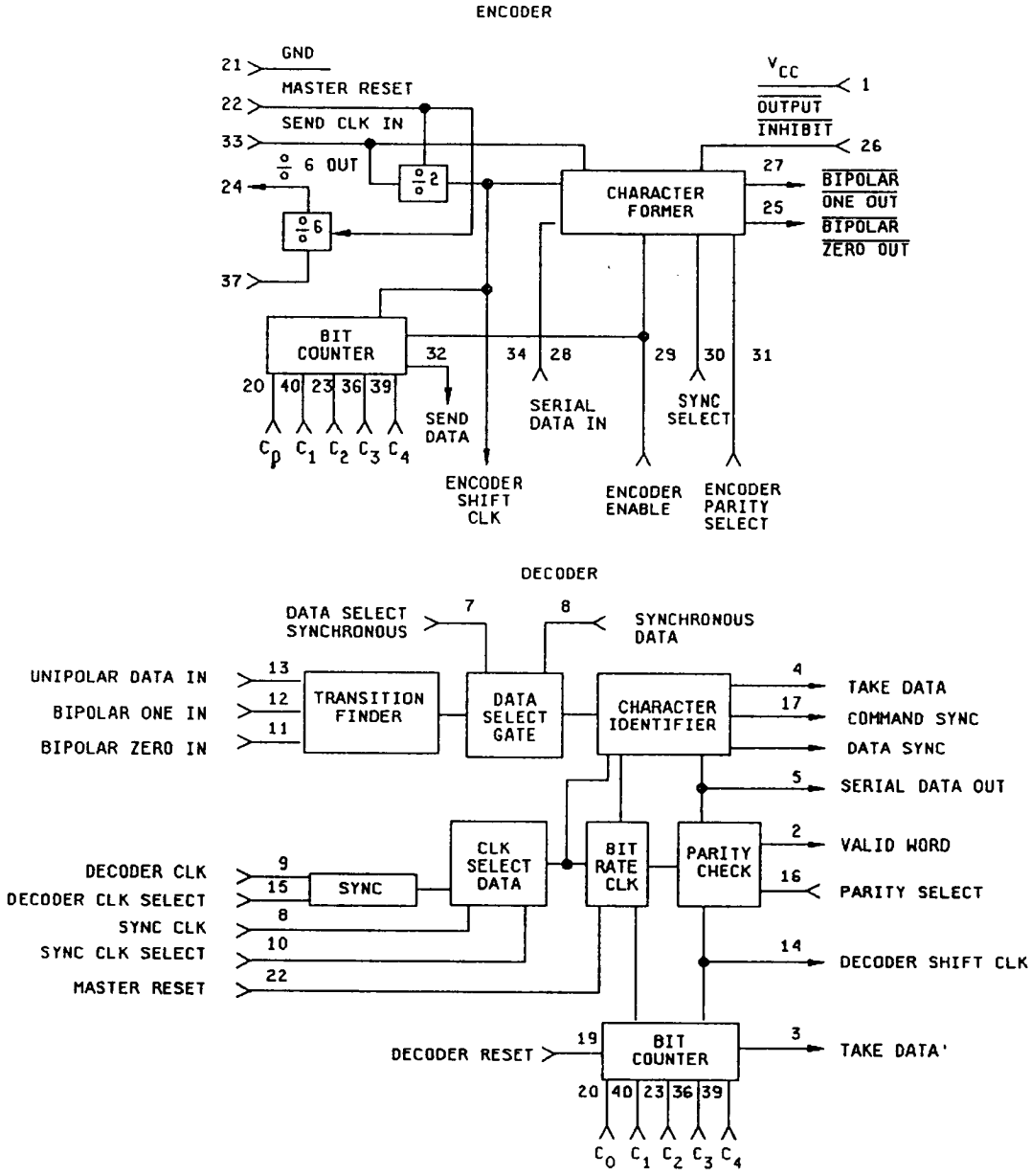


FIGURE 2. Block diagram.

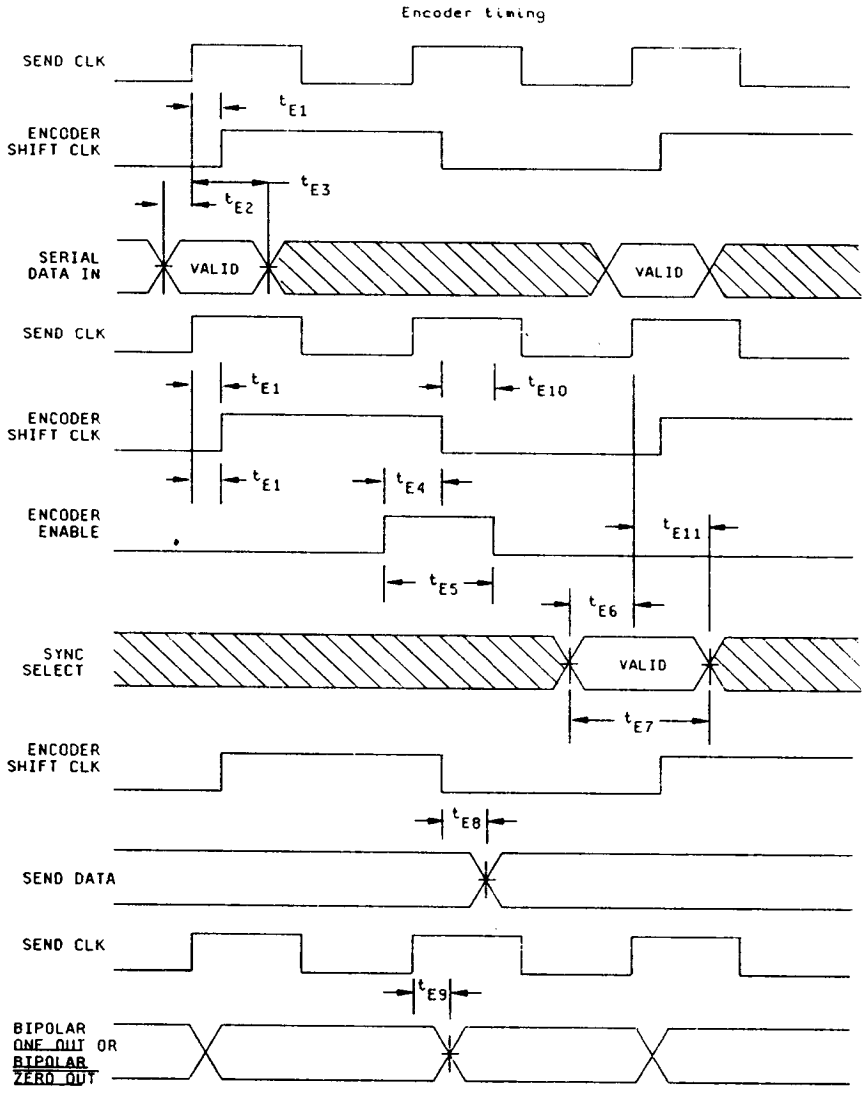


FIGURE 3. Timing diagrams.

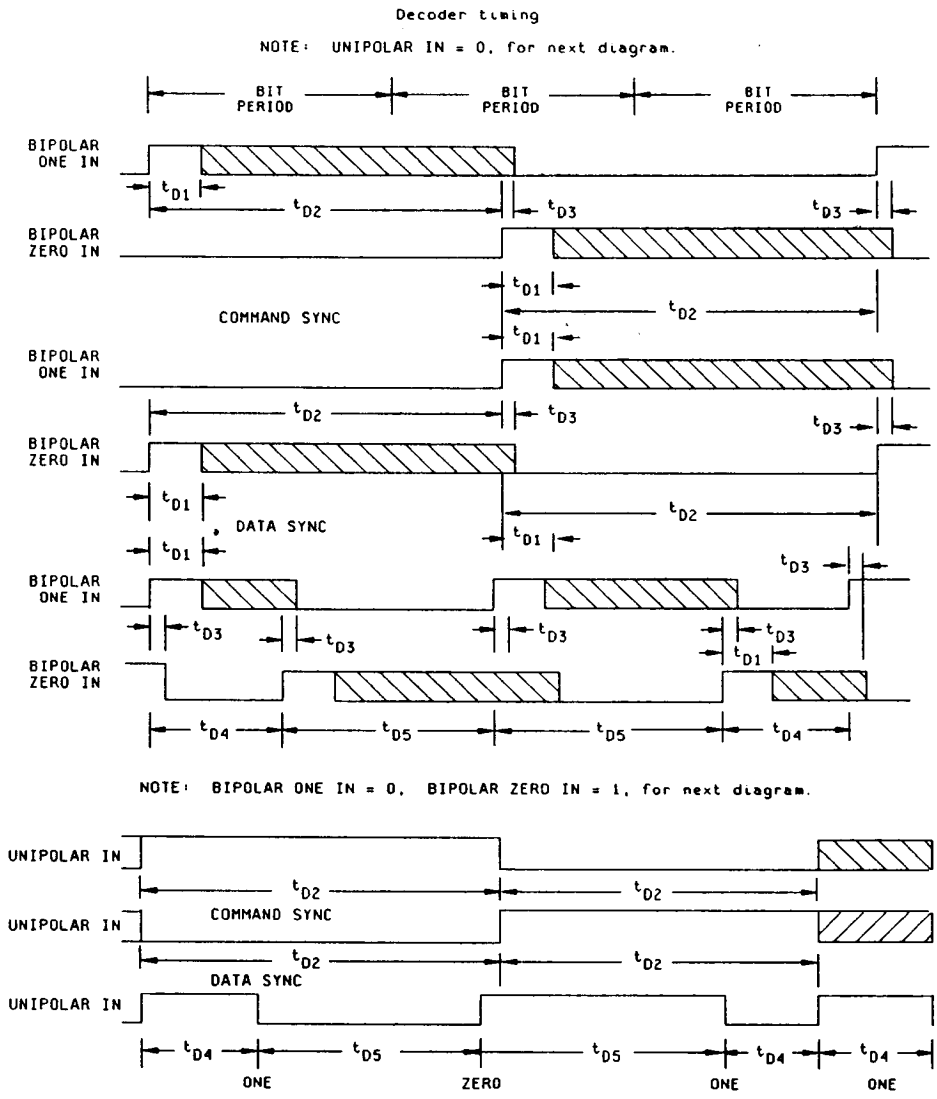


FIGURE 3. Timing diagrams - Continued.

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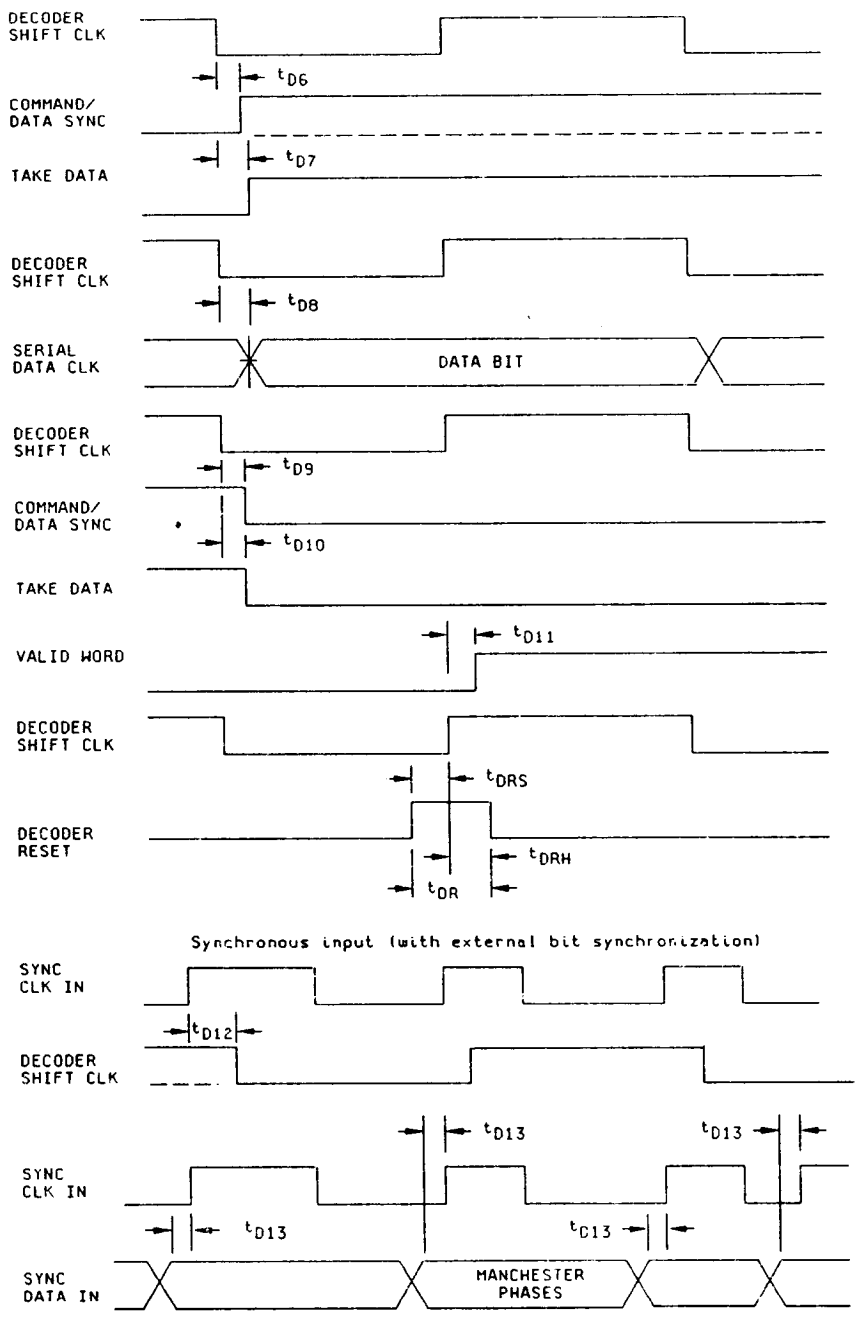
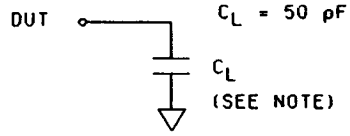
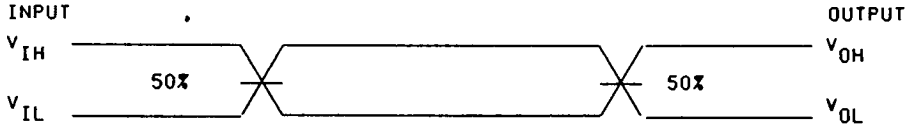


FIGURE 3. Timing diagrams - Continued.



NOTE: Includes stray and jig capacitance.



NOTE: AC testing: All inputs signals must switch between V_{IL} and V_{IH}.
Input rise and fall times are driven at 1 ns per volt.

NOTE: AC testing: All inputs signals must switch between V_{IL} and V_{IH}.
Input rise and fall times are driven at 1 ns per volt.

FIGURE 4. Input and output waveform.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1,2,3, 7,8,9 10,11 1/	1,2,3, 7,8, 10,11 1/	1,2,3, 7,8, 10,11 2/	1,2,3, 7,8, 10,11 1/	1,2,3, 7,8, 10,11 2/
Group A test requirements (see 4.4)	1,2,3,4, 7,8, 9,10,11	1,2,3,4, 7,8, 10,11 1/	1,2,3,4, 7,8, 9,10,11	1,2,3,4, 7,8, 9,10,11 1/	1,2,3,4, 7,8, 9,10,11
Group B end-point electrical parameters (see 4.4)	---	---	1,7,9	---	
Group C end-point electrical parameters (see 4.4)	1,7,9	1,7,9	---	1,7,9	1,7,9
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4 (C_I, $C_I/0$ measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

c. Subgroups 7 and 8 shall verify the functionality of the device. These tests form a part of the manufacturer's test tape and shall be maintained and available from the approved source of supply.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023	100%
Reverse bias burn-in	1015	100%
Burn-in parameters	1015, total of 240 hours at +125°C	100%
Radiographic	2012	100%

4.4.3.1 Additional criteria for device classes M, B, and S. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IIA herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table IIA herein.

d. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes M, B, and S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-8526.

6.4 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8526.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510 and MIL-STD-1331.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

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New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Pin description.

Pin number	Type 1/	Name	Section	Description
1		VCC	Both	Positive supply pin. A 0.1 uF decoupling capacitor from VCC (pin1) to GROUND (Pin 21) is recommended.
2	O	VALID WORD	Decoder	Output high indicates receipt of a valid word, (valid parity and no Manchester errors).
3	O	TAKE DATA'	Decoder	A continuous, free running signal provided for host timing or data handling. When data is present on the bus, this signal will be synchronized to the incoming data and will be identical to take data.
4	O	TAKE DATA	Decoder	Output is high during receipt of data after identification of a valid sync pulse and two valid Manchester bits.
5	O	SERIAL DATA OUT	Decoder	Delivers received data in correct NRZ format.
6	I	SYNCHRONOUS DATA	Decoder	Input presents Manchester data directly to character identification logic. SYNCHRONOUS DATA SELECT must be held high to use this input. If not used this pin must be held high.
7	I	SYNCHRONOUS DATA SELECT	Decoder	In high state allows the synchronous data to enter the character identification logic. Tie this input for asynchronous data.
8	I	SYNCHRONOUS CLOCK	Decoder	Input provides externally synchronized clock to the decoder, for use when receiving synchronous data. This input must be tied high when not in use.
9	I	DECODER CLOCK	Decoder	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the decoder. Input a frequency equal to 12X the data rate.

See footnote at end of table.

Pin number	Type 1/	Name	Section	Description
10	I	SYNCHRONOUS CLOCK SELECT	Decoder	In high state directs the SYNCHRONOUS CLOCK to control the decoder character identification logic. A low state selects the DECODER CLOCK.
11	I	BIPOLAR ZERO IN	Decoder	A high input should be applied when the bus is in its negative state. This pin must be held high when the unipolar input is used.
12	I	BIPOLAR ONE IN	Decoder	A High input should be applied when the bus is in its positive state. This pin must be held low when the unipolar input is used.
13	I	UNIPOLAR DATA IN	Decoder	With pin 11 high and pin 12 low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low.
14	O	DECODER SHIFT CLOCK	Decoder	Output which delivers a frequency (DECODER CLOCK ÷ 12), synchronous by the recovered serial data stream.
15	I	TRANSITION SELECT	Decoder	A high input to this pin causes the transition finder to synchronize on every transition of inout data. A low input causes the transition finder to synchronize only on mid-bit transitions.
16		N.C	Blank	Not connected.
17	O	COMMAND SYNC	Decoder	Output of a high from this pin occurs during output of decoder data which was preceded by a Commander (or Status) synchronizing charater.
18	I	DECODER PARITY SELECT	Decoder	An input for parity sense, calling for even parity with input high and odd parity with input low.
19	I	DECODER RESET	Decoder	A high input to this pin during a rising edge of DECODER shift CLOCK resets the decoder bit counting logic to a condition ready for a new word.
20	I	COUNT C0	Both	One of five binary inputs which established the total bit count to be encoded or decoded.
21		GROUND	Both	Supply pin.
22	I	MASTER RESET	Both	A high on this pin clears 2:1 counters in both encoder and decoder, and resets the ÷ 6 circuit.
23	I	COUNT C2	Both	See pin 20.
24	O	÷ 6 OUT	Encoder	Output from 6:1 divider which is driven by the ENCODER CLOCK.

1/ I = input, O = output.

Pin number	Type 1/	Name	Section	Description
25	O	$\overline{\text{BIPOLAR ZERO OUT}}$	Encoder	An active low output designed to drive the zero or negative sense of a bipolar line driver.
26	I	OUTPUT INHIBIT	Encoder	A low on this pin forces pin 25 and 27 high, the inactive states.
27	O	BIPOLAR ONE OUT	Encoder	An active low output designed to drive the one or positive sense of a bipolar line driver.
28	I	SERIAL DATA IN	Encoder	Accepts a serial data stream at a data rate rate equal to ENCODER SHIFT CLOCK.
29	I	ENCODER ENABLE	Encoder	A high on this pin initiates the encode cycle. (Subject to the preceding cycle being complete.)
30	I	SYNC SELECT	Encoder	Actuates a Command sync for an input high and Data sync for an input low.
31	I	ENCODER PARITY SELECT	Encoder	Sets transmit parity odd for a high input , even for a low input.
32	O	SEND DATA	Encoder	Is an active high output which enables the external source of serial data.
33	I	SEND CLOCK IN	Encoder	Clock input at a frequency equal to the data rate X2
34	O	ENCODER SHIFT CLOCK	Encoder	Output for shifting data into the Encoder. The Encoder samples SDI pin-28 on the low-to-high transition of ESC.
35		N.C	Blank	Not connected.
36	I	COUNT C3	Both	See pin 20.
37	I	ENCODER CLOCK	Encoder	Input to the 6:1 divider, a frequency equal to 12 times the data rate is usually input here.
38	O	DATA SYNC	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded by a data synchronizing character.
39	I	COUNT C4	Both	See pin 20.
40	I	COUNT C1	Both	See pin 20.

1/ I = input, O = output.