

RJK1052DPB

Silicon N Channel Power MOS FET Power Switching

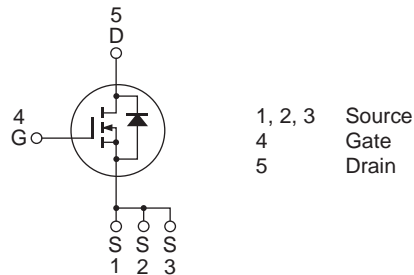
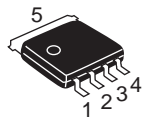
R07DS0083EJ0102
(Previous: REJ03G1769-0101)
Rev.1.02
Jul 30, 2010

Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 15 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)
- Pb-free
- Halogen-free

Outline

RENESAS Package code: PTZZ0005DA-A
(Package name: LFPAK)



Application

- Switching Mode Power Supply

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	20	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	80	A
Body-drain diode reverse drain current	I_{DR}	20	A
Avalanche current	I_{AP} ^{Note 2}	10	A
Avalanche energy	E_{AR} ^{Note 2}	10	mJ
Channel dissipation	P_{ch} ^{Note 3}	55	W
Channel to Case Thermal Resistance	θ_{ch-C}	2.27	$^\circ\text{C}/\text{W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

- Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
 2. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$
 3. $T_c = 25^\circ\text{C}$

This product is for the low voltage drive ($\leq 10\text{V}$).

If the driving voltage is over 10 V under normal conditions, please use the product for high gate to source cutoff voltage ($V_{GS(off)}$) which characteristics has been improved.

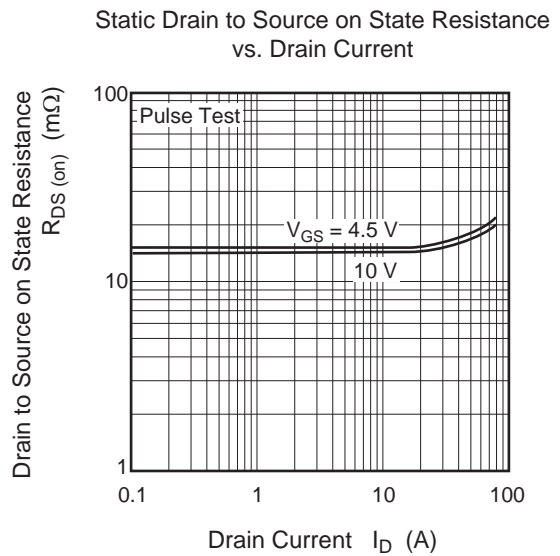
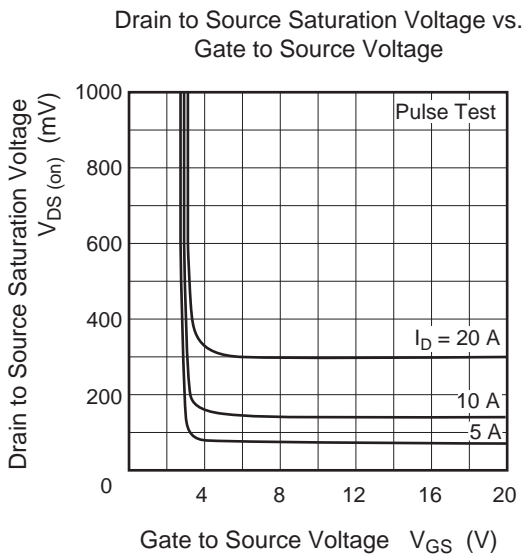
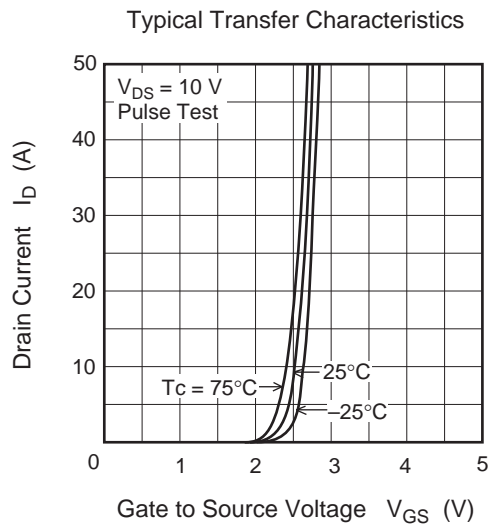
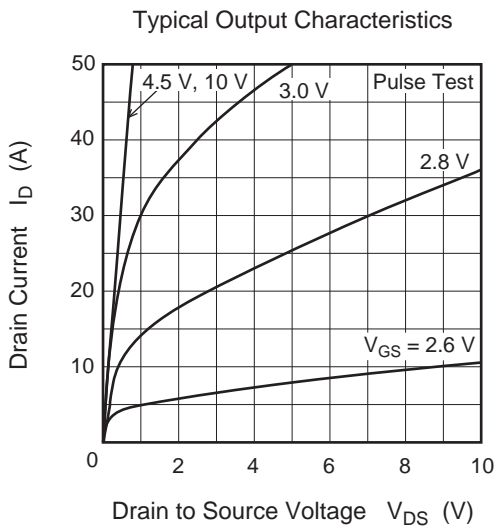
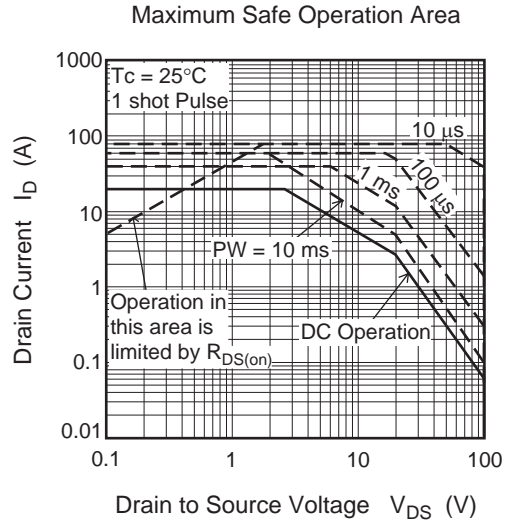
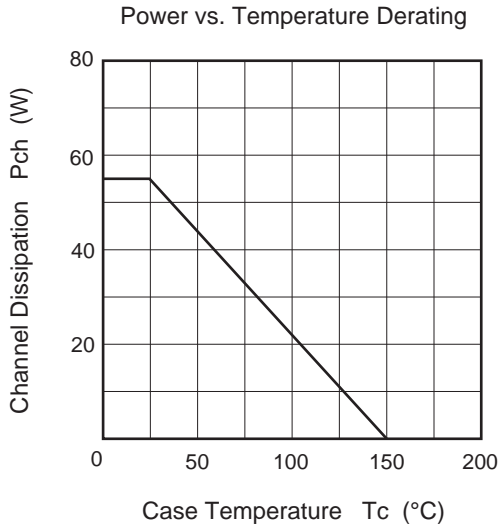
Electrical Characteristics

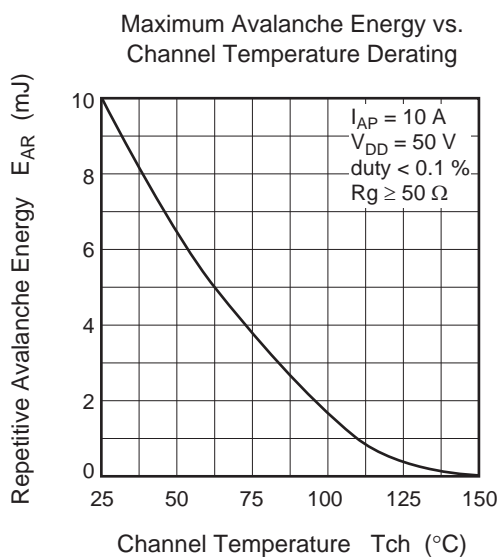
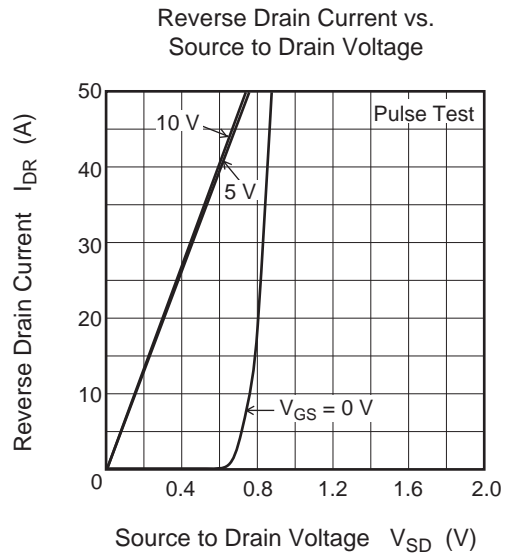
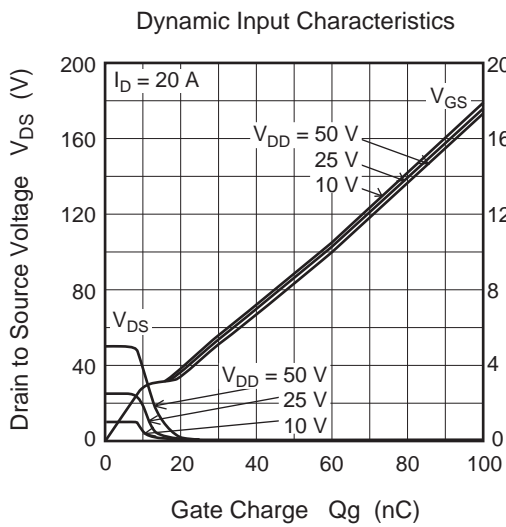
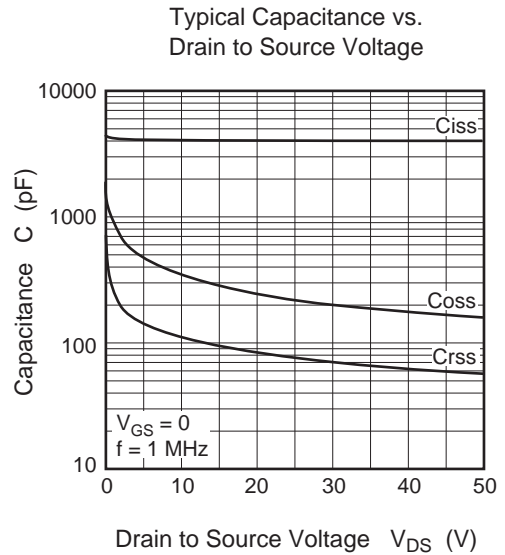
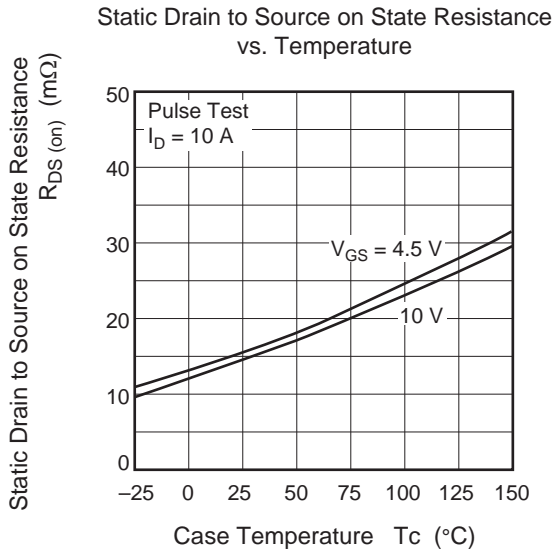
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0 \text{ V}$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0 \text{ V}$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 100 \text{ V}$, $V_{GS} = 0 \text{ V}$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	15	20	$\text{m}\Omega$	$I_D = 10 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	16	22	$\text{m}\Omega$	$I_D = 10 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	42	—	S	$I_D = 10 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	4160	—	pF	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	354	—	pF	
Reverse transfer capacitance	C_{rss}	—	136	—	pF	
Gate Resistance	R_g	—	0.4	—	Ω	
Total gate charge	Q_g	—	29	—	nC	$V_{DD} = 50 \text{ V}$, $V_{GS} = 4.5 \text{ V}$, $I_D = 20 \text{ A}$
Gate to source charge	Q_{gs}	—	12	—	nC	
Gate to drain charge	Q_{gd}	—	9.2	—	nC	
Turn-on delay time	$t_{d(on)}$	—	11	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 10 \text{ A}$, $V_{DD} \cong 30 \text{ V}$, $R_L = 3 \Omega$, $R_g = 4.7 \Omega$
Rise time	t_r	—	5.0	—	ns	
Turn-off delay time	$t_{d(off)}$	—	54	—	ns	
Fall time	t_f	—	6.8	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.83	1.1	V	$I_F = 20 \text{ A}$, $V_{GS} = 0 \text{ V}$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	46	—	ns	$I_F = 20 \text{ A}$, $V_{GS} = 0 \text{ V}$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

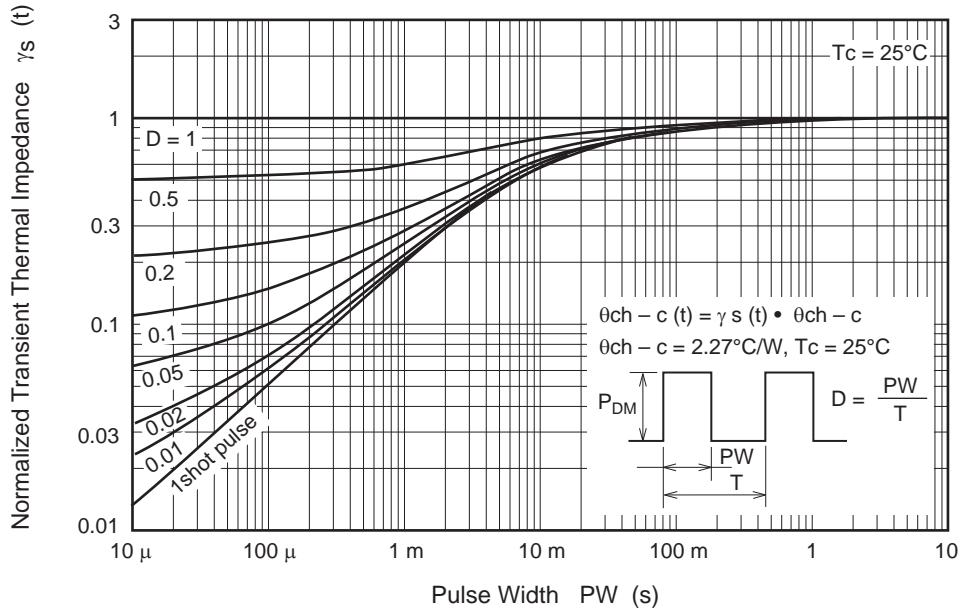
Notes: 4. Pulse test

Main Characteristics

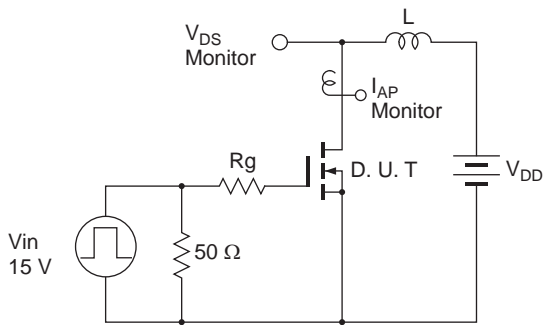




Normalized Transient Thermal Impedance vs. Pulse Width

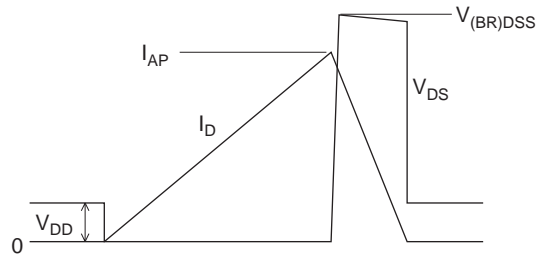


Avalanche Test Circuit

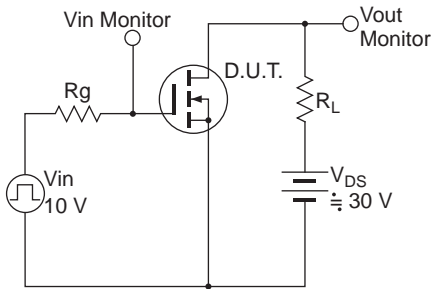


Avalanche Waveform

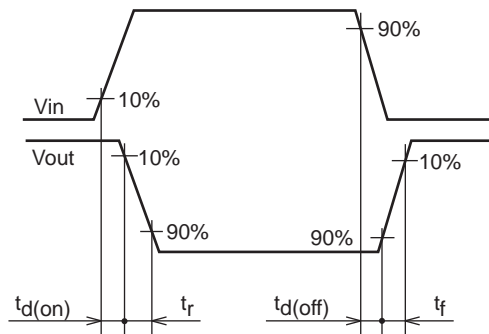
$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



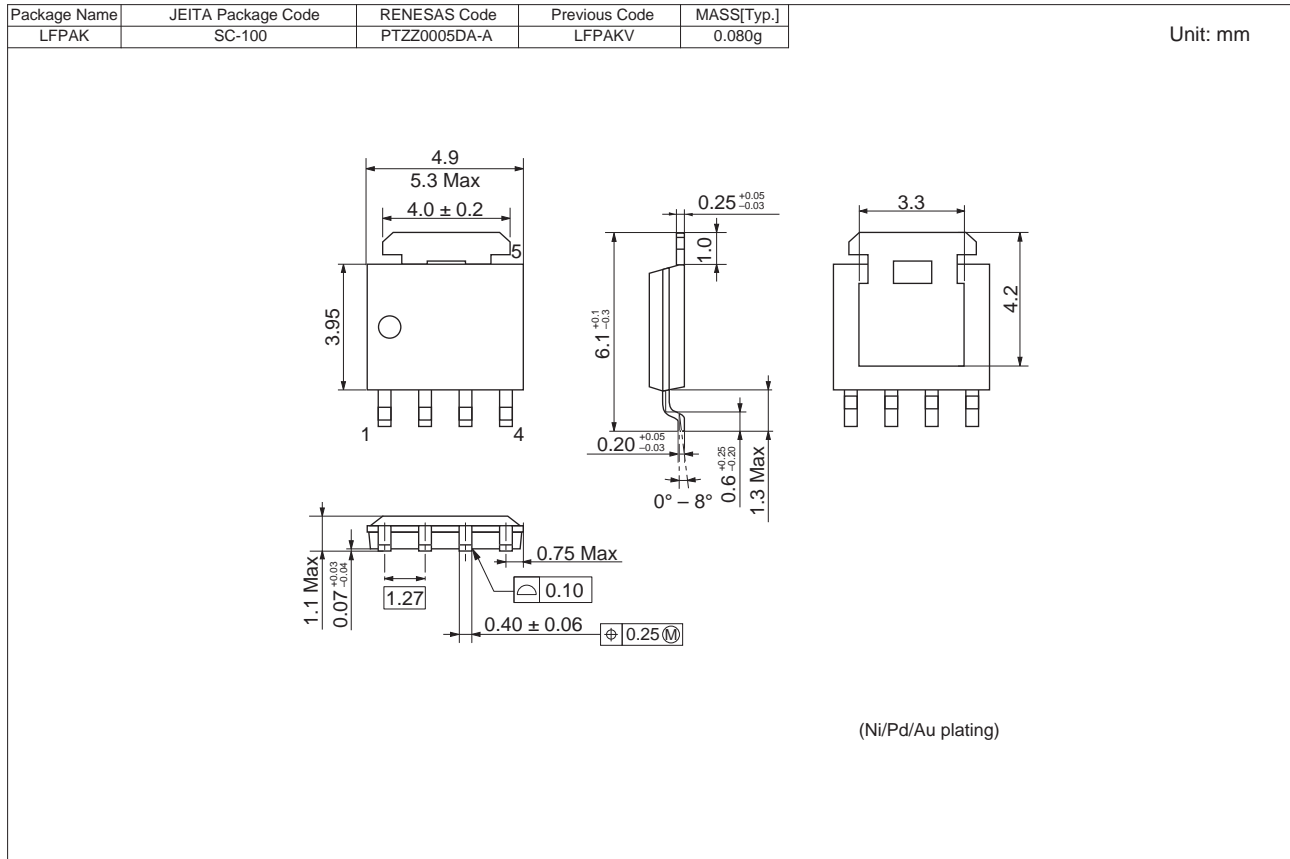
Switching Time Test Circuit



Switching Time Waveform



Package Dimensions



Ordering Information

Part No.	Quantity	Shipping Container
RJK1052DPB-00-J5	2500 pcs	Taping

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