Quad Driver

ISL35411

The ISL35411 is a quad de-emphasis driver with extended functionality for advanced protocols operating with line rates up to 11.1 Gbps such as InfiniBand (QDR) and 40G Ethernet (40GBASE-CR4/SR4). The ISL35411 is a high-speed driver/limiting amplifier with built in de-emphasis to drive twin-axial copper cables and compensate for the frequency dependent attenuation of PCB traces such as the SFI channel in the 10G SFP+ specification (SFF-8431).

Used in conjunction with Intersil's ISL36411 receive-side equalizer, ISL35411 enables active copper cable assemblies that support 10G serial data transmission over >15m of twin-axial copper cables.

Operating on a single 1.2V power supply, the ISL35411 enables per channel throughputs of 10Gbps to 11.1Gbps. The ISL35411 uses current mode logic (CML) input/output and is packaged in a 4mmx7mm 46 lead QFN.

Features

- Supports four channels with data rates up to 11.1Gbps
- Low power (90mW per channel)
- Low latency
- Adjustable output de-emphasis
- Four drivers in a 4mmx7mm QFN package for straight route-through architecture & simplified routing
- Supports 64b/66b encoded data – long run lengths
- Line silence preservation
- 1.2V supply voltage
- TX_Disable

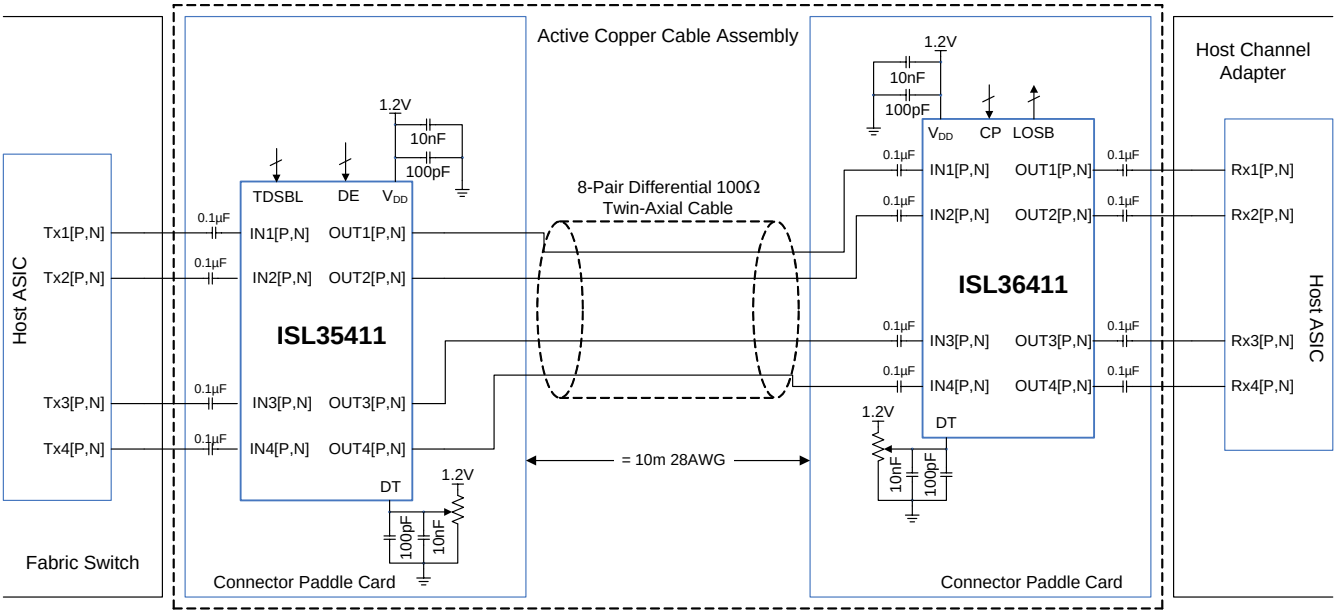
Applications

- QSFP active copper cable modules
- InfiniBand (QDR)
- 40G Ethernet (40GBase-CR4/SR4)
- 100G Ethernet (100GBase-CR10/SR10)
- High-speed active cable assemblies
- High-speed printed circuit board (PCB) traces

Benefits

- Thinner gauge cable
- Extends cable reach greater than 3x
- Improved BER

Typical Application Circuit



Ordering Information

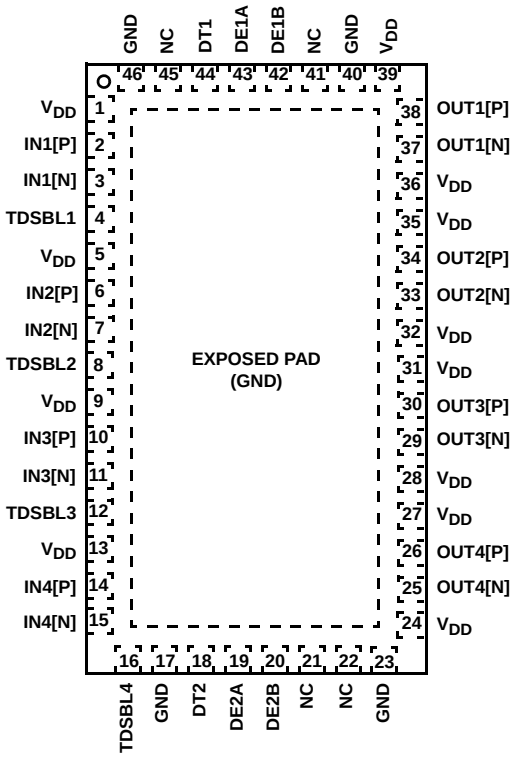
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL35411DRZ-TS	ISL35411DRZ	0 to +85	46 Ld QFN (7'' 100 pcs.)	L46.4x7
ISL35411DRZ-T7	ISL35411DRZ	0 to +85	46 Ld QFN (7" 1k pcs.)	L46.4x7

NOTES:

1. "-TS" and "-T7" suffix is for Tape and Reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL35411. For more information on MSL please see techbrief TB363.

Pin Configuration

ISL35411
(46 LD QFN)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
V_{DD}	1, 5, 9, 13, 24, 27, 28, 31, 32, 35, 36, 39	Power supply. 1.2V supply voltage. The use of parallel 100pF and 10nF decoupling capacitors to ground is recommended for each of these pins for broad high-frequency noise suppression.
IN1[P,N]	2, 3	Driver 1 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
TDSBL1	4	Transmit disable pin for Driver 1. Disables the driver when pulled to VDD. Connected to ground for normal operation.
IN2[P,N]	6, 7	Driver 2 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
TDSBL2	8	Transmit disable pin for Driver 2. Disables the driver when pulled to VDD. Connected to ground for normal operation.
IN3[P,N]	10, 11	Driver 3 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
TDSBL3	12	Transmit disable pin for Driver 3. Disables the driver when pulled to VDD. Connected to ground for normal operation.
IN4[P,N]	14, 15	Driver 4 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
TDSBL4	16	Transmit disable pin for Driver 4. Disables the driver when pulled to VDD. Connected to ground for normal operation.
GND	17, 23, 40, 46	These pins should be grounded.
DT2	18	Detection Threshold for drivers 3 and 4. Reference DC voltage threshold for input signal power detection. Data outputs OUT3 and OUT4 are muted when the power of IN3 and IN4, respectively, fall below the threshold. Tie to ground to disable electrical idle preservation and always enable the limiting amplifier.
DE2[A,B,]	19, 20	Control pins for setting de-emphasis on drivers 3 and 4. CMOS logic inputs. Pins are read as a 2-digit number to set the de-emphasis level. A is the MSB, and B is the LSB. Pins are internally pulled up and pulled down with 25kΩ resistors.
NC	21, 22, 41, 45	Not connected: Do not make any connections to these pins.
OUT4[N,P]	25, 26	Driver 4 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
OUT3[N,P]	29, 30	Driver 3 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
OUT2[N,P]	33, 34	Driver 2 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
OUT1[N,P]	37, 38	Driver 1 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
DE1[B,A]	42, 43	Control pins for setting de-emphasis on drivers 1 and 2. CMOS logic inputs. Pins are read as a 2-digit number to set the de-emphasis level. A is the MSB, and B is the LSB. Pins are internally pulled up and pulled down with 25kΩ resistors.
DT1	44	Detection Threshold for drivers 1 and 2. Reference DC voltage threshold for input signal power detection. Data outputs OUT1 and OUT2 are muted when the power of IN1 and IN2, respectively, fall below the threshold. Tie to ground to disable electrical idle preservation and always enable the limiting amplifier.
Exposed Pad	-	Exposed ground pad. For proper electrical and thermal performance, this pad should be connected to the PCB ground plane.

Absolute Maximum Ratings

Supply Voltage (V_{DD} to GND) . . . . . -0.3V to 1.5V
Voltage at All Input Pins . . . . . -0.3V to 1.5V
ESD Ratings
Human Body Model
High-Speed Pins 1.5kV
All Other Pins 2kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
46 Ld QFN Package (Notes 4, 5) . .	33	2.8

Operating Ambient Temperature Range . . . . . 0°C to +85°C
Storage Ambient Temperature Range . . . . -55°C to +150°C
Maximum Junction Temperature . . . . . +125°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Operating Conditions

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		1.1	1.2	1.3	V
Operating Ambient Temperature	T_A		0	25	85	°C
Bit Rate		NRZ data applied to any channel		10	11.1	Gbps

Control Pin Characteristics

V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 600mV_{P-P}, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Input LOW Logic Level	V_{IL}		0		350	mV
Input HIGH Logic Level	V_{IH}		750		V_{DD}	mV
Input Current		Current draw on digital pin, i.e., DE[k][A,B]		100	200	µA

Electrical Characteristics

V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 600mV_{P-P}, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}	De-Emphasis Disabled		260		mA	6
		De-Emphasis Enabled		300		mA	6
		Transmit Disable Mode		5.6		mA	6
Input Amplitude Range	V_{IN}	Measured differentially at data source	120		1600	mV_{P-P}	
DC Differential Input Resistance		Measured on input channel IN[k]	80	100	120	Ω	
DC Single-Ended Input Resistance		Measured on input channel IN[k]P or IN[k]N, with respect to V_{DD}	40	50	60	Ω	
Input Return Loss Limit (Differential)	$S_{DD}11$	100MHz to 4.1GHz		See 7		dB	7
		4.1GHz to 11.1GHz		See 8		dB	8
Input Return Loss Limit (Common Mode)	$S_{CC}11$	100MHz to 2.5GHz		See 9		dB	9
		2.5GHz to 11.1GHz		-3		dB	12
Input Return Loss Limit (Com. to Diff. Conversion)	$S_{DC}11$	100MHz to 11.1GHz		-10		dB	12
Output Amplitude Range	V_{OUT}	Measured differentially at OUT[k]P and OUT[k]N with 50Ω load on both output pinsde-emphasis disabled	450	700	820	mV_{P-P}	
Differential Output Impedance		Measured on OUT[k]	80	105	120	Ω	

Electrical Characteristics V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 600mV_{P-P}, unless otherwise noted. **(Continued)**

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Output Return Loss Limit (Differential)	$S_{DD}22$	100 MHz to 4.1GHz		See 7		dB	7
		4.1GHz to 11.1GHz		See 8		dB	8
Output Return Loss Limit (Common Mode)	$S_{CC}22$	100MHz to 2.5GHz		See 9		dB	9
		2.5GHz to 11.1GHz		-3		dB	12
Output Return Loss Limit (Com. to Diff. Conversion)	$S_{DC}22$	100MHz to 11.1GHz		-10		dB	12
Residual Deterministic Jitter		11.1Gbps; no channel attenuation; de-emphasis disabled		0.1		UI	10
Random Jitter				0.7		ps_{RMS}	
Output Transition Time	t_r, t_f	20% to 80%		35		ps	11
Minimum De-Emphasis Level				0		dB	
Maximum De-Emphasis Level				4		dB	
De-Emphasis Resolution				0.5		dB	

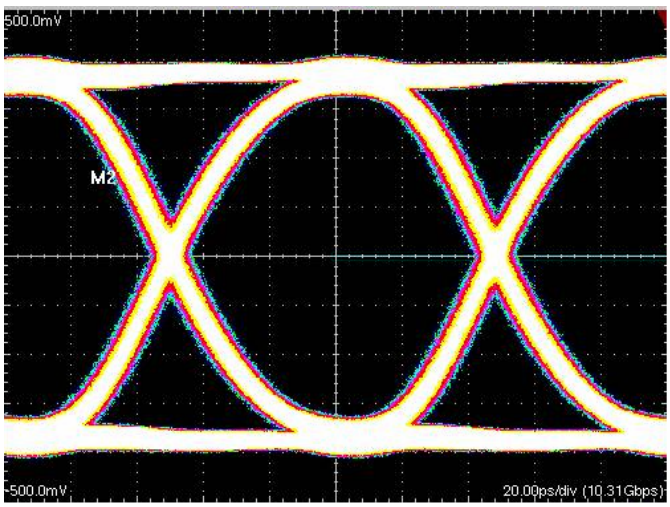
NOTES:

6. Temperature = +25°C, V_{DD} = 1.2V.
7. Maximum Reflection Coefficient given by equation SDDXX(dB)= -12 + 2*√(f), with f in GHz. Established by characterization and not production tested.
8. Maximum Reflection Coefficient given by equation SDDXX(dB)= -6.3 + 13Log10(f/5.5), with f in GHz. Established by characterization and not production tested.
9. Reflection Coefficient given by equation SCCXX(dB) < -7 + 1.6*f, with f in GHz. Established by characterization and not production tested.
10. Measured using a PRBS 2^7-1 pattern.
11. Rise and fall times measured with a 1-1-1-1-1-1-1-1-0-0-0-0-0-0-0-0 test pattern at 11.1Gbps with no channel loss and disabled de-emphasis.
12. Limits established by characterization and are not production tested.

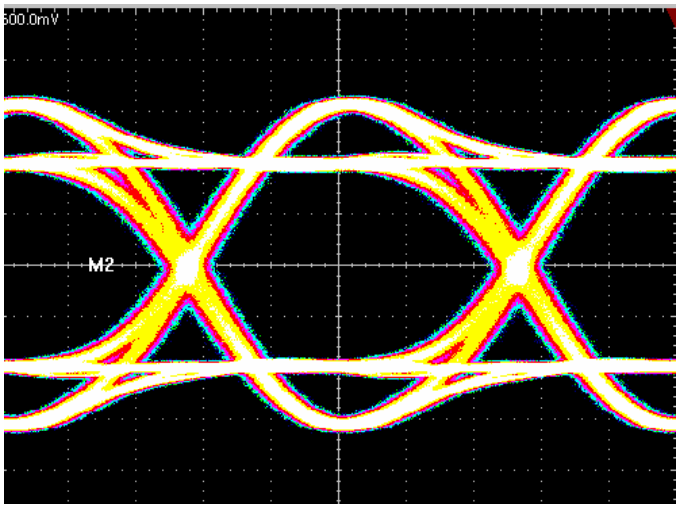
Typical Performance Characteristics

Performance is measured using the test setup illustrated in Figure 1. The signal from the pattern generator is launched into the chip evaluation board. The ISL35411 output signal is then visualized on a scope to determine signal integrity parameters such as jitter.

FIGURE 1. DEVICE CHARACTERIZATION TEST SETUP



2A. DE-EMPHASIS 0



2B. DE-EMPHASIS 6

FIGURE 2. ISL35411 10.3125Gbps OUTPUT; NO CHANNEL; PRBS-31

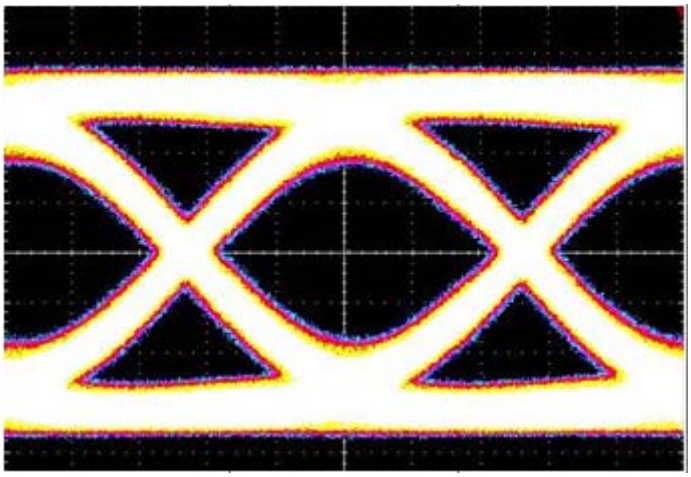


FIGURE 3. ISL35411 10.3125 GBPS OUTPUT AFTER A 22-INCH FR-408 TRACE, PRBS-31; DE-EMPHASIS 6

Operation

The ISL35411 is an advanced driver for high-speed interconnects. A functional diagram of ISL35411 is shown in Figure 4. In addition to a de-emphasis circuit to compensate for channel loss and improve signal fidelity, the ISL35411 contains unique integrated features to preserve special signaling protocols typically broken by other drivers. The signal detect function is used to mute the channel output when the equalized signal falls below the level determined by the Detection Threshold (DT) pin voltage. This function is intended to preserve periods of line silence

As illustrated in Figure 4, the core of the high-speed signal path in the ISL35411 is a sophisticated driver followed by a de-emphasis circuit. The device applies pre-distortion to compensate for skin effect loss, dielectric loss, and impedance discontinuities in the transmission channel.

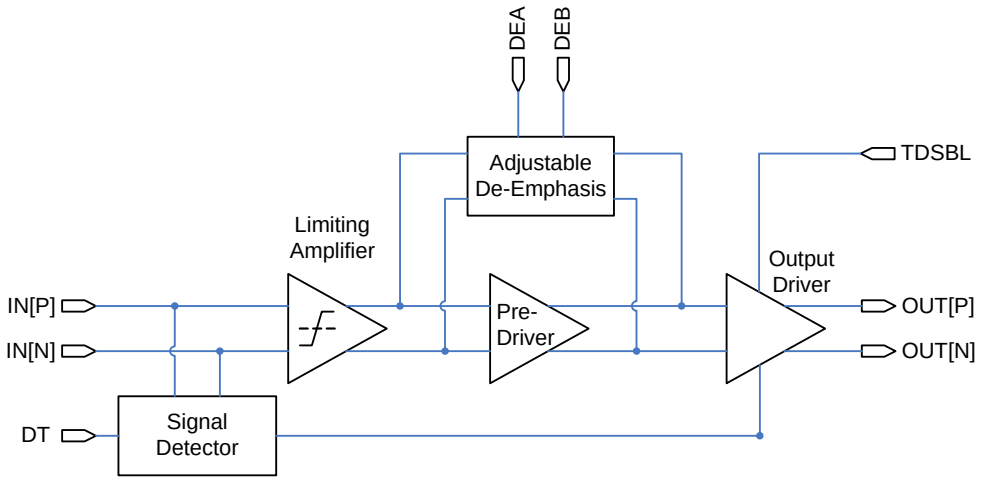


FIGURE 4. FUNCTIONAL DIAGRAM OF A SINGLE CHANNEL WITHIN THE ISL35411

Adjustable De-emphasis

ISL35411 features a settable de-emphasis driver for custom signal restoration.

The voltages at the DE pins are used to determine the de-emphasis levels of each 2-channel group – from 0dB to 4dB in 0.5dB increments. For each two of the four channels the [A] and [B] control pins DE[k] are associated with a non binary word. [A] and [B] can take one of three different values: 'LOW', 'MIDDLE', or 'HIGH'. This is achieved by leaving the DE pins floating or connecting them either to VDD or GND through 0Ω resistors. Table 1 defines the mapping from the 2-bit DE word to the 7 possible de-emphasis levels.

TABLE 1. MAPPING BETWEEN DE-EMPHASIS LEVEL AND DE-PIN CONNECTIVITY

DE PIN CONNECTION		NOMINAL DE-EMPHASIS LEVEL; 10.3125Gbps TO 11.1Gbps (dB)	DE-EMPHASIS SETTING
DE[A]	DE[B]		
Open	Open	0	0
Open	GND	0.6	1
Open	VDD	1.1	2
GND	Open	1.6	3
GND	GND	2.3	4
GND	VDD	3	5
VDD	Open	4	6

Line Silence / Quiescent Mode

The ISL35411 is capable of maintaining periods of line silence by monitoring its input pins for loss of signal (LOS) conditions and subsequently muting the output drivers when such a condition is detected. A reference voltage applied to the detection threshold DT[k] pins is used to set the LOS threshold of the internal signal detection circuitry. For most applications, it is recommended to leave the DT pin floating at its default internal bias. If the sensitivity of the detection threshold needs to be adjusted, the DT voltage can be adjusted with an external pull-up resistor. The resistor values should be validated on an application-specific basis. Connect the DT pin to ground in order to disable this feature and prevent the outputs from muting during line silence.

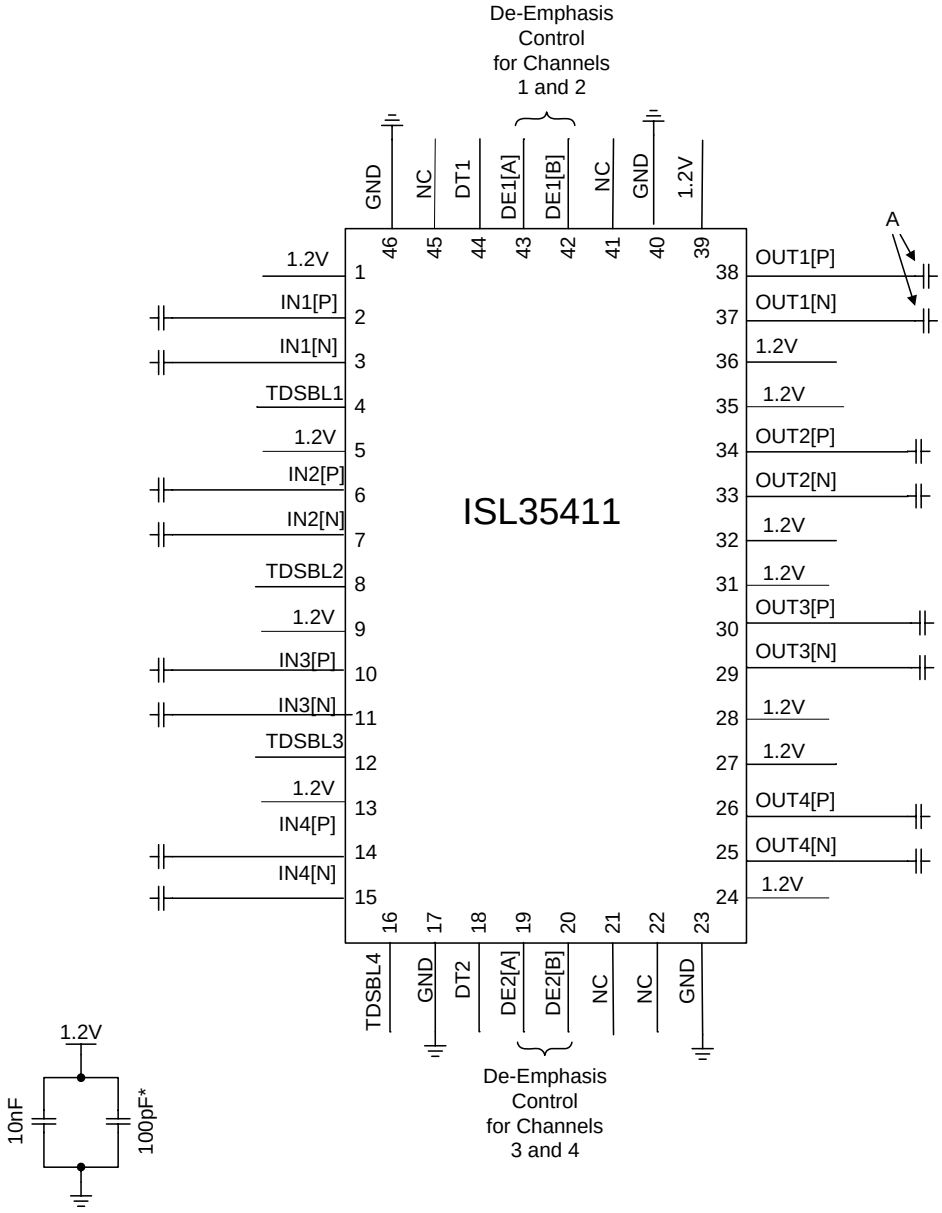
PCB Layout Considerations

Because of the high speed of the ISL35411 signals, careful PCB layout is critical to maximize performance. The following guidelines should be adhered to as closely as possible:

- All high speed differential pair traces should have a characteristic impedance of 50Ω with respect to ground plane and 100Ω with respect to each other.
- Avoid using vias for high speed traces as this will create discontinuity in the traces' characteristic impedance.
- Input and output traces need to have DC blocking capacitors (100nF). Capacitors should be placed as close to the chip as possible.
- For each differential pair, the positive trace and the negative trace need to be of the same length in order to avoid intra-pair skew. A Serpentine technique may be used to match trace lengths.
- Maintain a constant solid ground plane underneath the high-speed differential traces.
- Each VDD pin should be connected to 1.2V and also bypassed to ground through a 10nF and a 100pF capacitor in parallel. Minimize the trace length and avoid vias between the VDD pin and the bypass capacitors in order to maximize the power supply noise rejection.
- If 4 channels of the device are set to the same boost, then the quantity of CP resistors can be reduced by tying both CP pins together.

Application Information

Typical application schematic for ISL35411 is shown in Figure 5.



Bypass circuit for each V_{DD} pin
(*100pF capacitor should be positioned closest to the pin)

A) DC Blocking Capacitors = X7R or COG
0.1µF (>6GHz bandwidth)

NOTES:

13. See “Adjustable De-emphasis” on page 7 for information on how to connect the DE pins.

14. See “Line Silence/Quiescent Mode” on page 7 for details on DT pin operation.

FIGURE 5. TYPICAL APPLICATION REFERENCE SCHEMATIC FOR ISL35411

About Q:Active®

Intersil has long realized that to enable the complex server clusters of next generation datacenters, it is critical to manage the signal integrity issues of electrical interconnects. To address this, Intersil has developed its groundbreaking Q:ACTIVE® product line. By integrating its analog ICs inside cabling interconnects, Intersil is able to achieve unsurpassed improvements in reach, power consumption, latency, and cable gauge size as well as increased airflow in tomorrow's datacenters. This new technology transforms passive cabling into intelligent "roadways" that yield lower operating expenses and capital expenditures for the expanding datacenter.

Intersil Lane Extenders allow greater reach over existing cabling while reducing the need for thicker cables. This significantly reduces cable weight and clutter, increases airflow, and improves power consumption.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
3/16/10	FN6971.1	page 4: • Control pin characteristics: change 'output low/high' to 'input', change symbols to VIL/VIH; condition – blank VIL : min 0, max 350, delete typical "0" VIH; min 750 mV • Input current: typ 100; max 200 • Added High-Speed pins to ESD Ratings as follows to Abs Max Ratings: ESD Ratings Human Body Model High-Speed Pins 1.5kV All Other Pins 2kV • Removed the fland pattern on page 9 due to information already in outline drawing.
2/8/10	FN6971.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL35411

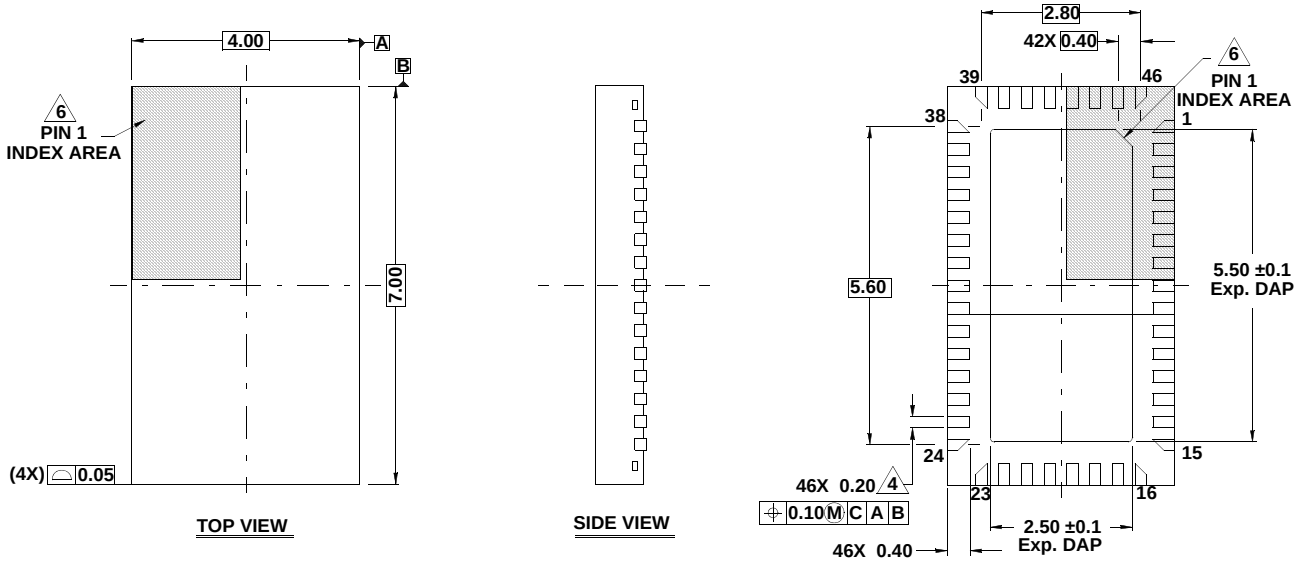
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

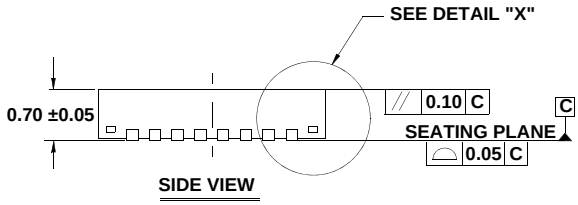
FITs are available from our website at http://rel.intersil.com/reports/search.php

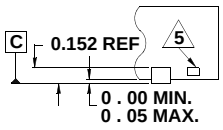
Package Outline Drawing

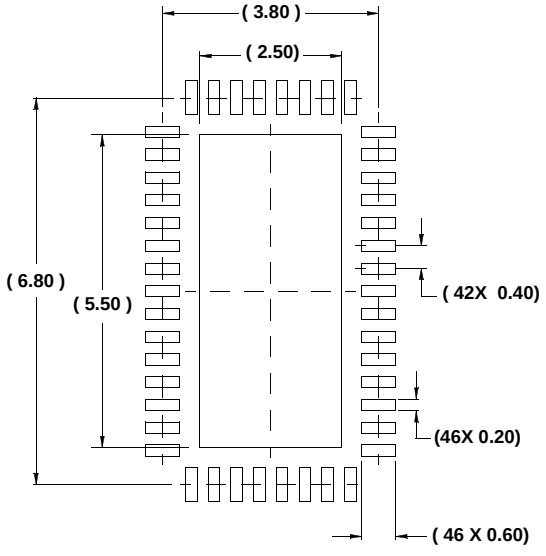
L46.4x7

46 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE (TQFN)
Rev 0, 9/09









NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.