



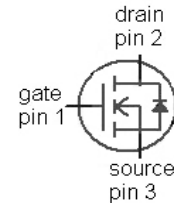
OptiMOS™ 3 Power-Transistor
Features

- Fast switching MOSFET for SMPS
- Optimized technology for DC/DC converters
- Qualified according to JEDEC¹⁾ for target applications
- N-channel, logic level
- Excellent gate charge $\times R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Avalanche rated
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product Summary

V_{DS}	30	V
$R_{DS(on),max}$	11.4	m Ω
I_D	30	A

Type	IPP114N03L G	IPB114N03L G
		
Package	PG-TO220-3-1	PG-TO263-3
Marking	114N03L	114N03L


Maximum ratings, at $T_j=25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$V_{GS}=10\text{ V}, T_C=25\text{ }^\circ\text{C}$	30	A
		$V_{GS}=10\text{ V}, T_C=100\text{ }^\circ\text{C}$	30	
		$V_{GS}=4.5\text{ V}, T_C=25\text{ }^\circ\text{C}$	30	
		$V_{GS}=4.5\text{ V}, T_C=100\text{ }^\circ\text{C}$	26	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ }^\circ\text{C}$	210	
Avalanche current, single pulse ³⁾	I_{AS}	$T_C=25\text{ }^\circ\text{C}$	30	
Avalanche energy, single pulse	E_{AS}	$I_D=12\text{ A}, R_{GS}=25\text{ }\Omega$	30	mJ
Reverse diode dv/dt	dv/dt	$I_D=30\text{ A}, V_{DS}=24\text{ V}, di/dt=200\text{ A}/\mu\text{s}, T_{j,max}=175\text{ }^\circ\text{C}$	6	kV/ μs
Gate source voltage	V_{GS}		± 20	V

¹⁾ J-STD20 and JESD22

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	38	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}		-	-	3.9	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ⁴⁾	-	-	40	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}, I_{\text{D}}=1\text{ mA}$	30	-	-	V
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\text{ }\mu\text{A}$	1	-	2.2	
Zero gate voltage drain current	I_{DSS}	$V_{\text{DS}}=30\text{ V}, V_{\text{GS}}=0\text{ V}, T_j=25\text{ °C}$	-	0.1	1	μA
		$V_{\text{DS}}=30\text{ V}, V_{\text{GS}}=0\text{ V}, T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{\text{GS}}=20\text{ V}, V_{\text{DS}}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance ⁵⁾	$R_{\text{DS(on)}}$	$V_{\text{GS}}=4.5\text{ V}, I_{\text{D}}=25\text{ A}$	-	13.1	16.4	m Ω
		$V_{\text{GS}}=10\text{ V}, I_{\text{D}}=30\text{ A}$	-	9.5	11.4	
Gate resistance	R_{G}		-	1.2	-	Ω
Transconductance	g_{fs}	$ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}, I_{\text{D}}=30\text{ A}$	24	49	-	S

²⁾ See figure 3 for more detailed information

³⁾ See figure 13 for more detailed information

⁴⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

⁵⁾ Measured from drain tab to source pin

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V},$ $f=1\text{ MHz}$	-	1100	1500	pF
Output capacitance	C_{oss}		-	460	610	
Reverse transfer capacitance	C_{rss}		-	22	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=10\text{ V},$ $I_D=30\text{ A}, R_G=1.6\ \Omega$	-	3.8	-	ns
Rise time	t_r		-	3.0	-	
Turn-off delay time	$t_{d(off)}$		-	15	-	
Fall time	t_f		-	2.4	-	

Gate Charge Characteristics⁵⁾

Gate to source charge	Q_{gs}	$V_{DD}=15\text{ V}, I_D=30\text{ A},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	3.7	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	1.7	-	
Gate to drain charge	Q_{gd}		-	1.6	-	
Switching charge	Q_{sw}		-	3.6	-	
Gate charge total	Q_g		-	6.6	-	
Gate plateau voltage	$V_{plateau}$		-	3.5	-	
Gate charge total	Q_g	$V_{DD}=15\text{ V}, I_D=30\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	14	-	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	5.7	-	
Output charge	Q_{oss}	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	12	-	

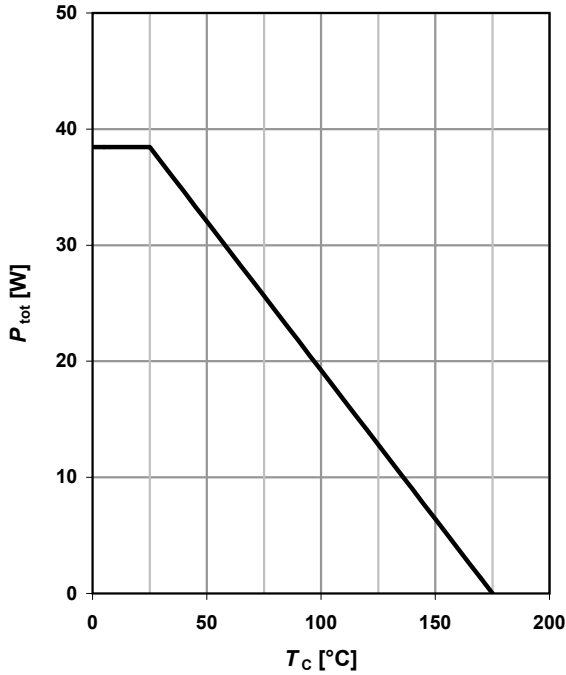
Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	30	A
Diode pulse current	$I_{S,pulse}$		-	-	210	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=30\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.97	1.2	V
Reverse recovery charge	Q_{rr}	$V_R=15\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$	-	-	10	nC

⁶⁾ See figure 16 for gate charge parameter definition

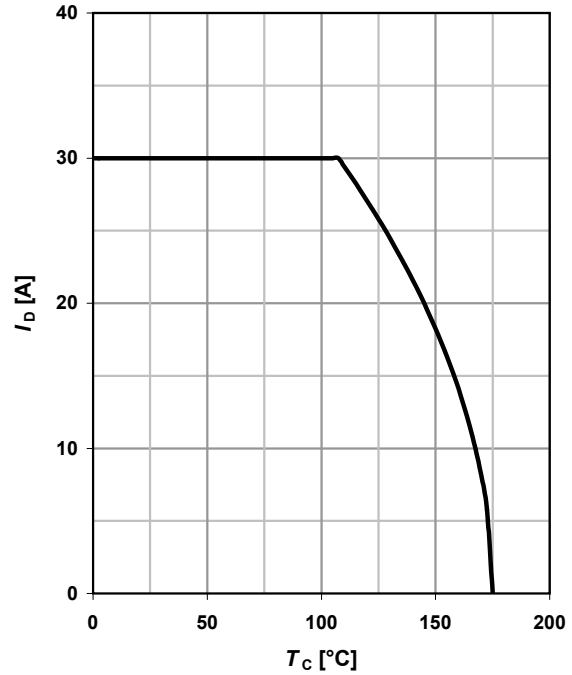
1 Power dissipation

$$P_{\text{tot}} = f(T_c)$$



2 Drain current

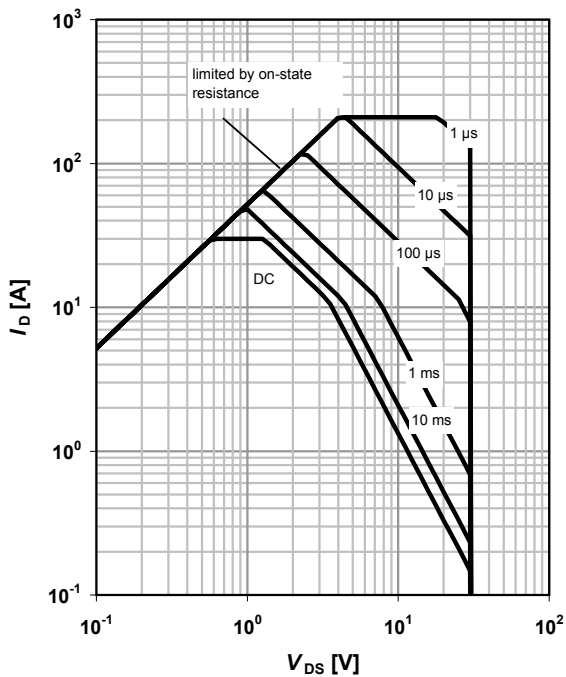
$$I_D = f(T_c); V_{GS} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_c = 25 \text{ °C}; D = 0$$

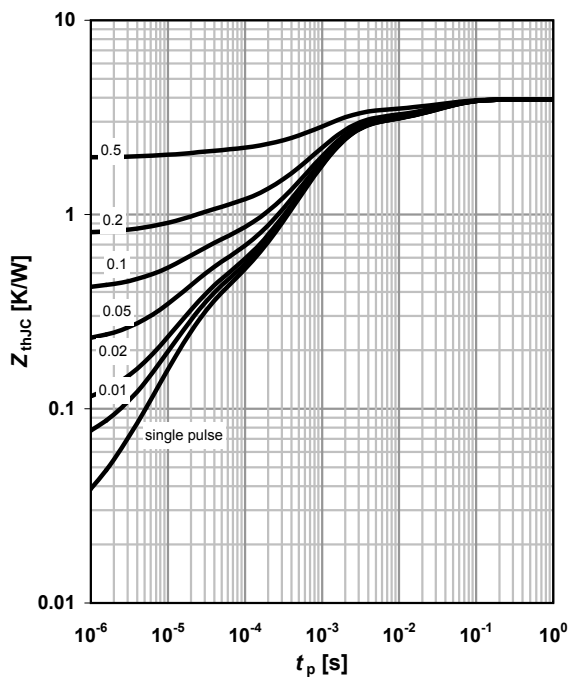
parameter: t_p



4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

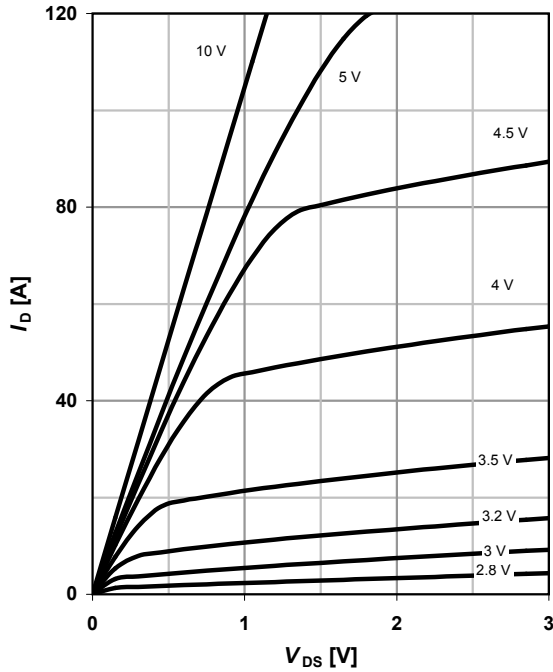
parameter: $D = t_p / T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

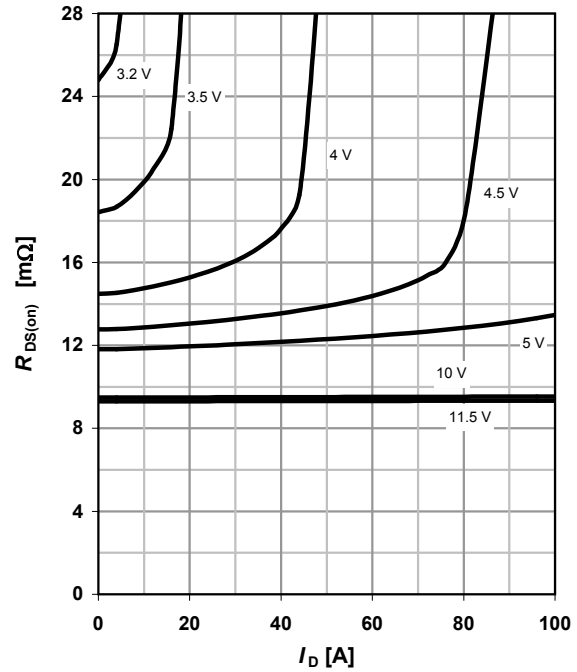
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

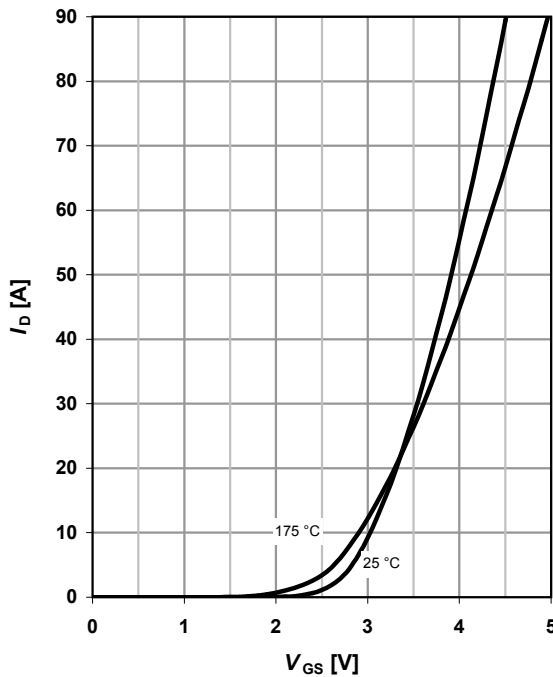
parameter: V_{GS}



7 Typ. transfer characteristics

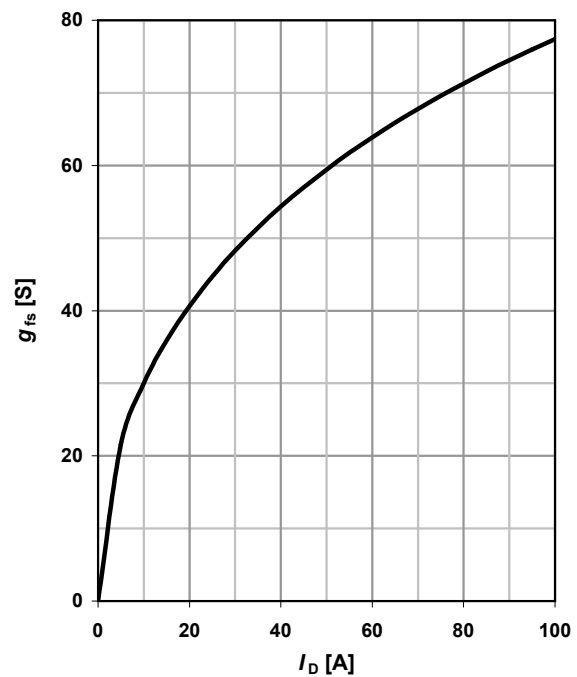
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter: T_j



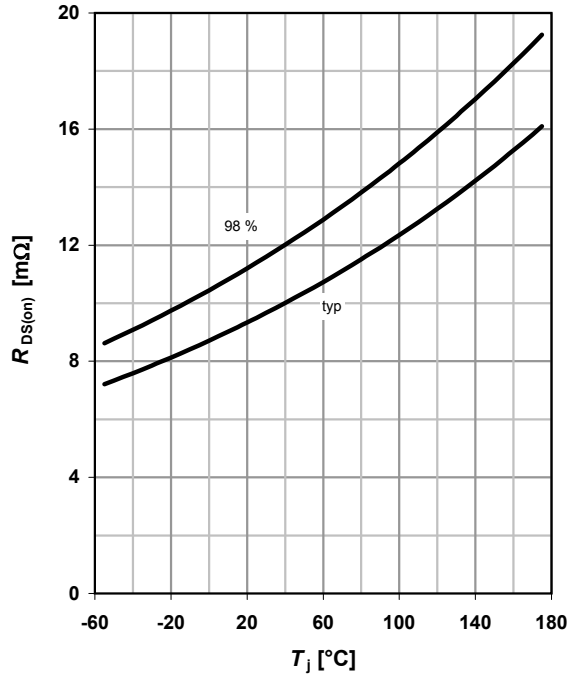
8 Typ. forward transconductance

$g_{fs} = f(I_D); T_j = 25\text{ °C}$



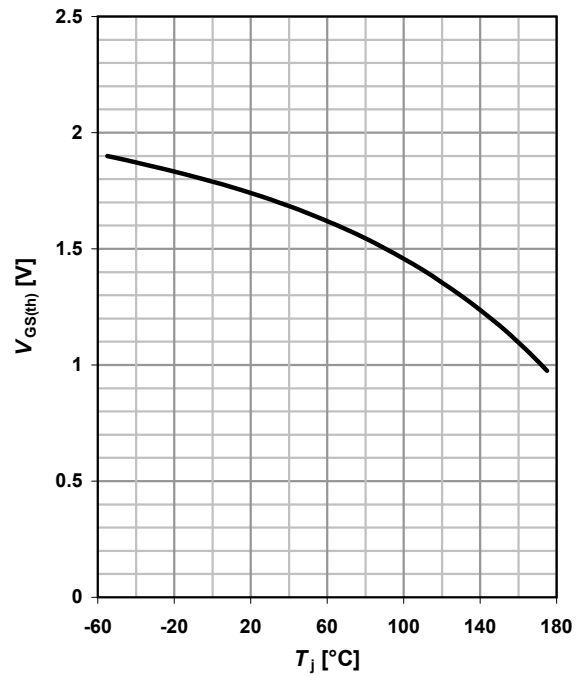
9 Drain-source on-state resistance

$R_{DS(on)} = f(T_j); I_D = 30 \text{ A}; V_{GS} = 10 \text{ V}$



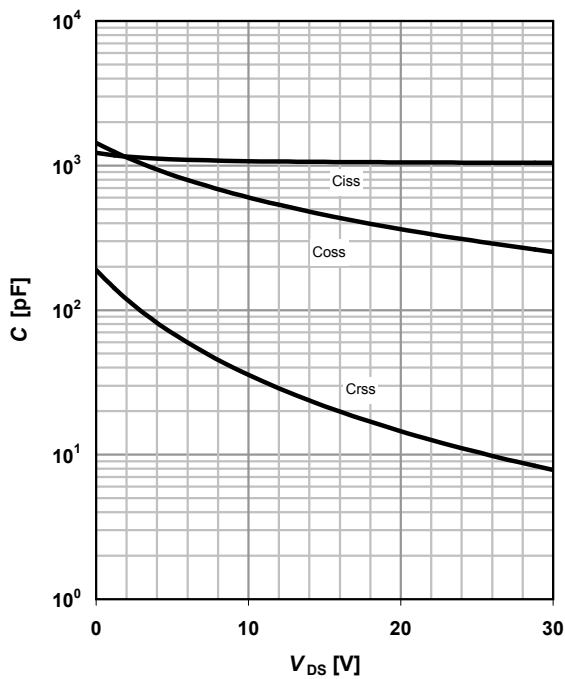
10 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = 250 \mu\text{A}$



11 Typ. capacitances

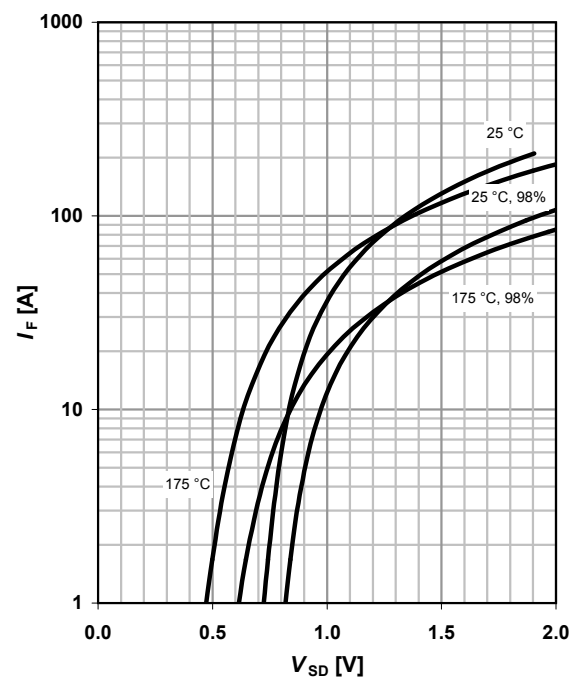
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



12 Forward characteristics of reverse diode

$I_F = f(V_{SD})$

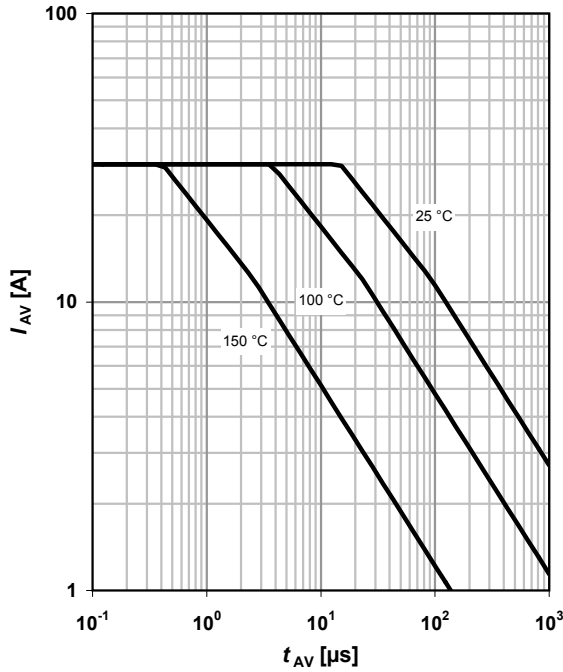
parameter: T_j



13 Avalanche characteristics

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

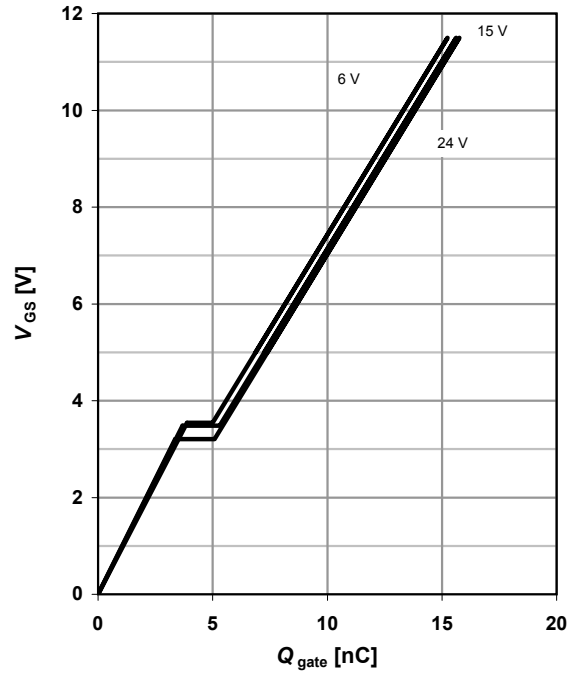
parameter: $T_{j(start)}$



14 Typ. gate charge

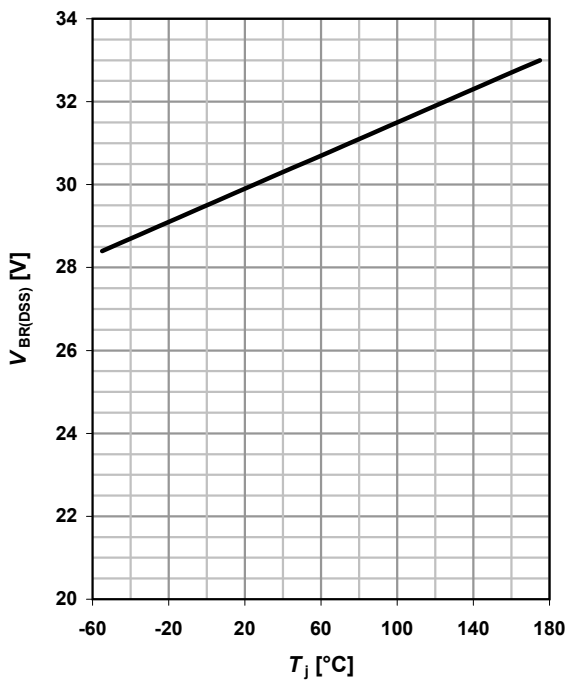
$V_{GS}=f(Q_{gate}); I_D=30 \text{ A pulsed}$

parameter: V_{DD}



15 Drain-source breakdown voltage

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

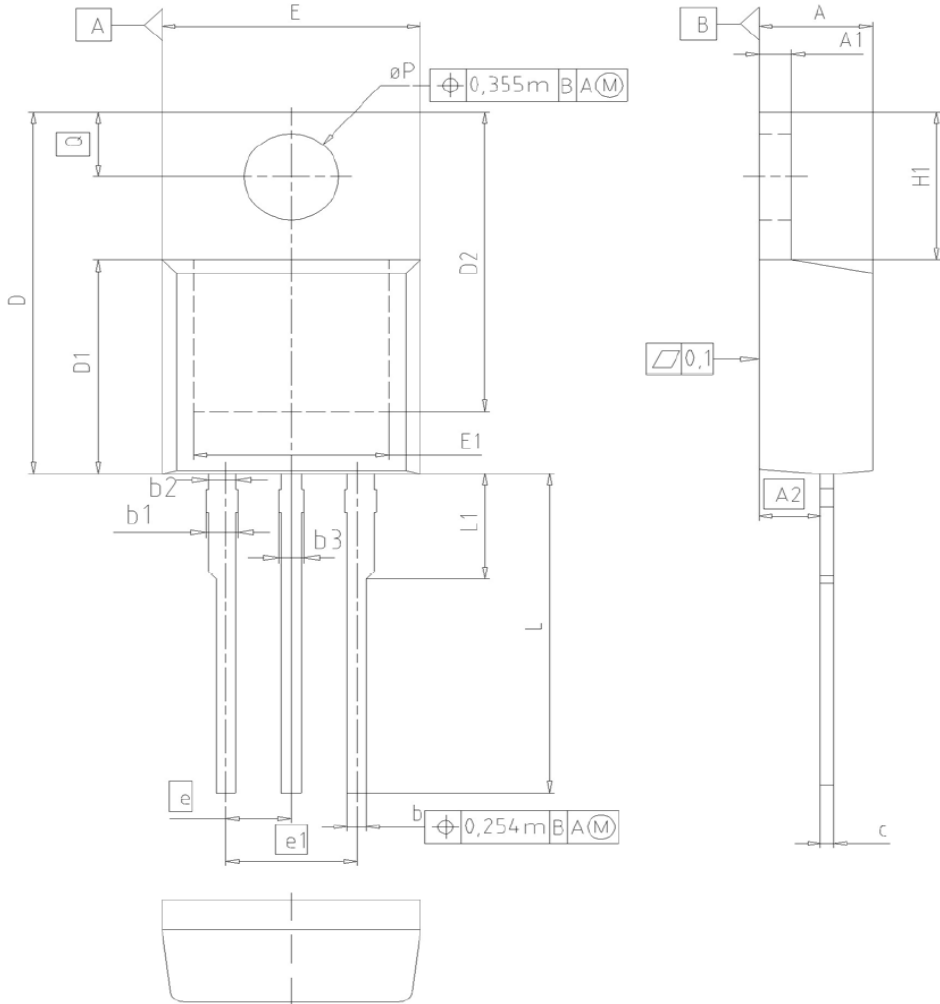


16 Gate charge waveforms



Package Outline

PG-TO220-3-1



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

DOCUMENT NO.
Z8B00003318

SCALE

EUROPEAN PROJECTION

ISSUE DATE
23-08-2007

REVISION
05

Published by

Infineon Technologies AG

81726 München, Germany

© Infineon Technologies AG 2006.

All Rights Reserved.

Attention please!

The information given in this data sheet shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie"). With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.