Octal LNA/VGA/AAF/ADC and Crosspoint Switch

Preliminary Technical Data

AD9271

FEATURES

8 channels of LNA, VGA, AAF, and ADC
Low noise preamplifier (LNA)
- **Input-referred noise = 1.2 nV/√Hz @ 7.5 MHz typical**
- **SPI-programmable gain = 14 dB/15.6 dB/18 dB**
- **Single-ended input; V_{IN} maximum = 400 mV p-p/ 333 mV p-p/250 mV p-p**
- **Dual mode, active input impedance match**
- **Bandwidth (BW) > 70 MHz**
- **Full-scale (FS) output = 2 V p-p diff**

Variable gain amplifier (VGA)
- **Gain range = −6 dB to +24 dB**
- **Linear-in-dB gain control**

Antialiasing filter (AAF)
- **3rd-order Butterworth cutoff**
- **Programmable from 8 MHz to 18 MHz**

Analog-to-digital converter (ADC)
- **12 bits at 10 MSPS to 50 MSPS**
- **SNR = 70 dB**
- **SFDR = 80 dB**
- **Serial LVDS (ANSI-644, IEEE 1596.3 reduced range link)**
- **Data and frame clock outputs**

Includes crosspoint switch to support continuous wave (CW) Doppler
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Low power, 150 mW/channel at 12 bits/40 MSPS (TGC)
60 mW/channel in CW Doppler
Single 1.8 V supply (3.3 V supply for CW Doppler output bias)
Flexible power-down modes
Overload recovery in <10 ns
Fast recovery from low power standby mode, <2 μs
100-pin TQFP

APPLICATIONS

Medical imaging/ultrasound
Automotive radar

GENERAL DESCRIPTION

The AD9271 is designed for low cost, low power, small size, and ease of use. It contains eight channels of a variable gain amplifier (VGA) with low noise preamplifier (LNA); an antialiasing filter (AAF); and a 12-bit, 10 MSPS to 50 MSPS analog-to-digital converter (ADC).

Each channel features a variable gain range of 30 dB, a fully differential signal path, an active input preamplifier termination, a maximum gain of up to 40 dB, and an ADC with a conversion rate of up to 50 MSPS. The channel is optimized for dynamic performance and low power in applications where a small package size is critical.

The LNA has a single-ended-to-differential gain that is selectable through the SPI. The LNA input noise is typically 1.2 nV/√Hz,

FUNCTIONAL BLOCK DIAGRAM

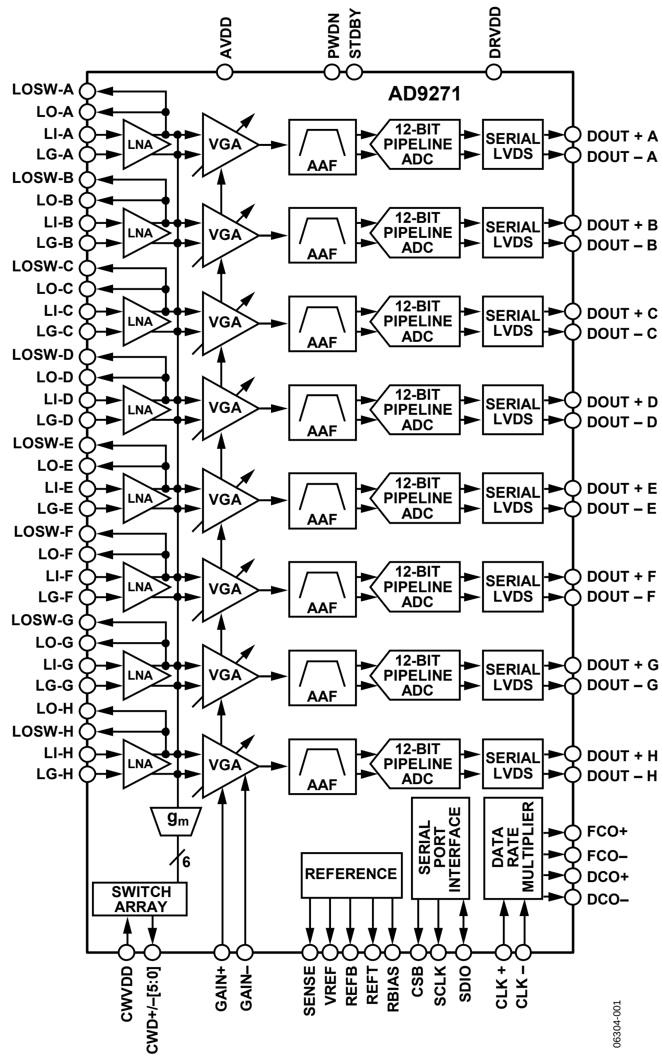

Figure 1.Block Diagram

and the combined input-referred noise of the entire channel is 1.4 nV/√Hz at maximum gain. Assuming a 15 MHz noise bandwidth (NBW) and a 15.6 dB LNA gain, the input SNR is roughly 86 dB. In CW Doppler mode, the LNA output drives a transconductance amp that is switched through an 8 × 6, differential crosspoint switch. The switch is programmable through the SPI.

Rev. PrA
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REVISION HISTORY

x/07—Revision 0: Initial Version

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The AD9271 requires a LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock (DCO) for capturing data on the output and a frame clock (FCO) trigger for signaling a new output byte are provided.

Powering down individual channel is supported to increase battery life for portable applications. There is also a standby mode option that allows quick power-up for power cycling. In CW Doppler operation, the VGA, AAF, and ADC are powered down. The power of the TGC path scales with selectable speed grades.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as a programmable clock, data alignment, and programmable digital test pattern generation. The digital test patterns include built-in fixed patterns, built-in pseudorandom pattern, and custom user-defined test patterns entered via the serial port interface.

Fabricated in an advanced CMOS process, the AD9271 is available in a 14 mm × 14 mm, Pb-free, 100-lead TQFP. It is specified over the industrial temperature range of –40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Small Footprint. Eight channels are contained in a small, space-saving package. Full TGC path, ADC, and crosspoint switch contained within a 100-lead, 16 mm × 16 mm, TQFP.
2. Low power of 150 mW/channel at 40 MSPS.
3. Integrated Crosspoint Switch. This switch allows numerous multichannel configuration options to enable the CW Doppler mode.
4. Ease of Use. A data clock output (DCO) operates up to 300 MHz and supports double data rate operation (DDR).
5. User Flexibility. Serial port interface (SPI) control offers a wide range of flexible features to meet specific system requirements.
6. Integrated Third-Order Antialiasing Filter. This filter is placed between TGC path and ADC and is programmable from 8 MHz to 18 MHz.

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SPECIFICATIONS

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, CWVDD = 3.3 V, 1.0 V internal ADC reference, AIN = 5 MHz, R_S = 50 Ω, LNA gain = 15.6 dB (6), unless otherwise noted.

Table 1.

Parameter[1]	Conditions	AD9271-25 Min	AD9271-25 Typ	AD9271-25 Max	AD9271-40 Min	AD9271-40 Typ	AD9271-40 Max	AD9271-50 Min	AD9271-50 Typ	AD9271-50 Max	Unit
LNA CHARACTERISTICS											
Gain = 5/6/8	Single-ended input to differential output		14/15.6/18			14/15.6/18			14/15.6/18		dB
	Single-ended input to single-ended output		8/9.6/12			8/9.6/12			8/9.6/12		dB
Input Voltage Range, Gain = 5/6/8	LNA output limited to 2 V p-p differential output		400/333/250			400/333/250			400/333/250		mV p-p SE[2]
Input Common Mode			1.4			1.4			1.4		V
Input Resistance	RFB = 200 Ω,		50			50			50		Ω
	RFB = 400 Ω,		100			100			100		Ω
	RFB = ∞		15			15			15		kΩ
Input Capacitance	LI-x		15			15			15		pF
−3 dB Bandwidth			40			60			70		MHz
Input Noise Voltage, Gain = 5/6/8	R_S = 0 Ω, RFB = ∞		1.4/1.4/1.3			1.3/1.2/1.1			1.3/1.2/1.1		nV/√Hz
1 dB Input Compression Point	V_{GAIN} = 0 V		782.6/649.1/508.8			782.6/649.1/508.8			782.6/649.1/508.8		mV p-p
Gain = 5/6/8											
Active Termination Match	Ω, RFB = 200 Ω		6.7			6.7			6.7		dB
Unterminated	RFB = ∞		4.9			4.4			4.2		dB
FULL-CHANNEL (TGC) CHARACTERISTICS											
AAF High-Pass Cutoff	−3 dB		DC/350/700			DC/350/700			DC/350/700		kHz
AAF Low-Pass Cutoff	−3 dB, programmable		1/3 × f_{SAMPLE} (8 to 18)			1/3 × f_{SAMPLE} (8 to 18)			1/3 × f_{SAMPLE} (8 to 18)		MHz
Group Delay Variation	f = 1 MHz to 10 MHz, gain = 0 V to 1 V		±1			±1			±1		ns
Bandwidth Tolerance			±15			±15			±15		%
Input-Referred Noise Voltage, LNA Gain = 5/6/8	RFB = ∞		1.7/1.6/1.5			1.6/1.4/1.3			1.6/1.4/1.2		nV/√Hz
Correlated Noise	No signal		−30			−30			−30		dB
Output Offset	AAF high-pass = 700 kHz		TBD			TBD			TBD		LSB
Signal-to-Noise Ratio (SNR)											
F_{IN} = 5 MHz at −7 dBFS	GAIN pin = 0 V		65			65			65		dBFS

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Parameter[1]	Conditions	AD9271-25 Min	AD9271-25 Typ	AD9271-25 Max	AD9271-40 Min	AD9271-40 Typ	AD9271-40 Max	AD9271-50 Min	AD9271-50 Typ	AD9271-50 Max	Unit
F_{IN} = 5 MHz at −1 dBFS	GAIN pin = 1 V		65			65			65		dBFS
Harmonic Distortion											
Second Harmonic, F_{IN} = 5 MHz at −7 dBFS	GAIN pin = 0 V		−65			−65			−65		dBFS
Second Harmonic, F_{IN} = 5 MHz at −1 dBFS	GAIN pin = 1 V		−65			−65			−65		dBFS
Third Harmonic, F_{IN} = 5 MHz at −7 dBFS	GAIN pin = 0 V		−70			−70			−70		dBFS
Third Harmonic, F_{IN} = 5 MHz at −1 dBFS	GAIN pin = 1 V		−70			−70			−70		dBFS
Two-Tone IMD3 (2 × F1 − F2) Distortion	GAIN pin = 1 V		−65			−65			−65		dB
F_{IN1} = 5.0 MHz at −1 dBFS											
F_{IN2} = 5.1 MHz at −26 dBFS											
Channel-to-Channel Crosstalk			−70			−70			−70		dB
Channel-to-Channel Crosstalk (Overrange Condition)[3]			−70			−70			−70		dB
Overload Recovery	LNA or VGA		10			10			10		ns
GAIN ACCURACY											
Absolute Gain Error	0 < V_{GAIN} < 0.1 V	−1.0	+0.5	+2.0	−1.0	+0.5	+2.0	−1.0	+0.5	+2.0	dB
	0.1 V < V_{GAIN} < 0.9 V, 1σ	−1.0	±0.3	+1.0	−1.0	±0.3	+1.0	−1.0	±0.3	+1.0	dB
	0.9 V < V_{GAIN} < 1 V	−2.0	-0.5	+1.0	−2.0	-0.5	+1.0	−2.0	-0.5	+1.0	dB
Channel-to-Channel Matching	0.1 V < V_{GAIN} < 0.9 V			1			1			1	dB
GAIN CONTROL INTERFACE											
Normal Operating Range		0		1	0		1	0		1	V
Gain Range	0 V to 1 V	10.6		40.6	10.6		40.6	10.6		40.6	dB
Scale Factor			32			32			32		dB/V
Response Time	30 dB change		350			350			350		ns
CW DOPPLER MODE											
Transconductance, LNA Gain = 5/6/8			10/12/16			10/12/16			10/12/16		mA/V
Common Mode	CW Doppler output pins	1.5		3.6	1.5		3.6	1.5		3.6	V
Input-Referred Noise Voltage, LNA Gain = 5/6/8	R_S = 0 Ω, RFB = ∞		1.8 /1.7/1.5			1.7 /1.5/1.4			1.7 /1.5/1.3		nV/√Hz
Output DC Bias	Per channel		2.4			2.4			2.4		mA
Maximum Output Swing	Per channel		±2			±2			±2		mA p-p
POWER SUPPLY											
AVDD		1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V

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Parameter[1]	Conditions	AD9271-25			AD9271-40			AD9271-50			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DRVDD		1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
CWVDD		3.0	3.3	3.6	3.0	3.3	3.6	3.0	3.3	3.6	
I_{AVDD}	Full-channel mode		500			622			746		mA
	CW Doppler mode with four channels enabled		136			160			170		mA
I_{DRVDD}			49			49			49		mA
Total Power Dissipation (Including Output Drivers)	Full-channel mode		984			1200			1400		mW
	CW Doppler mode with four channels enabled		192			216			224		mW
Power-Down Dissipation										10	mW
Standby Power Dissipation			65			65			65		mW
Power Supply Rejection Ratio (PSRR)			1			1			1		mV/V
ADC RESOLUTION			12			12			12		Bits

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Parameter[1]	Conditions	AD9271-25			AD9271-40			AD9271-50			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ADC REFERENCE											
Output Voltage Error (VREF = 1 V)			±2			±2			±2		mV
Load Regulation @ 1.0 mA (VREF = 1 V)			3			3			3		mV
Input Resistance			6			6			6		kΩ

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] SE = single ended.
[3] The overrange condition is specified as being 6 dB more than the full-scale input range.

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DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, CWVDD = 3.3 V, 400 m V p-p differential input, 1.0 V internal ADC reference, AIN = −0.5 dBFS, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	250			mV p-p
Input Common-Mode Voltage	Full		1.2		V
Input Resistance (Differential)	25°C		20		kΩ
Input Capacitance	25°C		1.5		pF
LOGIC INPUTS (PDWN, STBY, SCLK)					
Logic 1 Voltage	Full	1.2		3.6	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		0.5		pF
LOGIC INPUT (CSB)					
Logic 1 Voltage	Full	1.2		3.6	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		70		kΩ
Input Capacitance	25°C		0.5		pF
LOGIC INPUT (SDIO)					
Logic 1 Voltage	Full	1.2		DRVDD + 0.3	V
Logic 0 Voltage	Full	0		0.3	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		2		pF
LOGIC OUTPUT (SDIO)[3]					
Logic 1 Voltage (I_{OH} = 800 μA)	Full		1.79		V
Logic 0 Voltage (I_{OL} = 50 μA)	Full			0.05	V
DIGITAL OUTPUTS (D+, D−), (ANSI-644)[1]					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	247		454	mV
Output Offset Voltage (V_{OS})	Full	1.125		1.375	V
Output Coding (Default)			Offset binary		
DIGITAL OUTPUTS (D+, D−), (Low Power, Reduced Signal Option)[1]					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	150		250	mV
Output Offset Voltage (V_{OS})	Full	1.10		1.30	V
Output Coding (Default)			Offset binary		

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] Specified for LVDS and LVPECL only.
[3] Specified for 13 SDIO pins sharing the same connection.

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SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, CWVDD = 3.3 V, 400 m V p-p differential input, 1.0 V internal ADC reference, AIN = −0.5 dBFS, unless otherwise noted.

Table 3.

Parameter[1]	Temp	Min	Typ	Max	Unit
CLOCK[2]					
Maximum Clock Rate	Full	50			MSPS
Minimum Clock Rate	Full			10	MSPS
Clock Pulse Width High (t_{EH})	Full		10.0		ns
Clock Pulse Width Low (t_{EL})	Full		10.0		ns
OUTPUT PARAMETERS[2, 3]					
Propagation Delay (t_{PD})	Full	1.5	2.3	3.1	ns
Rise Time (t_R) (20% to 80%)	Full		300		ps
Fall Time (t_F) (20% to 80%)	Full		300		ps
FCO Propagation Delay (t_{FCO})	Full	1.5	2.3	3.1	ns
DCO Propagation Delay (t_{CPD})[4]	Full		t_{FCO} + (t_{SAMPLE}/24)		ns
DCO to Data Delay (t_{DATA})[4]	Full	(t_{SAMPLE}/24) – 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	ps
DCO to FCO Delay (t_{FRAME})[4]	Full	(t_{SAMPLE}/24) – 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	ps
Data-to-Data Skew ($t_{DATA-MAX}$ − $t_{DATA-MIN}$)	Full		±50	±200	ps
Wake-Up Time (Standby)	25°C		600		ns
Wake-Up Time (Power-Down)	25°C		375		µs
Pipeline Latency	Full		8		CLK cycles
APERTURE					
Aperture Uncertainty (Jitter)	25°C		<1		ps rms

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] Can be adjusted via the SPI interface.
[3] Measurements were made using a part soldered to FR4 material.
[4] t_{SAMPLE}/24 is based on the number of bits divided by 2, because the delays are based on half duty cycles.

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ADC TIMING DIAGRAMS

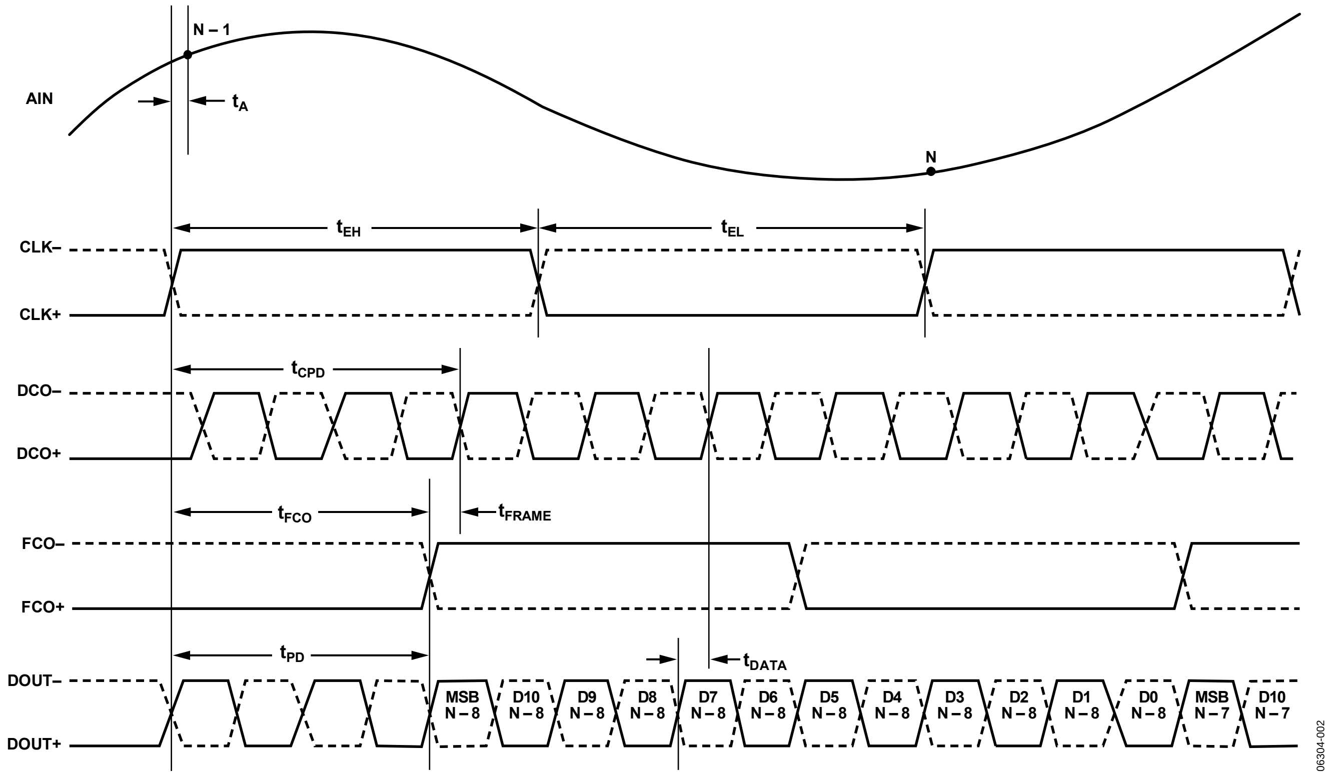

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Figure 2. 12-(Preliminary) Bit Data Serial Stream (Default)

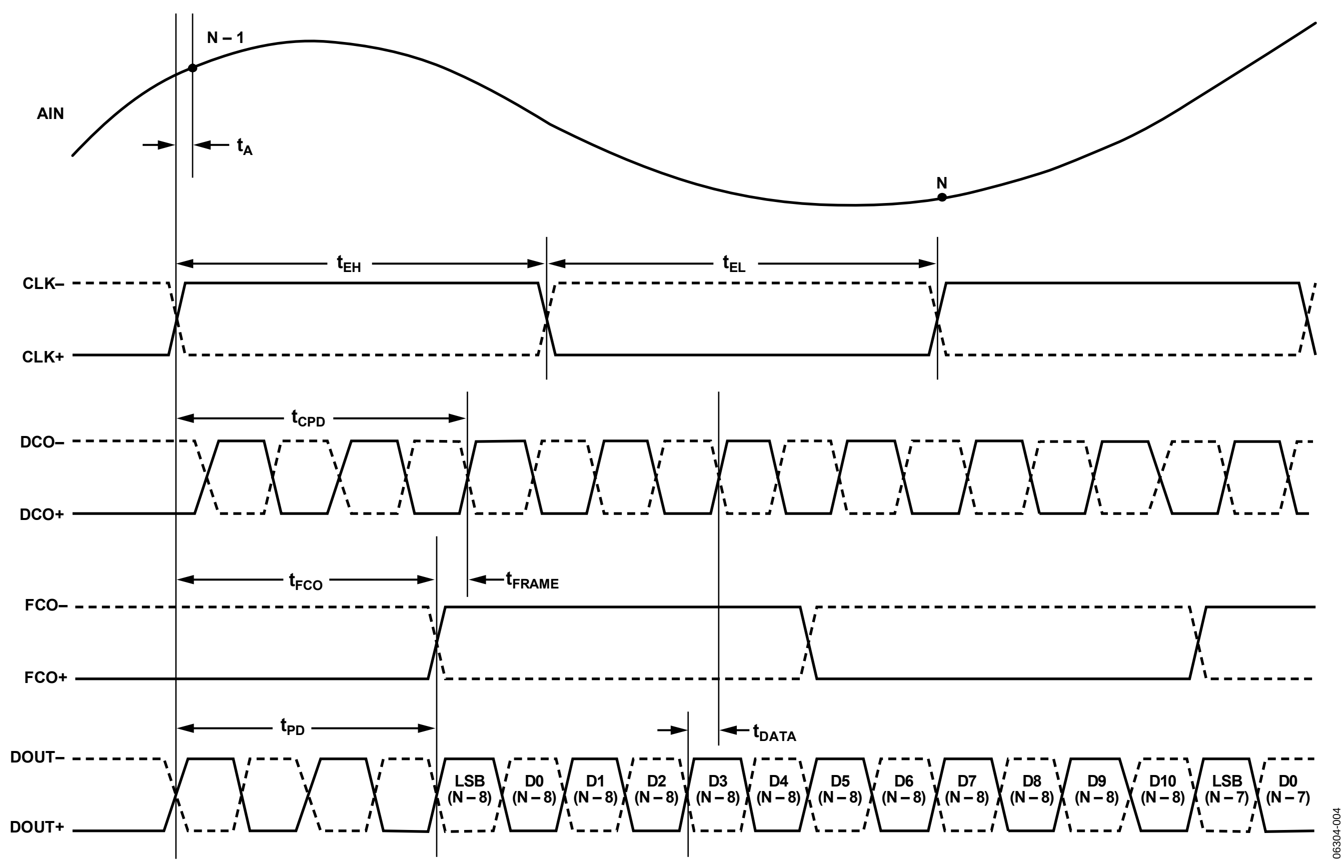

Figure 3. 12-(Preliminary) Bit Data Serial Stream, LSB First

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ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	With Respect To	Rating
ELECTRICAL		
AVDD	GND	−0.3 V to +2.0 V
DRVDD	GND	−0.3 V to +2.0 V
CWVDD	GND	−0.3 V to +3.9 V
GND	GND	−0.3 V to +0.3 V
AVDD	DRVDD	−2.0 V to +2.0 V
Digital Outputs (DOUT+, DOUT−, DCO+, DCO−, FCO+, FCO−)	GND	−0.3 V to +2.0 V
CLK+, CLK−	GND	−0.3 V to +3.9 V
LI-x	LG-x	−0.3 V to +2.0 V
LO-x	LG-x	−0.3 V to +2.0 V
LOSW-x	LG-x	−0.3 V to +2.0 V
CWDx−, CWDx+	GND	−0.3 V to +2.0 V
SDIO, GAIN+,GAIN−	GND	−0.3 V to +2.0 V
PDWN, STBY, SCLK, CSB	GND	−0.3 V to +3.9 V
REFT, REFB, RBIAS	GND	−0.3 V to +2.0 V
VREF, SENSE	GND	−0.3 V to +2.0 V
ENVIRONMENTAL		
Operating Temperature Range (Ambient)		−40°C to +85°C
Maximum Junction Temperature		150°C
Lead Temperature (Soldering, 10 sec)		300°C
Storage Temperature Range (Ambient)		−65°C to +150°C

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Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

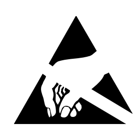
THERMAL IMPEDANCE

Table 5.

Air Flow Velocity (m/s)	θ_{JA}[1]	θ_{JB}	θ_{JC}
0.0	20.3°C/W		
1.0	14.4°C/W	7.6°C/W	4.7°C/W
2.5	12.9°C/W		

[1] θ_{JA} for a 4-layer PCB with solid ground plane (simulated). Exposed pad soldered to PCB.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

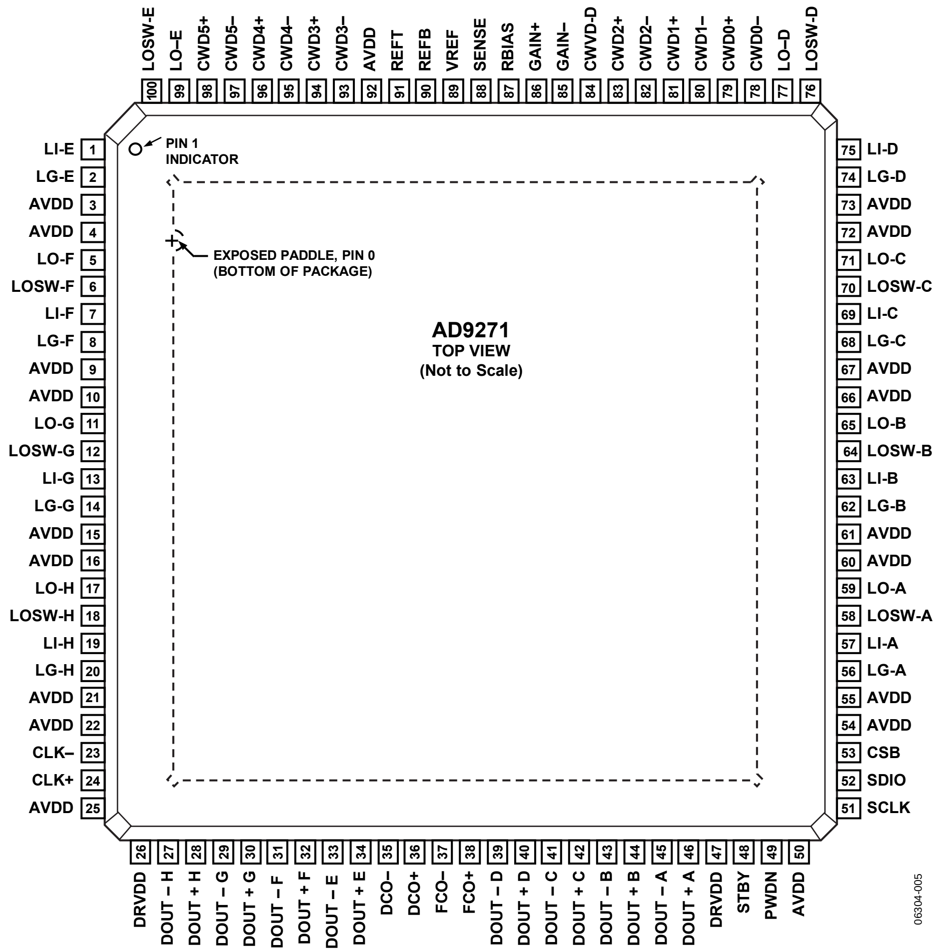

Figure 4. 100-Lead TQFP

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Table 6. Pin Function Descriptions

Pin No.	Name	Description
0	GND	Ground (Exposed paddle should be tied to a quiet analog ground)
3, 4, 9, 10, 15, 16, 21, 22, 25, 50, 54, 55, 60, 61, 66, 67, 72, 73,92	AVDD	1.8 V Analog Supply
26, 47	DRVDD	1.8 V Digital Output Driver Supply
84	CWVDD	3.3 V Analog Supply
1	LI-E	LNA Analog Input for Channel E
2	LG-E	LNA Ground for Channel E
5	LO-F	LNA Analog Output for Channel F
6	LOSW-F	LNA Analog Output Complement for Channel F
7	LI-F	LNA Analog Input for Channel F
8	LG-F	LNA Ground for Channel F
11	LO-G	LNA Analog Output for Channel G
12	LOSW-G	LNA Analog Output Complement for Channel G
13	LI-G	LNA Analog Input for Channel G
14	LG-G	LNA Ground for Channel G

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Pin No.	Name	Description
17	LO-H	LNA Analog Output for Channel H
18	LOSW-H	LNA Analog Output Complement for Channel H
19	LI-H	LNA Analog Input for Channel H
20	LG-H	LNA Ground for Channel H
23	CLK−	Clock Input Complement
24	CLK+	Clock Input True
27	DOUT − H	ADC H Digital Output Complement
28	DOUT + H	ADC H True Digital Output True
29	DOUT − G	ADC C Digital Output Complement
30	DOUT + G	ADC C True Digital Output
31	DOUT − F	ADC B Digital Output Complement
32	DOUT + F	ADC B True Digital Output True
33	DOUT − E	ADC A Digital Output Complement
34	DOUT + E	ADC A True Digital Output True
35	DCO−	Frame Clock Digital Output Complement
36	DCO+	Frame Clock Digital Output True
37	FCO−	Frame Clock Digital Output Complement
38	FCO+	Frame Clock Digital Output True
39	DOUT − D	ADC H Digital Output Complement
40	DOUT + D	ADC H True Digital Output True
41	DOUT − C	ADC C Digital Output Complement
42	DOUT + C	ADC C True Digital Output
43	DOUT − B	ADC B Digital Output Complement
44	DOUT + B	ADC B True Digital Output True
45	DOUT − A	ADC A Digital Output Complement
46	DOUT + A	ADC A True Digital Output True
48	STDBY	Standby Power Down
49	PDWN	Full Power Down
51	SCLK	Serial Clock
52	SDIO	Serial Data Input/Output
53	CSB	Chip Select Bar
56	LG-A	LNA Ground for Channel A
57	LI-A	LNA Analog Input for Channel A
58	LOSW-A	LNA Analog Output Complement for Channel A
59	LO-A	LNA Analog Output for Channel A
62	LG-B	LNA Ground for Channel B
63	LI-B	LNA Analog Input for Channel B
64	LOSW-B	LNA Analog Output Complement for Channel B
65	LO-B	LNA Analog Output for Channel B
68	LG-C	LNA Ground for Channel C
69	LI-C	LNA Analog Input for Channel C
70	LOSW-C	LNA Analog Output Complement for Channel C
71	LO-C	LNA Analog Output for Channel C
74	LG-D	LNA Ground for Channel D
75	LI-D	LNA Analog Input for Channel D
76	LOSW-D	LNA Analog Output Complement for Channel D
77	LO-D	LNA Analog Output for Channel D
78	CWD0−	CW Doppler Output Complement for Channel 0
79	CWD0+	CW Doppler Output True for Channel 0
80	CWD1−	CW Doppler Output Complement for Channel 1
81	CWD1+	CW Doppler Output True for Channel 1
82	CWD2−	CW Doppler Output Complement for Channel 2
83	CWD2+	CW Doppler Output True for Channel 2

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Pin No.	Name	Description
85	GAIN−	GAIN Control Voltage Input Complement
86	GAIN+	GAIN Control Voltage Input True
87	RBIAS	External resistor sets the internal ADC core bias current
88	SENSE	Reference Mode Selection
89	VREF	Voltage Reference Input/Output
90	REFB	Differential Reference (Negative)
91	REFT	Differential Reference (Positive)
93	CWD3−	CW Doppler Output Complement for Channel 3
93	CWD3+	CW Doppler Output True for Channel 3
95	CWD4−	CW Doppler Output Complement for Channel 4
96	CWD4+	CW Doppler Output True for Channel 4
97	CWD5−	CW Doppler Output Complement for Channel 5
98	CWD5+	CW Doppler Output True for Channel 5
99	LO-E	LNA Analog Output for Channel E
100	LOSW-E	LNA Analog Output Complement for Channel E

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EQUIVALENT CIRCUITS

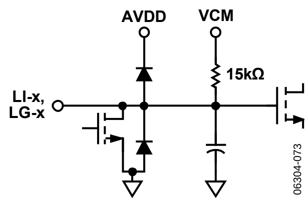

Figure 5. Equivalent LNA Input Circuit

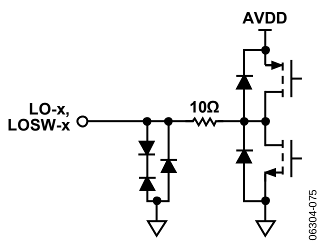

Figure 6. Equivalent LNA Output Circuit

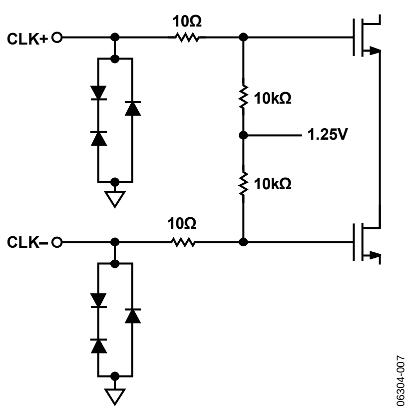

Figure 7. Equivalent Clock Input Circuit

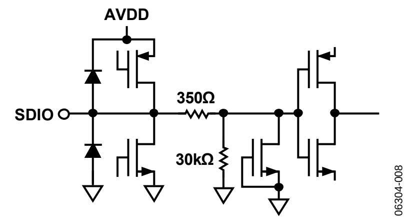

Figure 8. Equivalent SDIO Input Circuit

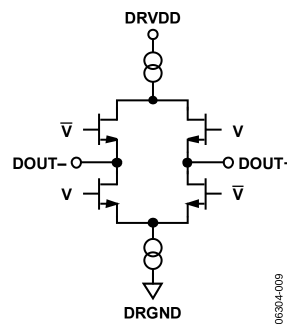

Figure 9. Equivalent Digital Output Circuit

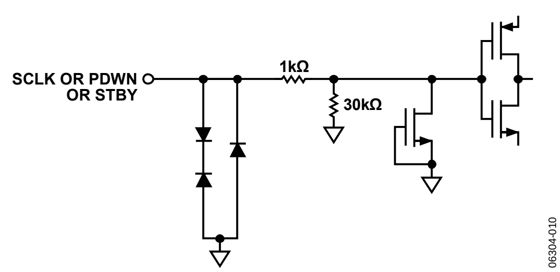

Figure 10. Equivalent SCLK Input Circuit

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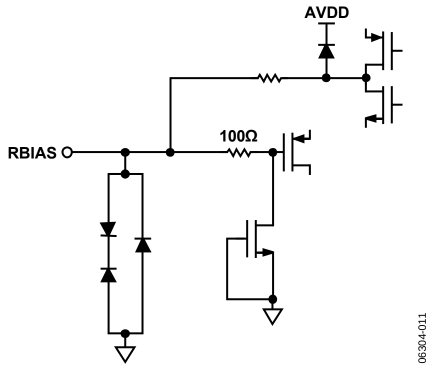

Figure 11. Equivalent RBIAS Circuit

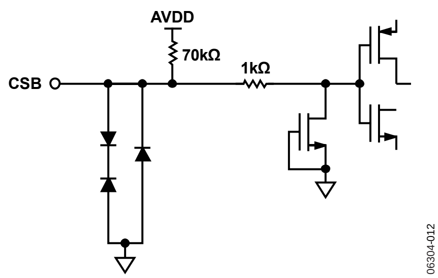

Figure 12. Equivalent CSB Input Circuit

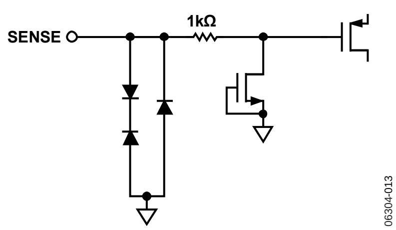

Figure 13. Equivalent SENSE Circuit

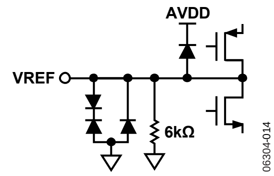

Figure 14. Equivalent VREF Circuit

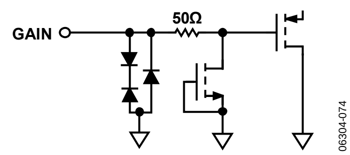

Figure 15. Equivalent GAIN Input Circuit

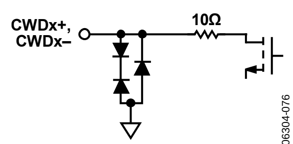

Figure 16. Equivalent CWD Output Circuit

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TYPICAL PERFORMANCE CHARACTERISTICS

(f_{SAMPLE} = 50 MSPS, AIN = 5 MHz, LPF = 1/3 × f_{SAMPLE}, LNA gain = 6×)

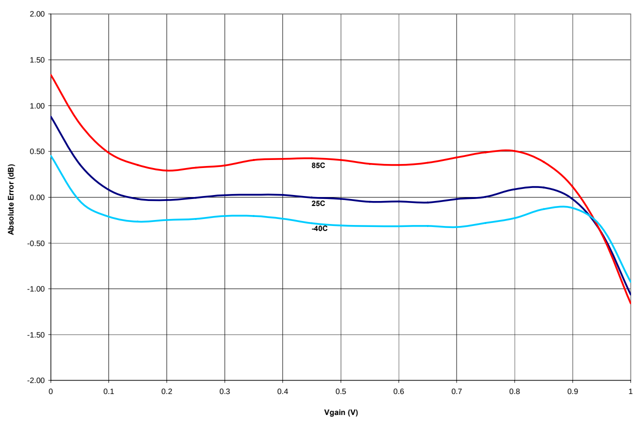

Figure 17. Absolute Gain Error vs. V_{GAIN} at Three Temperatures

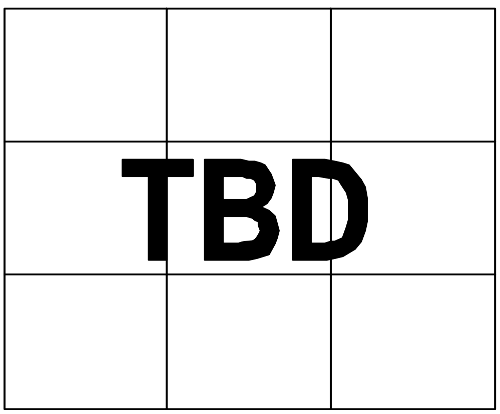

Figure 18. Gain Error Histogram

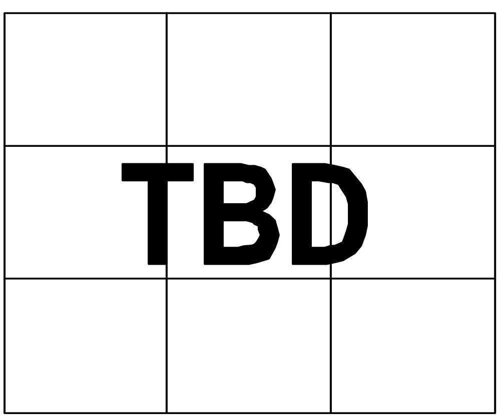

Figure 19. Gain Match Histogram for V_{GAIN} = 0.2 V and 0.7 V

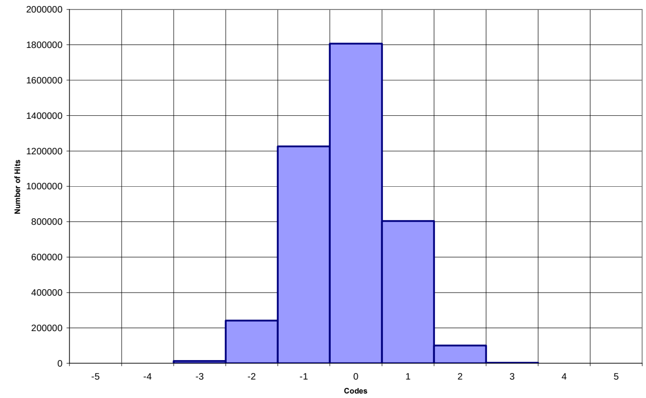

Figure 20. Output-Referred Noise Histogram with Gain Pin at 0.0V, AD9271-50

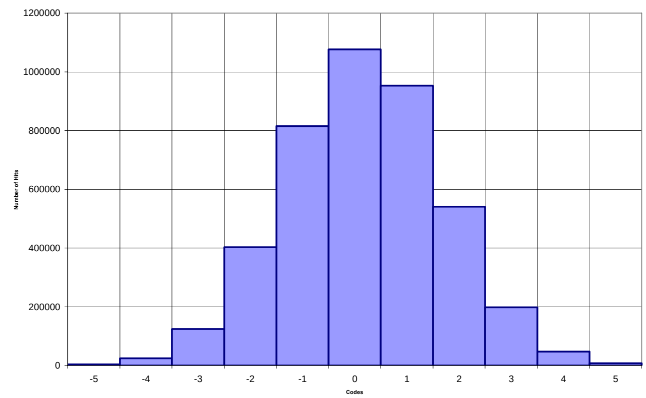

Figure 21. Output-Referred Noise Histogram with Gain Pin at 1.0V, AD9271-50

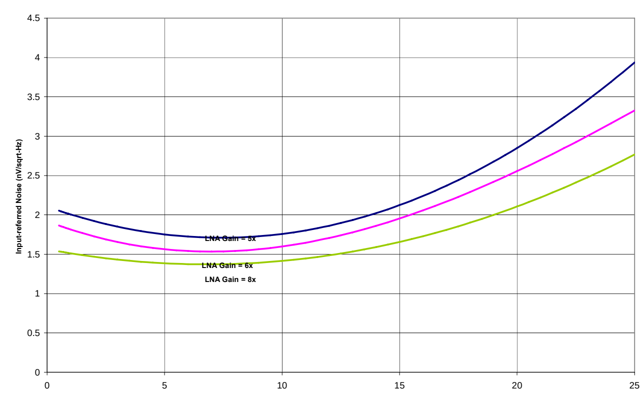

Figure 22. Short-Circuit, Input-Referred Noise vs. Frequency

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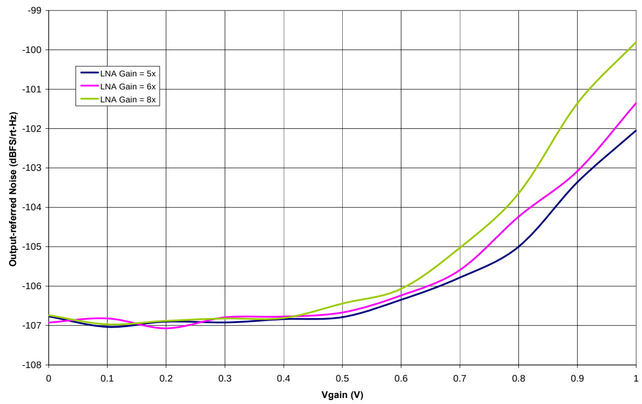

Figure 23. Short-Circuit, Output-Referred Noise vs. V_{GAIN}

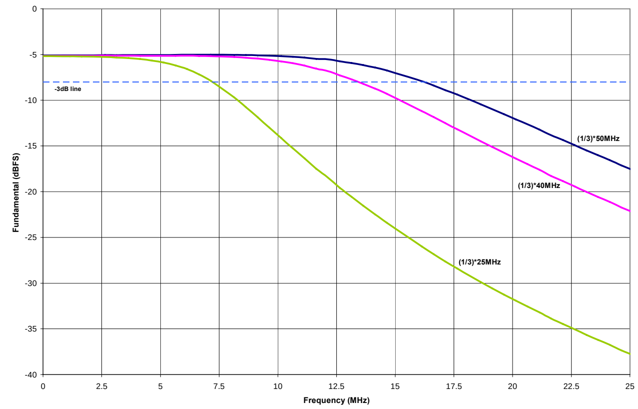

Figure 26. Antialiasing Filter (AAF) Pass-Band Response

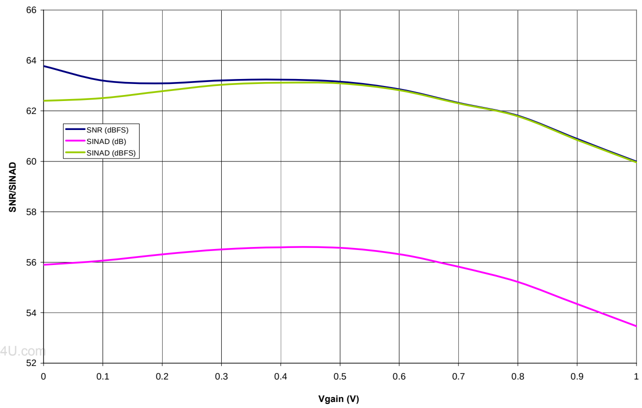

Figure 24. SNR/SINAD vs. Gain

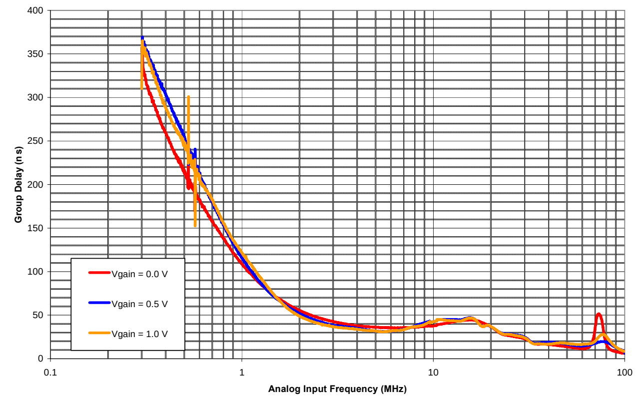

Figure 27. Antialiasing Filter (AAF) Group Delay Response

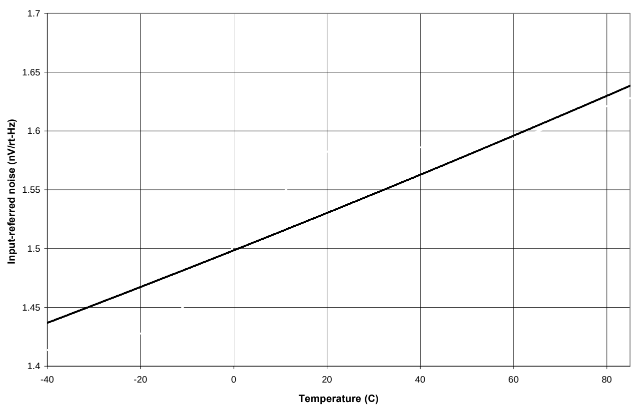

Figure 25. Short-Circuit, Input-Referred Noise vs. Temperature

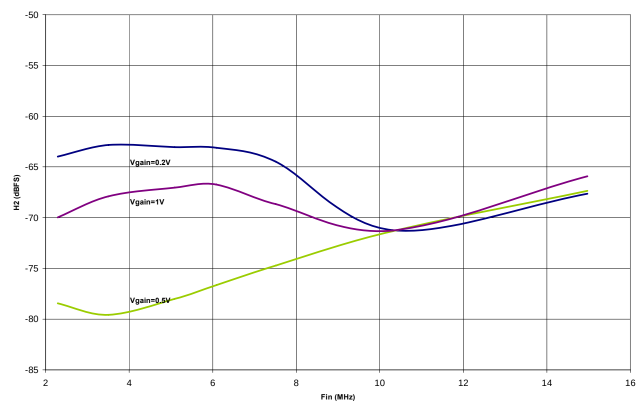

Figure 28. Second-Order Harmonic Distortion vs. Frequency

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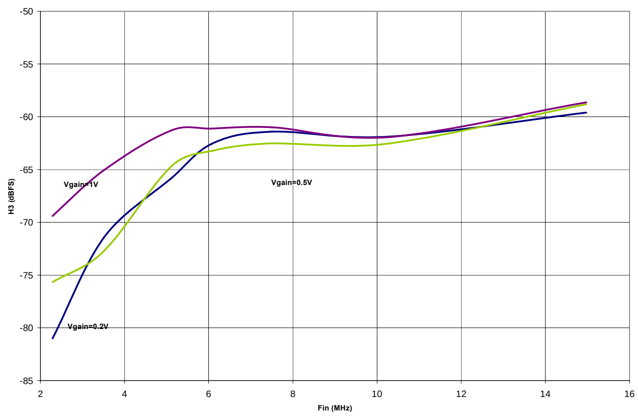

Figure 29. Third-Order Harmonic Distortion vs. Frequency

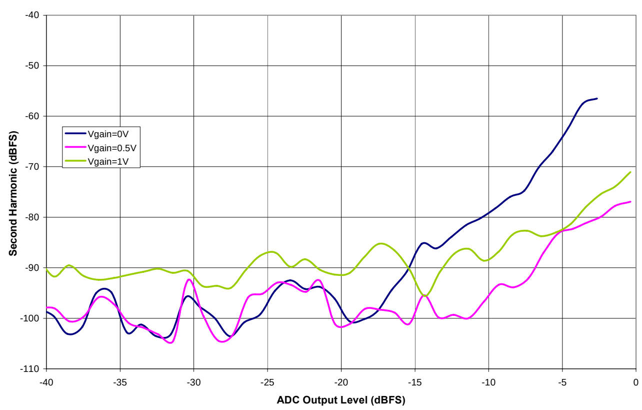

Figure 30. Second-Order Harmonic Distortion vs. ADC Output Level

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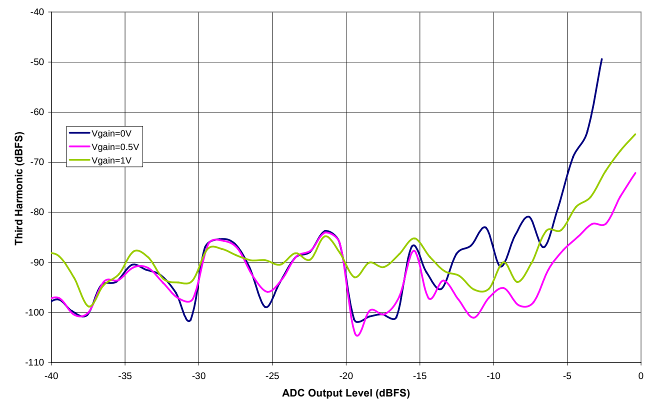

Figure 31. Third-Order Harmonic Distortion vs. ADC Output Level

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THEORY OF OPERATION

ULTRASOUND

The primary application for the AD9271 is medical ultrasound. Figure 32 shows a simplified block diagram of an ultrasound system. A critical function of an ultrasound system is the time gain control (TGC) compensation for physiological signal attenuation. Because the attenuation of ultrasound signals is exponential with respect to distance (time), a linear-in-dB VGA is the optimal solution.

Key requirements in an ultrasound signal chain are very low noise, active input termination, fast overload recovery, low power, and differential drive to an ADC. Because ultrasound machines use beam-forming techniques requiring large binary-weighted numbers (for example, 32 to 512) of channels, the lowest power at the lowest possible noise is of key importance.

Most modern machines use digital beam forming. In this technique, the signal is converted to digital format immediately following the TGC amplifier; beam forming is done digitally.

The ADC resolution of 12 bits with up to 50 MSPS sampling satisfies the requirements of both general-purpose and high-end systems.

Power consumption and low cost are of primary importance in low-end and portable ultrasound machines, and the AD9271 is designed for these criteria.

For additional information regarding ultrasound systems, refer to "How Ultrasound System Considerations Influence Front-End Component Choice," *Analog Dialogue*, Volume 36, Number 3, May–July 2002.

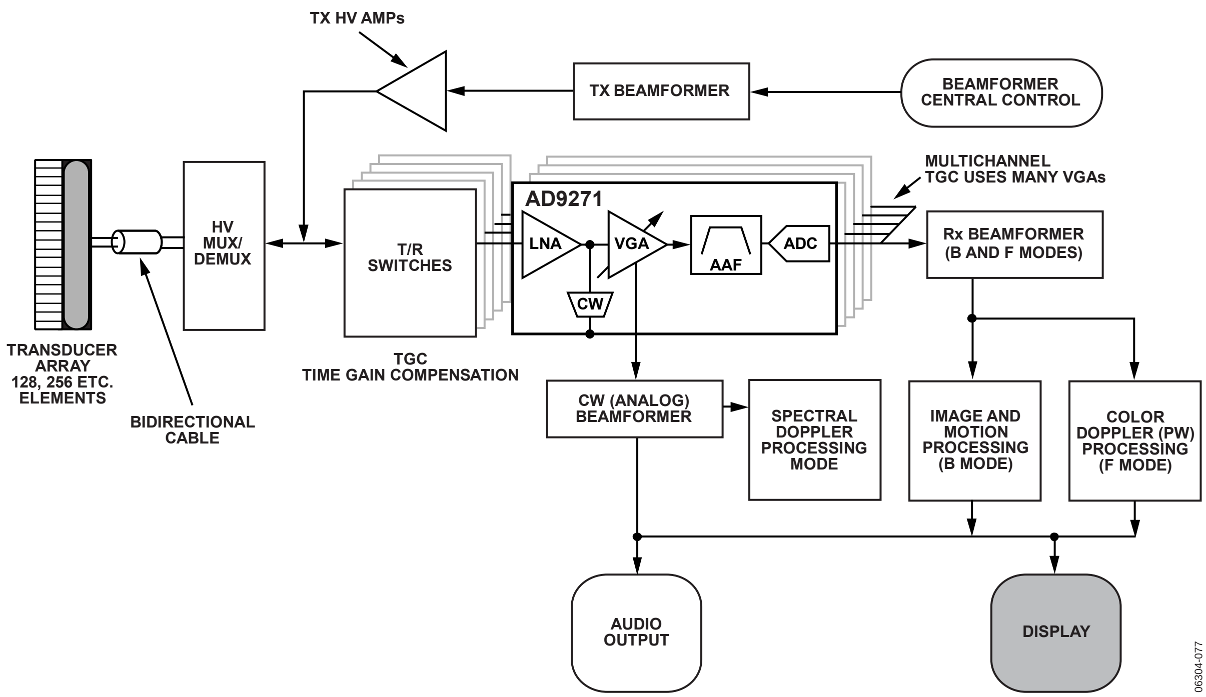

Figure 32. Simplified Ultrasound System Block Diagram

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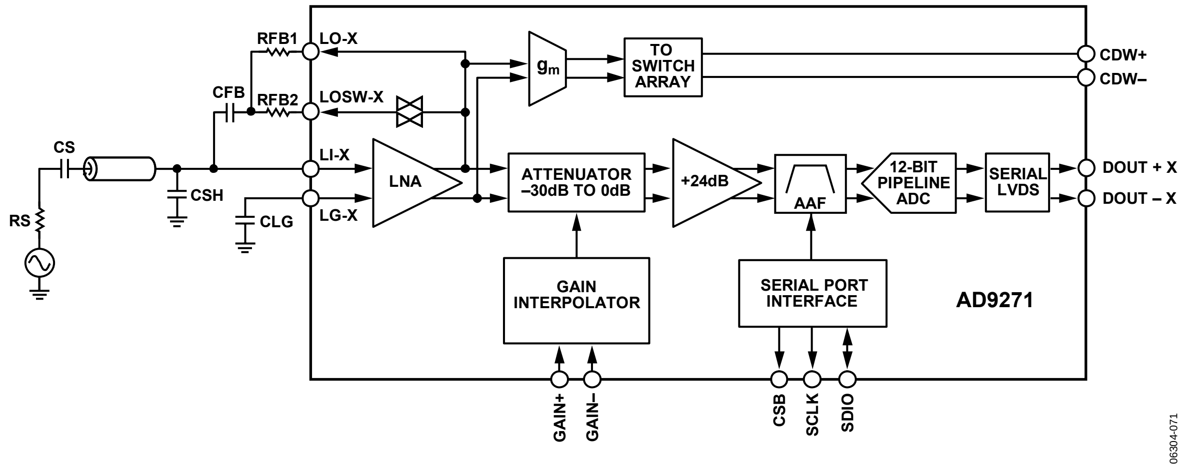

Figure 33. Simplified Block Diagram of Single Channel

CHANNEL OVERVIEW

Each channel contains both a TGC and CW Doppler signal path. Common to both signal paths, the LNA provides user-adjustable input impedance termination. The CW Doppler path includes a transconductance amplifier and crosspoint switch. The TGC path includes a differential X-AMP® VGA, an antialiasing filter, and an ADC. Figure 33 shows a simplified block diagram with external components.

The signal path is fully differential throughout to maximize signal swing and reduce even-order distortion; however, the LNA is designed to be driven from a single-ended signal source.

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Low Noise Amplifier (LNA)

Good noise performance relies on a proprietary ultralow noise LNA at the beginning of the signal chain, which minimizes the noise contribution in the following VGA. Active impedance control optimizes noise performance for applications that benefit from input impedance matching.

A simplified schematic of the LNA is shown in Figure 34. LI-x is capacitively coupled to the source. An on-chip bias generator establishes dc input bias voltages of around 1.4 V and centers the output common-mode levels at 0.9 V (VDD/2). A capacitor, C_{LG}, of the same value as the input coupling capacitor, C_S, is connected from the LG-x pin to ground.

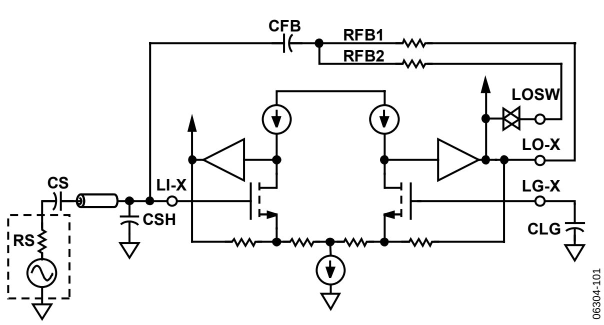

Figure 34. Simplified LNA Schematic

The LNA supports differential output voltages as high as 2 V p-p with positive and negative excursions of ±0.5 V from a common-mode voltage of 0.9 V. The LNA differential gain sets the maximum input signal before saturation. One of three gains is set through the SPI. The corresponding input full-scale for the gain settings of 5, 6, or 8 is 400 mV p-p, 333 mV p-p, and 250 mV p-p, respectively. Overload protection ensures quick recovery time from large input voltages. Because the inputs are capacitively coupled to a bias voltage near midsupply, very large inputs can be handled without interacting with the ESD protection.

Low value feedback resistors and the current-driving capability of the output stage allow the LNA to achieve a low input-referred noise voltage of 1.2 nV/√Hz. This is achieved with a current consumption of only 16 mA per channel (30 mW). On-chip resistor matching results in precise single-ended gains critical for accurate impedance control. The use of a fully differential topology and negative feedback minimizes distortion. Low HD2 is particularly important in second harmonic ultrasound imaging applications. Differential signaling enables smaller swings at each output, further reducing third-order distortion.

Active Impedance Matching

The LNA consists of a single-ended voltage gain amplifier with differential outputs and the negative output externally available. For example, with a fixed gain of 6 (15.6 dB), an active input termination is synthesized by connecting a feedback resistor between the negative output pin, LO-x, and the positive input pin, LI-x. This technique is well known and results in the input resistance shown in Equation 2, where A/2 is the single-ended gain or the gain from the LI-x inputs to the LO-x outputs.

$$R_{IN} = \frac{R_{FB}}{(1 + A/2)} \qquad (2)$$

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Because the amplifier has a gain of 6× from its input to its differential output, it is important to note that the gain A/2 is the gain from Pin LI-x to Pin LO-x, and is 6 dB less than the gain of the amplifier, or 9.6 dB (3×). The input resistance is reduced by an internal bias resistor of 15 kΩ in parallel with the source resistance connected to Pin LI-x, with Pin LG-x ac grounded. Equation 3 can be used to calculate the needed R_{FB} for a desired R_{IN}, even for higher values of R_{IN}.

$$R_{IN} = \frac{R_{FB}}{(1+3)} \| 15\,\mathrm{k}\Omega \quad (3)$$

For example, to set R_{IN} to 200 Ω, the value of R_{FB} is 845 Ω. If the simplified equation, Equation 2, is used to calculate R_{IN}, the resulting value is 190 Ω, resulting in a less than 0.1 dB gain error. Factors such as a dynamic source resistance might influence the absolute gain accuracy more significantly. At higher frequencies, the input capacitance of the LNA needs to be considered. The user must determine the level of matching accuracy and adjust R_{FB} accordingly.

The bandwidth (BW) of the LNA is about 70 MHz. Ultimately the BW of the LNA limits the accuracy of the synthesized R_{IN}. For $R_{IN} = R_S$ up to about 200 Ω, the best match is between 100 kHz and 10 MHz, where the lower frequency limit is determined by the size of the ac-coupling capacitors, and the upper limit, by the LNA BW. Furthermore, the input capacitance and R_S limit the BW at higher frequencies.

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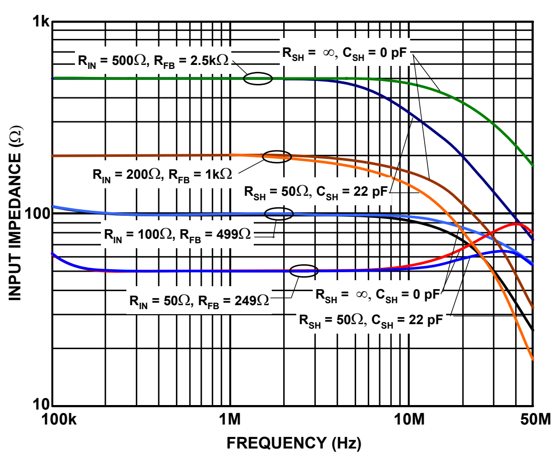

Figure 35. R_{IN} vs. Frequency for Various Values of R_{FB} (Effects of R_{SH} and C_{SH} are Also Shown

Figure 35 shows R_{IN} vs. frequency for various values of R_{FB}. Note that at the lowest value, 50 Ω, R_{IN} peaks at frequencies greater than 10 MHz. This is due to the BW roll-off of the LNA as mentioned earlier.

However, as can be seen for larger R_{IN} values, parasitic capacitance starts rolling off the signal BW before the LNA can produce peaking. C_{SH} further degrades the match; therefore, C_{SH} should not be used for values of R_{IN} that are greater than 100 Ω. Table 7 lists the recommended values for R_{FB} and C_{SH} in terms of R_{IN}.

C_{FB} is needed in series with R_{FB} because the dc levels at Pin LO-x and Pin LI-x are unequal.

Table 7. Active Termination External Component Values

LNA Gain	R_{IN} (Ω)	R_{FB} (Ω)	Minimum C_{SH} (pF)	BW (MHz)
5×	50	175	90	49
6×	50	200	70	59
8×	50	250	50	73
5×	100	350	30	49
6×	100	400	20	59
8×	100	500	10	73
5×	200	700	na	49
6×	200	800	na	49
8×	200	1000	na	49

LNA Noise

The short-circuit noise voltage (input-referred noise) is an important limit on system performance. The short-circuit noise voltage for the LNA is 1.2 nV/√Hz or 1.4 nV/√Hz (at maximum gain), including the VGA noise. These measurements, which are taken without a feedback resistor, provide the basis for calculating the input noise and noise figure performance of the configurations shown in Figure 43. Figure 43 and Figure 44 are simulations of noise figure vs. R_S results using these configurations and an input-referred noise voltage for the VGA of 4 nV/√Hz. Unterminated ($R_{FB} = \infty$) operation exhibits the lowest equivalent input noise and noise figure. Figure 44 shows the noise figure vs. source resistance rising at low R_S—where the LNA voltage noise is large compared with the source noise—and at high R_S due to current noise.

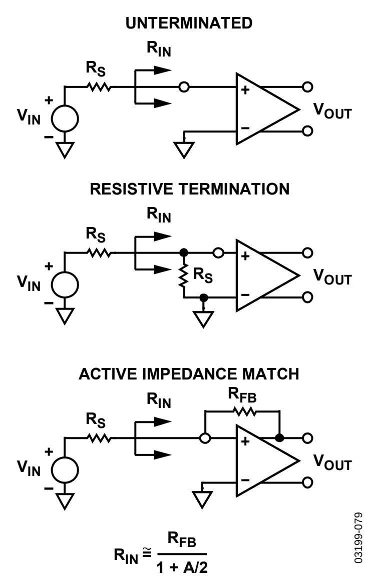

Figure 36. Input Configurations

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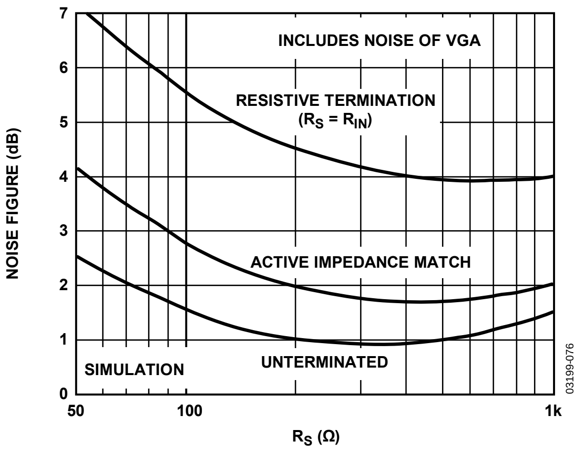

Figure 37. Noise Figure vs. R_S for Resistive, Active Matched and Unterminated Inputs, Gain = 1 V

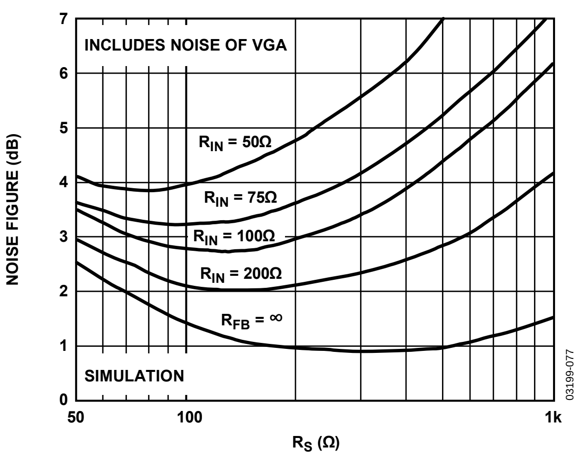

Figure 38. Noise Figure vs. R_S for Various Fixed Values of R_{IN}, Actively Matched, Gain = 1 V.

The primary purpose of input impedance matching is to improve the system transient response. With resistive termination, the input noise increases due to the thermal noise of the matching resistor and the increased contribution of the LNA's input voltage noise generator. With active impedance matching, however, the contributions of both are smaller than they would be for resistive termination by a factor of 1/(1 + *LNA Gain*). Figure 37 shows the relative noise figure (NF) performance. In this graph, the input impedance was swept with R_S to preserve the match at each point. The noise figures for a source impedance of 50 Ω are 7.1 dB, 4.1 dB, and 2.5 dB for the resistive, active, and unterminated configurations, respectively. The noise figures for 200 Ω are 4.6 dB, 2.0 dB, and 1.0 dB, respectively.

Figure 38 shows the NF vs. R_S for various values of R_{IN}, which is helpful for design purposes. The plateau in the NF for actively matched inputs mitigates source impedance variations. For comparison purposes, a preamp with a gain of 15.6 dB and noise spectral density of 1.2 nV/√Hz, combined with a VGA with 4 nV/√Hz, yields a noise figure degradation of approximately 1.5 dB (for most input impedances), which is significantly worse than the AD9271 performance.

INPUT OVERDRIVE

Excellent overload behavior is of primary importance in ultrasound. Both the LNA and VGA have built-in overdrive protection and quickly recover after an overload event.

Input Overload Protection

As with any amplifier, voltage clamping prior to the inputs is highly recommended if the application is subject to high transient voltages.

A block diagram of a simplified ultrasound transducer interface is shown in Figure 39. A common transducer element serves the dual functions of transmitting and receiving ultrasound energy. During the transmitting phase, high voltage pulses are applied to the ceramic elements. A typical transmit/receive (T/R) switch may consist of four high voltage diodes in a bridge configuration. Although the diodes ideally block transmit pulses from the sensitive receiver input, diode characteristics are not ideal, and resulting leakage transients imposed on the LI-x inputs can be problematic.

Because ultrasound is a pulse system and time-of-flight is used to determine depth, quick recovery from input overloads is essential. Overload can occur in the preamp and the VGA. Immediately following a transmit pulse, the typical VGA gains are low, and the LNA is subject to overload from T/R switch leakage. With increasing gain, the VGA can become overloaded due to strong echoes that occur near field echoes and acoustically dense materials, such as bone.

Figure 39 illustrates an external overload protection scheme. A pair of back-to-back Schottky diodes is installed prior to installing the ac-coupling capacitors. Although the BAS40 diodes are shown, any diode is prone to exhibiting some amount of shot noise. Many types of diodes are available for achieving the desired noise performance. The configuration shown in Figure 39 tends to add 2 nV√Hz of input-referred noise. Decreasing the 5 kΩ resistor and increasing the 2 kΩ resistor may improve noise contribution, depending on the application. With the diodes shown in Figure 39, clamping levels of ±0.5 V or less significantly enhances the system overload performance.

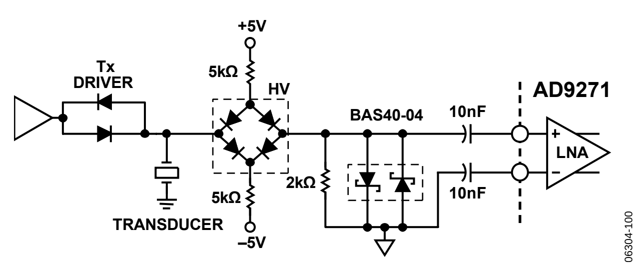

Figure 39. Input Overload Protection

CW DOPPLER OPERATION

Modern ultrasound machines used for medical applications employ a 2^n binary array of receivers for beam forming, with

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typical array sizes of 16 or 32 receiver channels phase-shifted and summed together to extract coherent information. When used in multiples, the desired signals from each of the channels can be summed to yield a larger signal (increased by a factor N, where N is the number of channels), and the noise is increased by the square root of the number of channels. This technique enhances the signal-to-noise performance of the machine. The critical elements in a beam-former design are the means to align the incoming signals in the time domain and the means to sum the individual signals into a composite whole.

Beam forming, as applied to medical ultrasound, is defined as the phase alignment and summation of signals that are generated from a common source but received at different times by a multielement ultrasound transducer. Beam forming has two functions: It imparts directivity to the transducer, enhancing its gain, and it defines a focal point within the body from which the location of the returning echo is derived.

The AD9271 includes the front-end components needed to implement analog beam forming for CW Doppler operation. These components allow CW channels with similar phases to be coherently combined before phase alignment and down mixing, thus reducing the number of delay lines or adjustable phase shifters/down mixers (AD8333 or AD8339) required. Next, if delay lines are used, the phase alignment is performed and then the channels are coherently summed and down converted by a dynamic range I/Q demodulator. Alternatively, if phase shifters/ down mixers, such as the AD8333 and AD8339, are used, phase alignment and down conversion are done before coherently summing all channels into I/Q signals. In either case, the resultant I and Q signals are filtered and sampled by two high resolution ADCs, and the sampled signals are processed to extract the relevant Doppler information.

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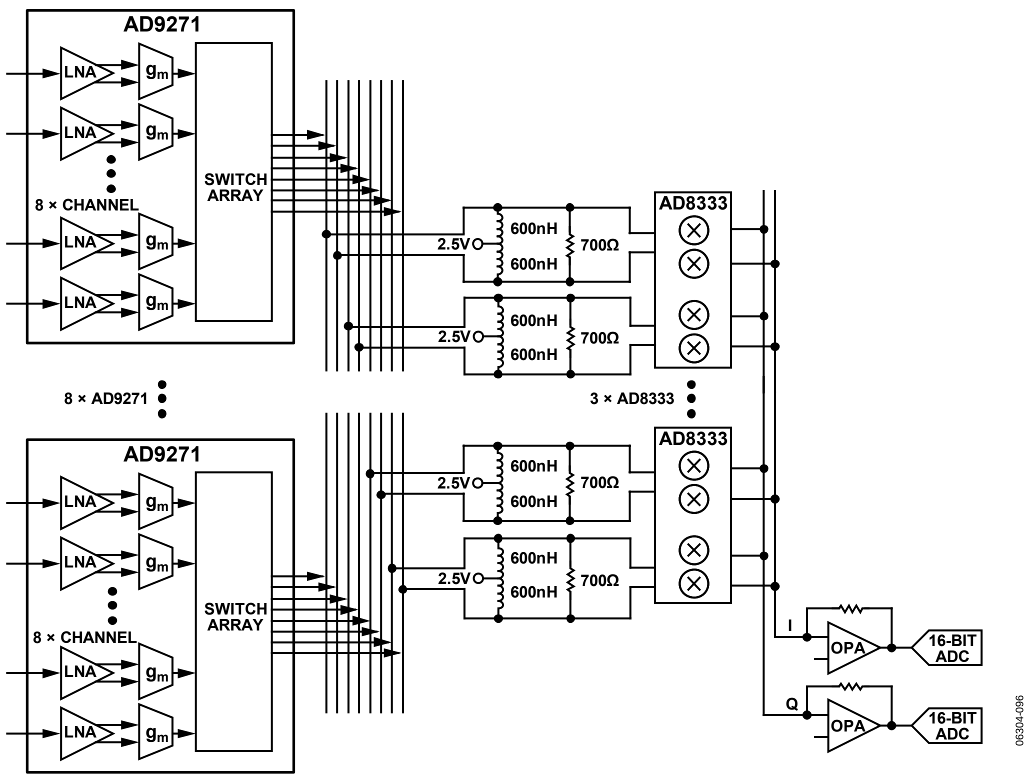

Figure 40. Typical CW Doppler System Using the AD9271 and AD8339

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Crosspoint Switch

Each LNA is followed by a transconductance amp for V/I conversion. Currents can be routed to one of six pairs of differential outputs or to 12 single-ended outputs for summing. Each CWD output pin sinks 2.4 mA dc current, and the signal has a full-scale of ±2 mA for each channel selected by the cross-point switch. For example, if four channels were to be summed on one CWD output, the output would sink 9.6 mA dc and have a full-scale current output of ±8 mA. The maximum number of channels combined must be considered in setting the load impedance for I/V conversion to ensure that the full-scale swing and common-mode voltage are within the operating limits of the AD9271. When interfacing to the AD8339, a common-mode voltage of 2.5 V and a full-scale swing of 2.8 V p-p are desired This can be accomplished by connecting an inductor between each CWD output and a 2.5 V supply, and then connecting either a single-ended or differential load resistance to the CWD outputs. The value of resistance should be calculated based on the maximum number of channels that can be combined.

CWD outputs are required under full-scale swing to be within 1.5 V and CWVDD (3.3 V supply).

TGC OPERATION

The signal path is fully differential throughout to maximize signal swing and reduce even-order distortion; however, the LNAs are designed to be driven from a single-ended signal source. Gain values are referenced from the single-ended LNA input to the differential output of the LNA. A simple exercise in understanding the maximum and minimum gain requirements is shown in Figure 41.

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Table 8. LNA Specifications

LNA Parameters	Specifications
BW (MHz)	15
FS/FSrms (mVpp/mV)	333/118
SNR (dB)	88.1
ENOB (Bits)	14.3
Noise (rms uV/nV/rt(Hz))	4.65/1.2

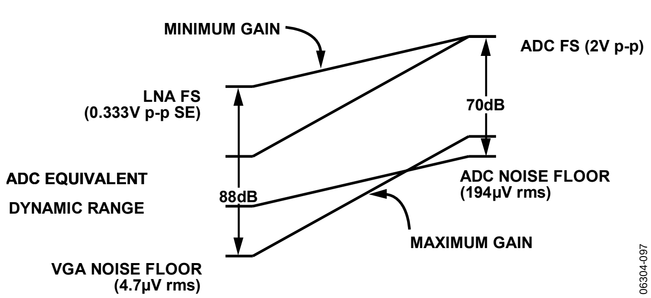

Figure 41. Gain Requirements of TGC for a 12-Bit, 40 MSPS ADC

Table 9. ADC Specifications

ADC Parameters	Specifications
FS/FSrms (Vpp/mV)	2/707
SNR (dB)	70
ENOB (Bits)	11.3
SFDR (dB)	−82
Noise (rms uV/nV/rt(Hz))	194/50

In summary, the maximum gain required is determined by

(*ADC Noise Floor*/*VGA Input Noise Floor*) + *Margin* =
20 log(194/4.7) + 10 dB = 42.3 dB

The minimum gain required is determined by

(*ADC Input FS*/*VGA Input FS*) + *Margin* =
20 log(2/0.333) − 6 dB = 9.6 dB

Therefore, a 12-bit, 40 MSPS ADC with 15 MHz of bandwidth should suffice in achieving the dynamic range required for most ultrasound systems today.

The system gain is distributed as listed in Table 7.

Table 10. Channel Gain Distribution

Section	Nominal Gain (dB)
LNA	14/15.6/18
Attenuator	0 to −30
VGA Amp	25
Filter	0
ADC	0
Total	9 to 39/10.6 to 40.6/13 to 43

The linear-in-dB gain range of the TGC path is 30 dB, extending from 9.6 dB to 39.6 dB. The slope of the gain control interface is 30 dB/V, and the gain control range is 0 V to 1 V. Equation 1 is the expression for gain.

$$Gain\,(dB) = 30\frac{\text{dB}}{\text{V}}V_{GAIN} + ICPT \tag{1}$$

where ICPT is the intercept point of the LNA gain.

In its default condition, the LNA has a gain of 15.6 dB (6×) and the VGA gain is −6 dB if the voltage on the V_{GAIN} pin is 0 V. This gives rise to a total gain (or ICPT) of 9.6 dB through the TGC path if the LNA input is unmatched, or of 3.6 dB if the LNA is matched to 50 Ω (R_{FB} = 200 Ω). If the voltage on the V_{GAIN} pin is 1 V, however, the VGA gain is 24 dB. This gives rise to a total gain of 39.6 dB through the TGC path if the LNA input is unmatched, or of 33.5 dB if the LNA input is matched.

Each of the LNA outputs is dc-coupled to a VGA input. The VGA consists of an attenuator with a range of 30 dB followed by an amplifier with 24 dB of gain for a net gain range of −5 dB to +25 dB. The X-AMP gain-interpolation technique results in low

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gain error and uniform bandwidth, and differential signal paths minimize distortion.

At low gain the VGA should limit the system noise performance (SNR), whereas at high gains the noise is defined by the source and LNA. The maximum voltage swing is bounded by the full-scale peak-to-peak ADC input voltage (2 V p-p).

Variable Gain Amplifier

The differential X-AMP VGA provides precise input attenuation and interpolation. It has a low input-referred noise of 4 nV/√Hz and excellent gain linearity. A simplified block diagram is shown in Figure 42.

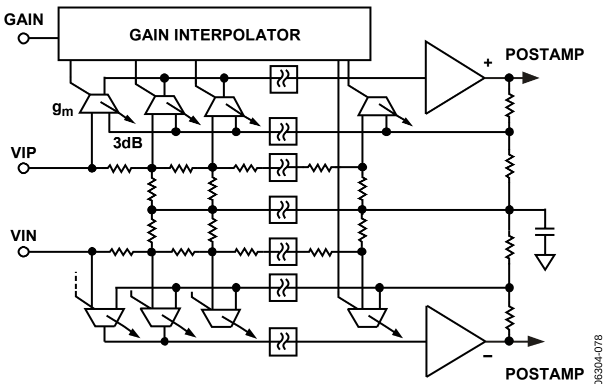

Figure 42. Simplified VGA Schematic

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The input of the VGA is a 12-stage differential resistor ladder with 3.01 dB per tap. The resulting total gain range is 30 dB, which allows for range loss at the endpoints. The effective input resistance per side is 180 Ω nominally for a total differential resistance of 360 Ω. The ladder is driven by a fully differential input signal from the LNA. LNA outputs are dc-coupled to avoid external decoupling capacitors. The common-mode voltage of the attenuator and the VGA is controlled by an amplifier that uses the same midsupply voltage derived in the LNA, permitting dc coupling of the LNA to the VGA without introducing large offsets due to common-mode differences. However, any offset from the LNA will be amplified as the gain is increased, producing an exponentially increasing VGA output offset.

The input stages of the X-AMP are distributed along the ladder, and a biasing interpolator, controlled by the gain interface, determines the input tap point. With overlapping bias currents, signals from successive taps merge to provide a smooth attenuation range from 0 dB to −30 dB. This circuit technique results in linear-in-dB gain law conformance and low distortion levels—only deviating ±0.2 dB or less from the ideal. The gain slope is monotonic with respect to the control voltage and is stable with variations in process, temperature, and supply.

The X-AMP inputs are part of a 25 dB gain feedback amplifier that completes the VGA. Its bandwidth is about 80 MHz. The input stage is designed to reduce feedthrough to the output and to ensure excellent frequency response uniformity across the gain setting.

Gain Control

The gain control interface, GAIN±, is a differential input. V_{GAIN} varies the gain of all VGAs through the interpolator by selecting the appropriate input stages connected to the input attenuator. The nominal V_{GAIN} range for 30 dB/V is 0 V to 1 V, with the best gain-linearity from about 0.1 V to 0.9 V, where the error is typically less than ±0.2 dB. For V_{GAIN} voltages greater than 0.9 V and less than 0.1 V, the error increases. The value of the V_{GAIN} voltage can be increased to that of the supply voltage without gain foldover.

Gain control response time is less than 750 ns to settle within 10% of the final value for a change from minimum to maximum gain.

There are two ways in which the GAIN pins can be interfaced. Using a single-ended method, a Kelvin type of connection to ground should be used as shown in Figure 43. For driving multiple devices, it is preferred to use a differential method as shown in Figure 44. In either method, the GAIN pins should be dc-coupled and driven to accommodate a 1 V full-scale input.

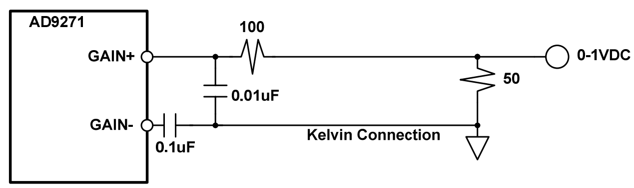

Figure 43. Single-Ended Gain Pin Configuration

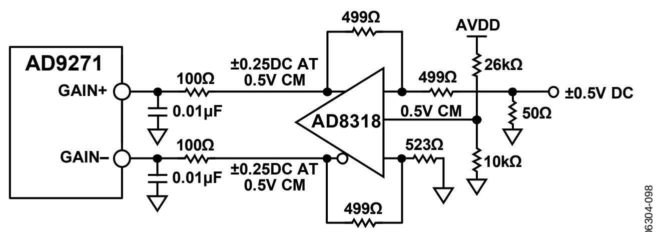

Figure 44. Differential Gain Pin Configuration

VGA Noise

In a typical application, a VGA compresses a wide dynamic range input signal to within the input span of an ADC. The input-referred noise of the LNA limits the minimum resolvable input signal, whereas the output-referred noise, which depends primarily on the VGA, limits the maximum instantaneous dynamic range that can be processed at any one particular gain control voltage. This limit is set in accordance with the quantization noise floor of the ADC.

Output- and input-referred noise as a function of V_{GAIN} are shown in Figure TBD and Figure TBD for the short-circuited input conditions. The input noise voltage is simply equal to the output noise divided by the measured gain at each point in the control range.

The output-referred noise is a flat 65 nV/√Hz over most of the gain range, because it is dominated by the fixed output-referred noise of the VGA. At the high end of the gain control range, the

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noise of the LNA and source prevail. The input-referred noise reaches its minimum value near the maximum gain control voltage, where the input-referred contribution of the VGA is miniscule.

At lower gains, the input-referred noise, and therefore the noise figure, increases as the gain decreases. The instantaneous dynamic range of the system is not lost, however, because the input capacity increases as the input-referred noise increases. The contribution of the ADC noise floor has the same dependence. The important relationship is the magnitude of the VGA output noise floor relative to that of the ADC.

Gain control noise is a concern in very low noise applications. Thermal noise in the gain control interface can modulate the channel gain. The resultant noise is proportional to the output signal level and usually only evident when a large signal is present. The gain interface includes an on-chip noise filter, which reduces this effect significantly at frequencies above 5 MHz. Care should be taken to minimize noise impinging at the GAIN input. An external RC filter can be used to remove V_{GAIN} source noise. The filter bandwidth should be sufficient to accommodate the desired control bandwidth.

Antialiasing Filter

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The filter that the signal reaches prior to the ADC is used to reject dc signals and to bandlimit the signal for antialiasing. Figure 45 shows the architecture of the filter.

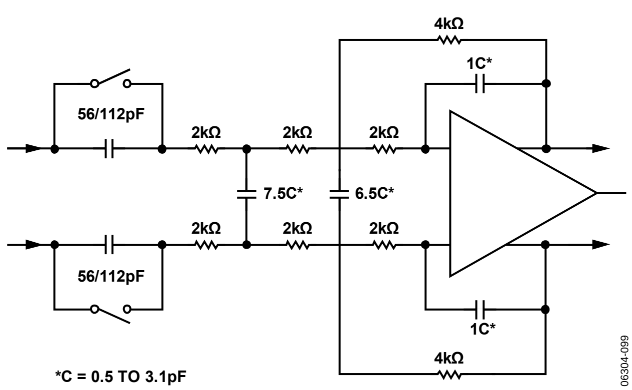

Figure 45. Simplified Filter Schematic

The filter can be configured for dc coupling or to have a single pole for high-pass filtering at either 700 kHz or 350 kHz (programmed through the SPI). The high-pass pole, however, is not tuned and can vary by ±30%.

A third-order Butterworth low-pass filter is used to reduce noise bandwidth and provide antialiasing for the ADC. The filter uses on-chip tuning to trim the capacitors to set the desired cutoff and reduce variation. The default −3dB cutoff is 1/3 the ADC sample clock rate. The cutoff can be scaled to 0.7, 0.8, 0.9, 1, 1.1, 1.2, or 1.3 times this frequency through the SPI. The cutoff can be set from 8 MHz to 18 MHz.

Tuning is normally off to avoid changing the capacitor settings during critical times. The tuning circuit is enabled and disabled through the SPI. Tuning should be done after initial power-up and after reprogramming the filter cutoff scaling or ADC sample rate. Occasional retuning during an idle time is recommended.

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A/D CONVERTER

The AD9271 architecture consists of a pipelined ADC that is divided into three sections: a 4-bit first stage followed by eight 1.5-bit stages and a 3-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stages. The quantized outputs from each stage are combined into a 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample and the remaining stages to operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage except for the last of the pipeline consists of a low resolution flash ADC connected to a switched-capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage consists of a flash ADC.

The output staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The data is then serialized and aligned to the frame and output clock.

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9271 sample clock inputs (CLK+ and CLK−) should be clocked with a differential signal. This signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or capacitors. These pins are biased internally and require no additional bias.

Figure 46 shows the preferred method for clocking the AD9271. The low jitter clock source, such as the Valpey Fisher oscillator VFAC3-BHL-50MHz, is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the secondary transformer limit clock excursions into the AD9271 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9271 and preserves the fast rise and fall times of the signal, which are critical to low jitter performance.

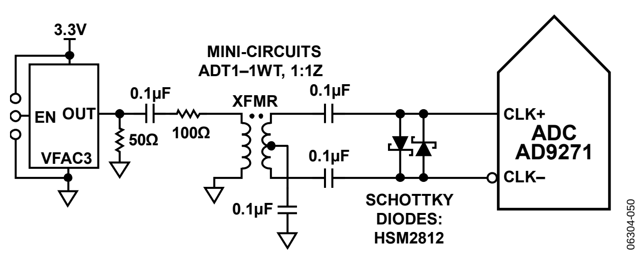

Figure 46. Transformer-Coupled Differential Clock

If a low jitter clock is available, another option is to ac-couple a differential PECL signal to the sample clock input pins as shown in Figure 47. The AD951x family of clock drivers offers excellent jitter performance.

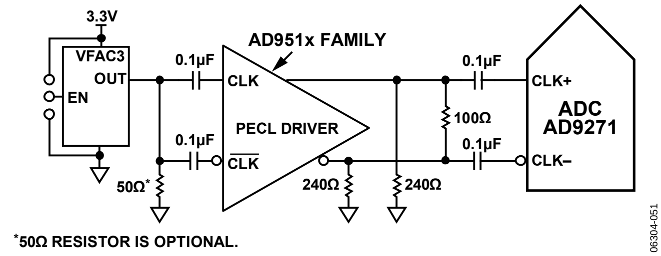

Figure 47. Differential PECL Sample Clock

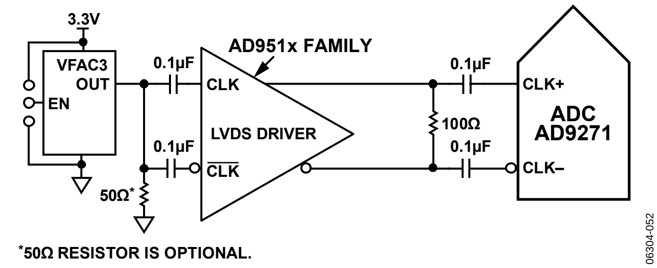

Figure 48. Differential LVDS Sample Clock

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, CLK+ should be driven directly from a CMOS gate, and the CLK− pin should be bypassed to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor (see Figure 48). Although the CLK+ input circuit supply is AVDD (1.8 V), this input is designed to withstand input voltages up to 3.3 V, making the selection of the drive logic voltage very flexible.

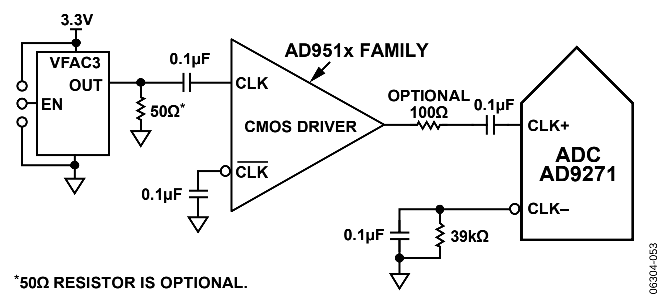

Figure 49. Single-Ended 1.8 V CMOS Sample Clock

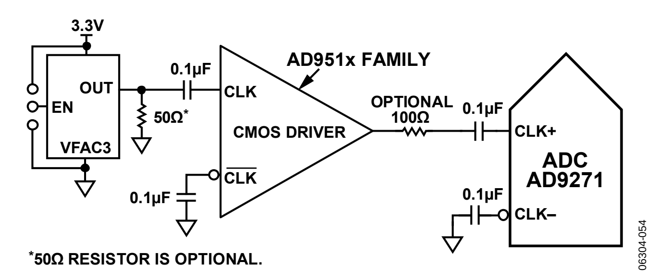

Figure 50. Single-Ended 3.3 V CMOS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to the clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9271 contains a duty cycle

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stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9271. When the DCS is on, noise and distortion performance are nearly flat for a wide range of duty cycles. However, some applications may require the DCS function to be off. If so, keep in mind that the dynamic range performance can be affected when operated in this mode. See the Memory Map section for more details on using this feature.

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately eight clock cycles to allow the DLL to acquire and lock to the new rate.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR\ Degradation = 20 \times \log 10[1/2 \times \pi \times f_A \times t_J]$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter. IF undersampling applications are particularly sensitive to jitter (see Figure 51).

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The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9271. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources, such as the Valpey Fisher VFAC3 series. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs (visit www.analog.com).

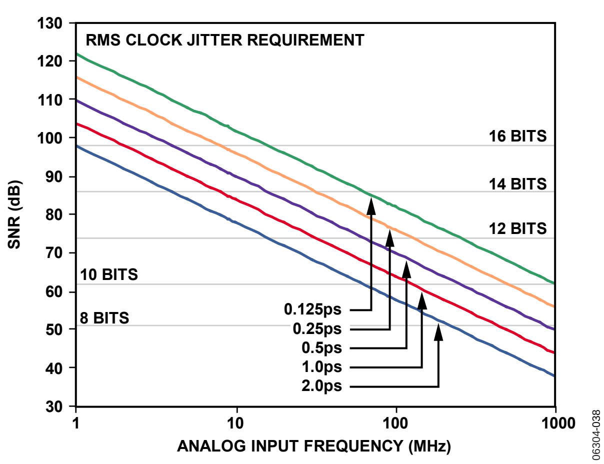

Figure 51. Ideal SNR vs. Input Frequency and Jitter

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Power Dissipation and Power-Down Mode

As shown in Figure 52, the power dissipated by the AD9271 is proportional to its sample rate. The digital power dissipation does not vary much because it is determined primarily by the DRVDD supply and bias current of the LVDS output drivers.

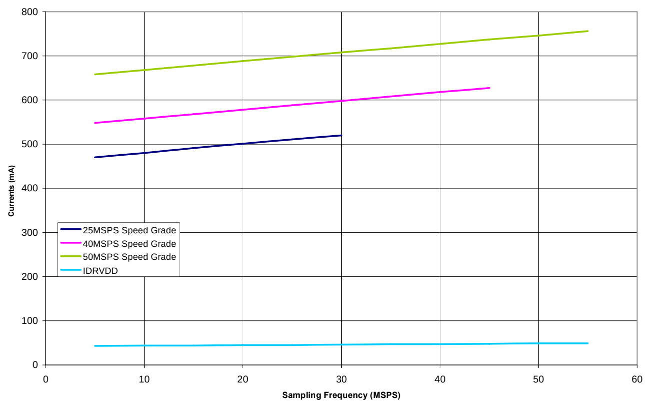

Figure 52. Supply Current vs. f_{SAMPLE} for f_{IN} = 7.5 MHz

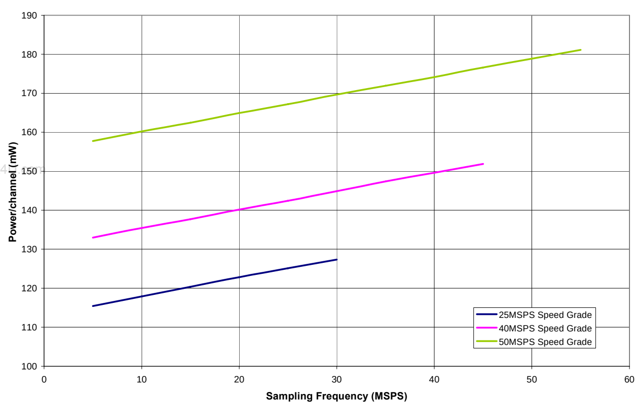

Figure 53. Power per Channel vs. f_{SAMPLE} for f_{IN} = 7.5 MHz

By asserting the PDWN pin high, the AD9271 is placed in power-down mode. In this state, the ADC typically dissipates xx mW. During power-down, the LVDS output drivers are placed in a high impedance state. The AD9271 returns to normal operating mode when the PDWN pin is pulled low. This pin is both 1.8 V and 3.3 V tolerant.

By asserting the STBY pin high, the AD9271 is placed in a standby mode. In this state, the ADC typically dissipates xx mW. During standby, the entire part is powered down except the internal references. The LVDS output drivers are placed in a high impedance state. This mode is well suited for applications that require power savings because it allows the device to be powered down when not in use and then quickly powered up. The time to power this device back up is also greatly reduced. The AD9271 returns to normal operating mode when the STBY pin is pulled low. This pin is both 1.8 V and 3.3 V tolerant.

In power-down mode, low power dissipation is achieved by shutting down the reference, reference buffer, PLL, and biasing networks. The decoupling capacitors on REFT and REFB are discharged when entering power-down mode and must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in the power-down mode; shorter cycles result in proportionally shorter wake-up times. With the recommended 0.1 µF and 4.7 µF decoupling capacitors on REFT and REFB, it takes approximately 1 sec to fully discharge the reference buffer decoupling capacitors and xx µs to restore full operation.

There are a number of other power-down options available when using the SPI port interface. The user can individually power down each channel or put the entire device into standby mode. This allows the user to keep the internal PLL powered up when fast wake-up times (~xxx ns) are required. See the Memory Map section for more details on using these features.

Digital Outputs and Timing

The AD9271 differential outputs conform to the ANSI-644 LVDS standard on default power-up. This can be changed to a low power, reduced signal option similar to the IEEE 1596.3 standard using the SDIO/ODM pin or via the SPI. This LVDS standard can further reduce the overall power dissipation of the device by approximately xx mW. See the SDIO Pin section or Table 16 in the Memory Map section for more information. The LVDS driver current is derived on-chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing at the receiver.

The AD9271 LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs that have LVDS capability for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor placed as close to the receiver as possible. No far-end receiver termination and poor differential trace routing may result in timing errors. It is recommended that the trace length is no longer than 24 inches and that the differential output traces are kept close together and at equal lengths. An example of the FCO and data stream with proper trace length and position can be found in Figure 54.

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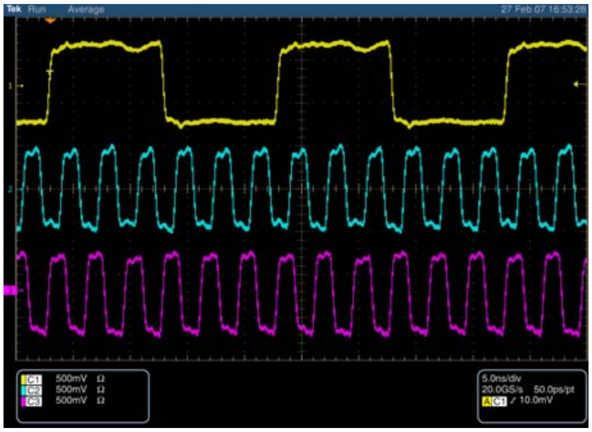

Figure 54. LVDS Output Timing Example in ANSI Mode (Default)

An example of the LVDS output using the ANSI standard (default) data eye and a time interval error (TIE) jitter histogram with trace lengths of less than 24 inches on regular FR-4 material is shown in Figure 55. Figure 56 shows an example of when the trace lengths exceed 24 inches on regular FR-4 material. Notice that the TIE jitter histogram reflects the decrease of the data eye opening as the edge deviates from the ideal position; therefore, the user must determine if the waveforms meet the timing budget of the design when the trace lengths exceed 24 inches. Additional SPI options allow the user to further increase the internal termination (and therefore increase the current) of all eight outputs in order to drive longer trace lengths (see Figure 57). Even though this produces sharper rise and fall times on the data edges, is less prone to bit errors, and improves frequency distribution (see Figure 57), the power dissipation of the DRVDD supply increases when this option is used.

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In cases that require increased driver strength to the DCO and FCO outputs because of load mismatch Register 15 allows the user to double the drive strength. To do this, set the appropriate bit in Register 5. Note that this feature cannot be used with Bit 4 and Bit 5 in Register 15 because these bits take precedence over this feature. See the Memory Map section for more details.

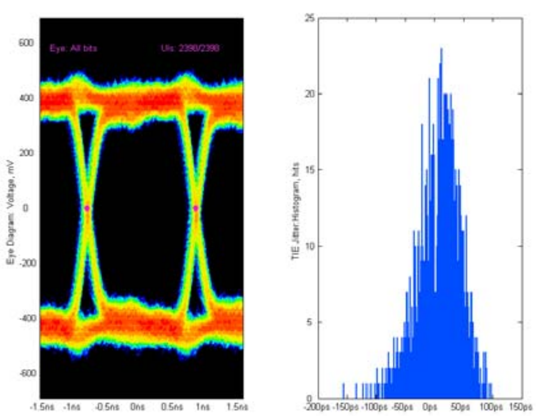

Figure 55. Data Eye for LVDS Outputs in ANSI Mode with Trace Lengths of Less than 24 Inches on Standard FR-4

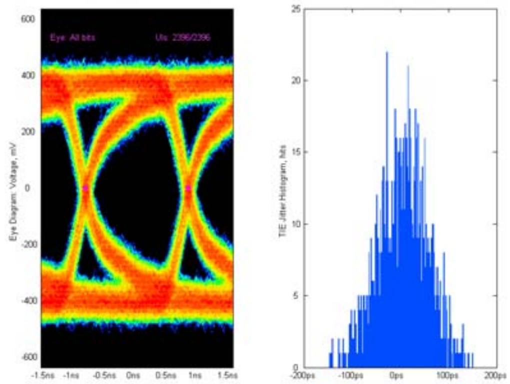

Figure 56. Data Eye for LVDS Outputs in ANSI Mode with Trace Lengths of Greater than 24 Inches on Standard FR-4

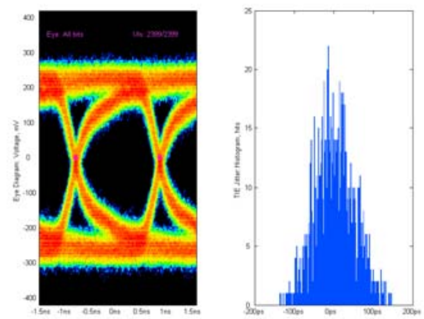

Figure 57. Data Eye for LVDS Outputs in ANSI Mode with 100 Ω Termination on and Trace Lengths of Greater than 24 Inches on Standard FR-4

The format of the output data is offset binary by default. An example of the output coding format can be found in Table 11. If it is desired to change the output data format to twos complement, see the Memory Map section.

Table 11. Digital Output Coding

Code	(VIN+) − (VIN−), Input Span = 2 V p-p (V)	Digital Output Offset Binary (D11 ... D0)
4095	+1.00	1111 1111 1111
2048	0.00	1000 0000 0000
2047	−0.000488	0111 1111 1111
0	−1.00	0000 0000 0000

Data from each ADC is serialized and provided on a separate channel. The data rate for each serial stream is equal to 12 bits times the sample clock rate, with a maximum of 600 Mbps (12 bits × 50 MSPS = 600 Mbps). The lowest typical conversion rate is 10 MSPS. However, if lower sample rates are required for a specific application, the PLL can be set up for encode rates lower than 10 MSPS via the SPI. This allows encode rates as low as 5 MSPS. See the Memory Map section for details on enabling this feature.

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Two output clocks are provided to assist in capturing data from the AD9271. The DCO is used to clock the output data and is equal to six times the sampling clock (CLK) rate. Data is clocked out of the AD9271 and must be captured on the rising and falling edges of the DCO that supports double data rate (DDR) capturing. The frame clock out (FCO) is used to signal the start of a new output byte and is equal to the sampling clock rate. See the timing diagram shown in Figure 2 for more information.

Table 12. Flex Output Test Modes

Output Test Mode Bit Sequence	Pattern Name	Digital Output Word 1	Digital Output Word 2	Subject to Data Format Select
0000	Off (default)	N/A	N/A	N/A
0001	Midscale short	1000 0000 (8 bits) 10 0000 0000 (10 bits) 1000 0000 0000 (12 bits) 10 0000 0000 0000 (14 bits)	Same	Yes
0010	+Full-scale short	1111 1111 (8 bits) 11 1111 1111 (10 bits) 1111 1111 1111 (12 bits) 11 1111 1111 1111 (14 bits)	Same	Yes
0011	−Full-scale short	0000 0000 (8 bits) 00 0000 0000 (10 bits) 0000 0000 0000 (12 bits) 00 0000 0000 0000 (14 bits)	Same	Yes
0100	Checkerboard	1010 1010 (8 bits) 10 1010 1010 (10 bits) 1010 1010 1010 (12 bits) 10 1010 1010 1010 (14 bits)	0101 0101 (8 bits) 01 0101 0101 (10 bits) 0101 0101 0101 (12 bits) 01 0101 0101 0101 (14 bits)	No
0101	PN sequence long[1]	N/A	N/A	Yes
0110	PN sequence short[1]	N/A	N/A	Yes
0111	One/zero word toggle	1111 1111 (8 bits) 11 1111 1111 (10 bits) 1111 1111 1111 (12 bits) 11 1111 1111 1111 (14 bits)	0000 0000 (8 bits) 00 0000 0000 (10 bits) 0000 0000 0000 (12 bits) 00 0000 0000 0000 (14 bits)	No
1000	User input	Register 0x19 to Register 0x1A	Register 0x1B to Register 0x1C	No
1001	One/zero bit toggle	1010 1010 (8 bits) 10 1010 1010 (10 bits) 1010 1010 1010 (12 bits) 10 1010 1010 1010 (14 bits)	N/A	No
1010	1× sync	0000 1111 (8 bits) 00 0001 1111 (10 bits) 0000 0011 1111 (12 bits) 00 0000 0111 1111 (14 bits)	N/A	No
1011	One bit high	1000 0000 (8 bits) 10 0000 0000 (10 bits) 1000 0000 0000 (12 bits) 10 0000 0000 0000 (14 bits)	N/A	No
1100	Mixed frequency	1010 0011 (8 bits) 10 0110 0011 (10 bits) 1010 0011 0011 (12 bits) 10 1000 0110 0111 (14 bits)	N/A	No

[1] All test mode options, except PN Sequence Short and PN Sequence Long, can support 8- to 14-bit word lengths in order to verify data capture to the receiver.

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When using the serial port interface (SPI), the DCO phase can be adjusted in 60° increments relative to the data edge. This enables the user to refine system timing margins if required. The default DCO timing, as shown in Figure 2, is 90° relative to the output data edge.

An 8-, 10-, and 14-bit serial stream can also be initiated from the SPI. This allows the user to implement different serial streams and test the device's compatibility with lower and higher resolution systems. When changing the resolution to an 8- or 10-bit serial stream, the data stream is shortened. When using the 14-bit option, the data stream stuffs two 0s at the end of the normal 14-bit serial data.

When using the SPI, all of the data outputs can also be inverted from their nominal state. This is not to be confused with inverting the serial stream to an LSB-first mode. In default mode, as shown in Figure 2, the MSB is represented first in the data output serial stream. However, this can be inverted so that the LSB is represented first in the data output serial stream (see Figure 3).

There are 12 digital output test pattern options available that can be initiated through the SPI. This is a useful feature when validating receiver capture and timing. Refer to Table 12 for the output bit sequencing options available. Some test patterns have two serial sequential words and can be alternated in various ways, depending on the test pattern chosen. It should be noted that some patterns may not adhere to the data format select option. In addition, customer user patterns can be assigned in the 0x19, 0x1A, 0x1B, and 0x1C register addresses. All test mode options, except PN Sequence Short and PN Sequence Long can support 8- to 14-bit word lengths in order to verify data capture to the receiver.

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The PN Sequence Short pattern produces a pseudorandom bit sequence that repeats itself every $2^9 - 1$ or 511 bits. A description of the PN sequence and how it is generated can be found in section 5.1 of the ITU-T 0.150 (05/96) standard. For the AD9271, the only discrepancy from the ITU standard is that the starting value is a specific value instead of all ones. See Table 10 for initial values.

The PN Sequence Long pattern produces a pseudorandom bit sequence that repeats itself every $2^{23} - 1$ or 8,388,607 bits. A description of the PN sequence and how it is generated can be found in section 5.6 of the ITU-T 0.150 (05/96) standard. The only two discrepancies between the ITU standard and the AD9271 PN Sequence Long implementation are as follows. First, the starting value is a specific value instead of all ones. Second, the AD9271 inverts the bit stream with relation to the ITU standard. See Table 10 for initial values.

Table 10. PN Sequence

	Initial Value	First 3 output samples (MSB 1st)
PN Sequence Short	0x0df	0xdf9, 0x353, 0x301
PN Sequence Long	0x29b80a	0x591, 0xfd7, 0a3

Consult the Memory Map section for information on how to change these additional digital output timing features through the serial port interface or SPI.

SDIO Pin

This pin is required to operate the SPI port interface. It has an internal 30 kΩ pull-down resistor that pulls this pin low and is only 1.8 V tolerant. If applications require that this pin be driven from a 3.3 V logic level, insert a 1 kΩ resistor in series with this pin to limit the current.

SCLK Pin

This pin is required to operate the SPI port interface. It has an internal 30 kΩ pull-down resistor that pulls this pin low and is both 1.8 V and 3.3 V tolerant.

CSB Pin

This pin is required to operate the SPI port interface. It has an internal 70 kΩ pull-down resistor that pulls this pin low and is both 1.8 V and 3.3 V tolerant.

RBIAS Pin

To set the internal core bias current of the ADC, place a resistor (nominally equal to 10.0 kΩ) to ground at the RBIAS pin. The resistor current is derived on-chip and sets the ADC's AVDD current to a nominal xxx mA at 50 MSPS. Therefore, it is imperative that at least a 1% tolerance on this resistor be used to achieve consistent performance.

Voltage Reference

A stable and accurate 0.5 V voltage reference is built into the AD9271. This is gained up internally by a factor of 2, setting V_{REF} to 1.0 V, which results in a full-scale differential input span of 2 V p-p for the ADC. The V_{REF} is set internally by default; however, the VREF pin can be driven externally with a 1.0 V reference to achieve more accuracy.

When applying the decoupling capacitors to the VREF, REFT, and REFB pins, use ceramic low ESR capacitors. These capacitors should be close to reference pins and on the same layer of the PCB as the AD9271. The recommended capacitor values and configurations for the AD9271 reference pin can be found in Figure 58.

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Table 13. Reference Settings

Selected Mode	SENSE Voltage	Resulting VREF (V)	Resulting Differential Span (V p-p)
External Reference	AVDD	N/A	2 × external reference
Internal, 2 V p-p FSR	AGND to 0.2 V	1.0	2.0

Internal Reference Operation

A comparator within the AD9271 detects the potential at the SENSE pin and configures the reference. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 58), setting VREF to 1 V.

The REFT and REFB pins establish their input span of the ADC core from the reference configuration. The analog input full-scale range of the ADC equals twice the voltage at the reference pin for either an internal or an external reference configuration.

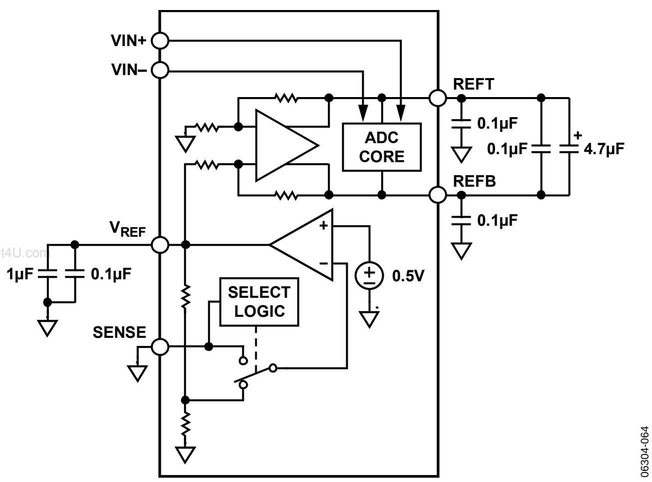
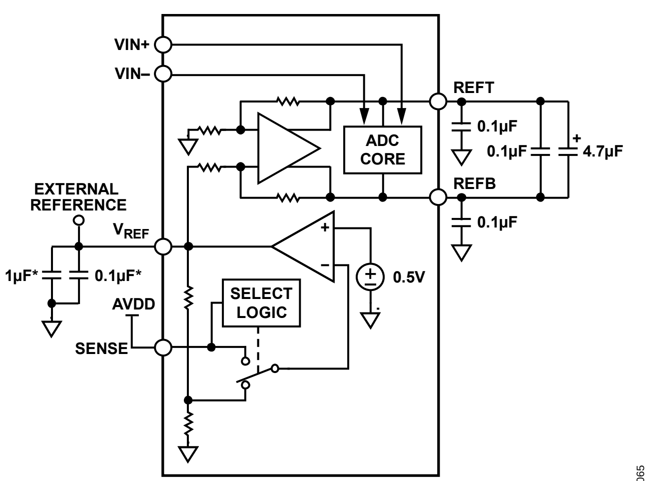


Figure 58. Internal Reference Configuration



*OPTIONAL.

Figure 59. External Reference Operation

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 61 shows the typical drift characteristics of the internal reference in 1 V mode.

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. The external reference is loaded with an equivalent 6 kΩ load. An internal reference buffer generates the positive and negative full-scale references, REFT and REFB, for the ADC core. Therefore, the external reference must be limited to a nominal of 1.0 V.

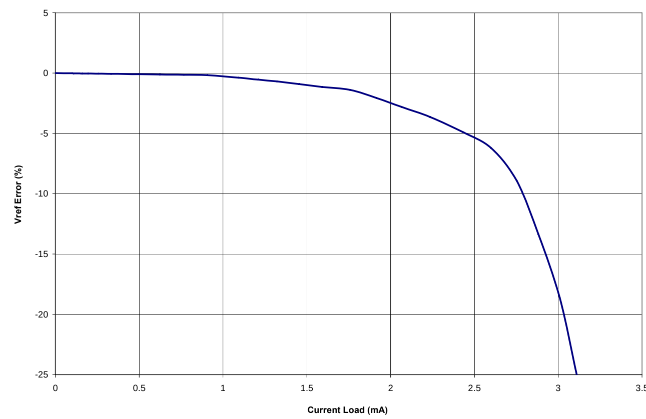


Figure 60. V_{REF} Accuracy vs. Load, AD9271-50

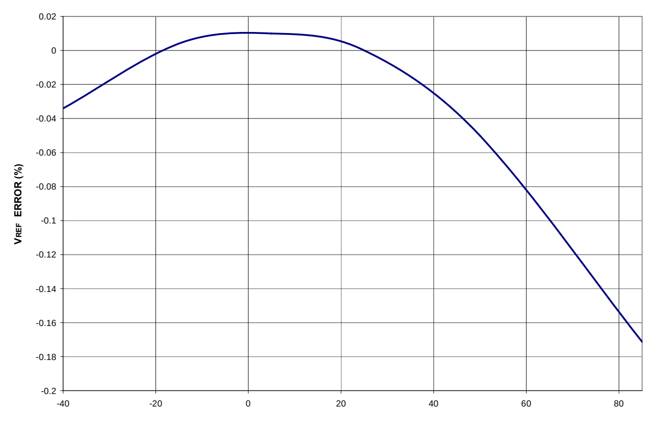


Figure 61. Typical V_{REF} Drift, AD9271-50

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SERIAL PORT INTERFACE (SPI)

The AD9271 serial port interface allows the user to configure the signal chain for specific functions or operations through a structured register space provided inside the chip. This offers the user added flexibility and customization depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided down into fields, as documented in the Memory Map section. Detailed operational information can be found in the Analog Devices, Inc., user manual *Interfacing to High Speed ADCs via SPI*.

There are three pins that define the serial port interface, or SPI, to this particular ADC. They are the SCLK, SDIO, and CSB pins. The SCLK (serial clock) is used to synchronize the read and write data presented to the ADC. The SDIO (serial data input/output) is a dual-purpose pin that allows data to be sent to and read from the internal ADC memory map registers. The CSB (chip select bar) is an active low control that enables or disables the read and write cycles (see Table 14).

Table 14. Serial Port Pins

Pin	Function
SCLK	Serial Clock. The serial shift clock input. SCLK is used to synchronize serial interface reads and writes.
SDIO	Serial Data Input/Output. A dual-purpose pin. The typical role for this pin is as an input or output, depending on the instruction sent and the relative position in the timing frame.
CSB	Chip Select Bar (Active Low). This control gates the read and write cycles.

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The falling edge of the CSB in conjunction with the rising edge of the SCLK determines the start of the framing sequence. During an instruction phase, a 16-bit instruction is transmitted, followed by one or more data bytes, which is determined by Bit Fields W0 and W1. An example of the serial timing and its definitions can be found in Figure 63 and Table 15. In normal operation, CSB is used to signal to the device that SPI commands are to be received and processed. When CSB is brought low, the device processes SCLK and SDIO to process instructions. Normally, CSB remains low until the communication cycle is complete. However, if connected to a slow device, CSB can be brought high between bytes, allowing older microcontrollers enough time to transfer data into shift registers. CSB can be stalled when transferring one, two, or three bytes of data. When W0 and W1 are set to 11, the device enters streaming mode and continues to process data, either reading or writing, until the CSB is taken high to end the communication cycle. This allows complete memory transfers without having to provide additional instructions. Regardless of the mode, if CSB is taken high in the middle of any byte transfer, the SPI state machine is reset and the device waits for a new instruction.

In addition to the operation modes, the SPI port can be configured to operate in different manners. For applications that do not require a control port, the CSB line can be tied and held high. This places the remainder of the SPI pins in their secondary mode as defined in the Serial Port Interface (SPI) section. CSB can also be tied low to enable 2-wire mode. When CSB is tied low, SCLK and SDIO are the only pins required for communication. Although the device is synchronized during power-up, caution must be exercised when using this mode to ensure that the serial port remains synchronized with the CSB line. When operating in 2-wire mode, it is recommended to use a 1-, 2-, or 3-byte transfer exclusively. Without an active CSB line, streaming mode can be entered but not exited.

In addition to word length, the instruction phase determines if the serial frame is a read or write operation, allowing the serial port to be used to both program the chip and read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB- or LSB-first mode. MSB-first mode is the default at power-up and can be changed by adjusting the configuration register. For more information about this and other features, see the user manual *Interfacing to High Speed ADCs via SPI*.

HARDWARE INTERFACE

The pins described in Table 14 compose the physical interface between the user's programming device and the serial port of the AD9271. The SCLK and CSB pins function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

In cases where multiple SDIO pins share a common connection, care should be taken to ensure that proper V_{OH} levels are met. Figure 62 shows the number of SDIO pins that can be connected together, assuming the same load as the AD9271 and the resulting V_{OH} level.

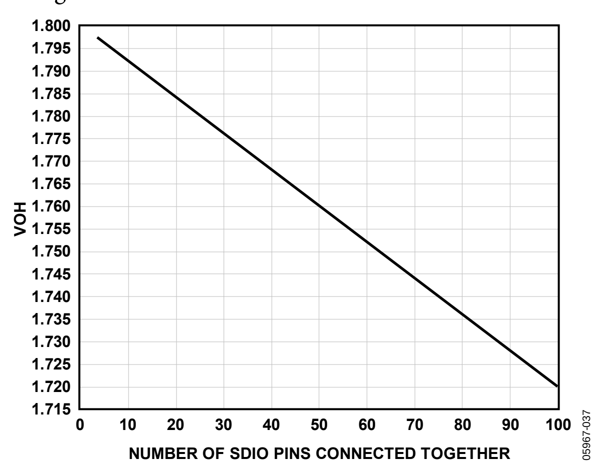

Figure 62. SDIO Pin Loading

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This interface is flexible enough to be controlled by either serial PROMS or PIC mirocontrollers. This provides the user an alternative method, other than a full SPI controller, to program the ADC (see the AN-812 Application Note).

If the user chooses not to use the SPI interface, these pins serve a dual function and are associated with secondary functions when the CSB is strapped to AVDD during device power-up. See the section for details on which pin-strappable functions are supported on the SPI pins.

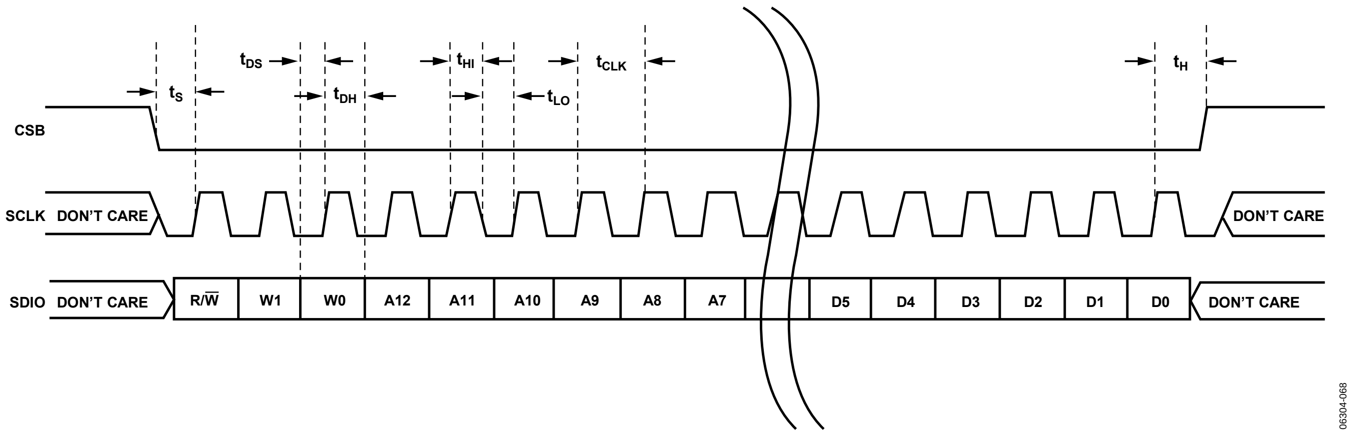

Figure 63. Serial Timing Details

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Table 15. Serial Timing Definitions

Parameter	Minimum Timing (ns)	Description
t_{DS}	5	Setup time between the data and the rising edge of SCLK
t_{DH}	2	Hold time between the data and the rising edge of SCLK
t_{CLK}	40	Period of the clock
t_S	5	Setup time between CSB and SCLK
t_H	2	Hold time between CSB and SCLK
t_{HI}	16	Minimum period that SCLK should be in a logic high state
t_{LO}	16	Minimum period that SCLK should be in a logic low state
t_{EN_SDIO}	1	Minimum time for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 63).
t_{DIS_SDIO}	5	Minimum time for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 63).

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MEMORY MAP

READING THE MEMORY MAP TABLE

Each row in the memory map table has eight address locations. The memory map is roughly divided into three sections: chip configuration register map (Address 0x00 to Address 0x02), device index and transfer register map (Address 0x05 and Address 0xFF), and program register map (Address 0x08 to Address 0x25).

The left most column of the memory map indicates the register address number, and the default value is shown in the right most column. The (MSB) Bit 7 column is the start of the default hexadecimal value given. For example, Address 0x09, clock, has a default value of 0x01, meaning that Bit 7 = 0, Bit 6 = 0, Bit 5 = 0, Bit 4 = 0, Bit 3 = 0, Bit 2 = 0, Bit 1 = 0, and Bit 0 = 1, or 0000 0001 in binary. This setting is the default for the duty cycle stabilizer in the on condition. By writing a 0 to Bit 6 of this address followed by an 0x01 in Register 0xFF (transfer bit), the duty cycle stabilizer turns off. It is important to follow each writing sequence with a transfer bit to update the SPI registers. For more information on this and other functions, consult the user manual *Interfacing to High Speed ADCs via SPI*.

RESERVED LOCATIONS

Undefined memory locations should not be written to except when writing the default values suggested in this data sheet. Addresses that have values marked as 0 should be considered reserved and have a 0 written into their registers during power-up.

DEFAULT VALUES

After a reset, critical registers are automatically loaded with default values. These values are indicated in Table 16, where an X refers to an undefined feature.

LOGIC LEVELS

An explanation of various registers follows: “Bit is set” is synonymous with “bit is set to Logic 1” or “writing Logic 1 for the bit.” Similarly, “clear a bit” is synonymous with “bit is set to Logic 0” or “writing Logic 0 for the bit.”

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Table 16. Memory Map Register

Addr. (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
Chip Configuration Registers											
00	chip_port_config	0	LSB first 1 = on 0 = off (default)	Soft reset 1 = on 0 = off (default)	1	1	Soft reset 1 = on 0 = off (default)	LSB first 1 = on 0 = off (default)	0	0x18	The nibbles should be mirrored so that LSB- or MSB-first mode registers correctly regardless of shift mode.
01	chip_id	Chip ID Bits 7:0 (AD9271 = 0x13), (default)								Read only	Default is unique chip ID, different for each device. This is a read-only register.
02	chip_grade	X	X	Child ID 6:4 (identify device variants of Chip ID) 00 = 50 MSPS (default) 01 = 40 MSPS 11 = 25 MSPS		X	X	X	X	0x00	Child ID used to differentiate graded devices.
Device Index and Transfer Registers											
04	device_index_2	X	X	X	X	Data Channel H 1 = on (default) 0 = off	Data Channel G 1 = on (default) 0 = off	Data Channel F 1 = on (default) 0 = off	Data Channel E 1 = on (default) 0 = off	0x0F	Bits are set to determine which on-chip device receives the next write command.
05	device_index_1	X	X	Clock Channel DCO 1 = on 0 = off (default)	Clock Channel FCO 1 = on 0 = off (default)	Data Channel D 1 = on (default) 0 = off	Data Channel C 1 = on (default) 0 = off	Data Channel B 1 = on (default) 0 = off	Data Channel A 1 = on (default) 0 = off	0x0F	Bits are set to determine which on-chip device receives the next write command.
FF	device_update	X	X	X	X	X	X	X	SW transfer 1 = on 0 = off (default)	0x00	Synchronously transfers data from the master shift register to the slave.
ADC Functions											
08	modes	X	X	X	X	LNA bypass 1 = on 0 = off (default)	Internal power-down mode 000 = chip run (default) 001 = full power-down 010 = standby 011 = reset 100 = CW mode (TGC PWDN)			0x00	Determines various generic modes of chip operation.
09	clock	X	X	X	X	X	X	X	Duty cycle stabilizer 1 = on (default) 0 = off	0x01	Turns the internal duty cycle stabilizer on and off.
0D	test_io	User test mode 00 = off (default) 01 = on, single alternate 10 = on, single once 11 = on, alternate once		Reset PN long gen 1 = on 0 = off (default)	Reset PN short gen 1 = on 0 = off (default)	Output test mode—see Table 12 in the Digital Outputs and Timing section 0000 = off (default) 0001 = midscale short 0010 = +FS short 0011 = −FS short 0100 = checkerboard output 0101 = PN 23 sequence 0110 = PN 9 0111 = one/zero word toggle 1000 = user input 1001 = one/zero bit toggle				0x00	When set, the test data is placed on the output pins in place of normal data. (Local, expect for PN sequence)

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Addr. (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
						1010 = 1× sync 1011 = one bit high 1100 = mixed bit frequency (format determined by output_mode)					
0F	Flex_channel_input	Filter cutoff frequency control 0000 = 0.7 × 1/3 × f_{SAMPLE} 0001 = 0.8 × 1/3 × f_{SAMPLE} 0010 = 0.9 × 1/3 × f_{SAMPLE} 0011 = 1.0 × 1/3 × f_{SAMPLE} 0100 = 1.1 × 1/3 × f_{SAMPLE} 0101 = 1.2 × 1/3 × f_{SAMPLE} 0110 = 1.3 × 1/3 × f_{SAMPLE}				X	X	X	X	0x30	Antialiasing filter cutoff (global)
10	Flex_offset	X	X	6-bit LNA offset adjustment Table = TBD						0x20	LNA force offset correction (local)
11	Flex_gain	X	X	X	X	X	X	LNA gain 00 = 5× 01 = 6× 10 = 8×		0x01	LNA gain adjustment (global)
14	output_mode	X	0 = LVDS ANSI (default) 1 = LVDS low power, (IEEE 1596.3 similar)	X	X	X	Output invert 1 = on 0 = off (default)	00 = offset binary (default) 01 = twos complement		0x00	Configures the outputs and the format of the data.
15	output_adjust	X	X	Output driver termination 00 = none (default) 01 = 200 Ω 10 = 100 Ω 11 = 100 Ω		X	X	X	DCO and FCO 2× drive strength 1 = on 0 = off (default)	0x00	Determines LVDS or other output properties. Primarily functions to set the LVDS span and common-mode levels in place of an external resistor.
16	output_phase	X	X	X	X	0011 = output clock phase adjust (0000 through 1010) (Default: 180° relative to DATA edge) 0000 = 0° relative to DATA edge 0001 = 60° relative to DATA edge 0010 = 120° relative to DATA edge 0011 = 180° relative to DATA edge 0100 = 240° relative to DATA edge 0101 = 300° relative to DATA edge 0110 = 360° relative to DATA edge 0111 = 420° relative to DATA edge 1000 = 480° relative to DATA edge 1001 = 540° relative to DATA edge 1010 = 600° relative to DATA edge 1011 to 1111 = 660° relative to DATA edge				0x03	On devices that utilize global clock divide, determines which phase of the divider output is used to supply the output clock. Internal latching is unaffected.
19	user_patt1_lsb	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-defined pattern, 1 LSB (global).
1A	user_patt1_msb	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-defined pattern, 1 MSB (global).
1B	user_patt2_lsb	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-defined pattern, 2 LSB. (global)
1C	user_patt2_msb	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-defined pattern, 2 MSB (global).

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Addr. (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
21	serial_control	LSB first 1 = on 0 = off (default)	X	X	X	<10 MSPS, low encode rate mode 1 = on 0 = off (default)	000 = 12 bits (default, normal bit stream) 001 = 8 bits 010 = 10 bits 011 = 12 bits 100 = 14 bits			0x00	Serial stream control. Default causes MSB first and the native bit stream (global).
22	serial_ch_stat	X	X	X	X	X	X	Channel output reset 1 = on 0 = off (default)	Channel power-down 1 = on 0 = off (default)	0x00	Used to power down individual sections of a converter (local).
2B	Flex_filter	X	Enable automatic low-pass tuning 1 = on 0 = off (default)	X	X	X	X	High-pass filter cutoff 00 = dc (default) 01 = 700 kHz 10 = 350 kHz		0x00	Filter cutoff (global)
2C	Analog_Input	X	X	X	X	X	X	X	LOSW 1 = on 0 = off (default)	0x00	LNA active termination/input impedance (global)
2D	Cross_point_Switch	X	X	X	Crosspoint switch enable 0 0000 = CDW0p/n 0 0001 = CDW1p/n 0 0010 = CDW2p/n 0 0011 = CDW3p/n 0 0100 = CDW4p/n 0 0101 = CDW5p/n 0 0111 = power down CW channel 1 0000 = CDW0p SE 1 0001 = CDW1p SE 1 0010 = CDW2p SE 1 0011 = CDW3p SE 1 0100 = CDW4p SE 1 0101 = CDW5p SE 1 0111 = power down CW channel 1 1000 = CDW0n SE 1 1001 = CDW1n SE 1 1010 = CDW2n SE 1 1011 = CDW3n SE 1 1100 = CDW4n SE 1 1101 = CDW5n SE 1 1111 = power down CW channel					0x07	Crosspoint switch enable (local)

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Power and Ground Recommendations

When connecting power to the AD9271, it is recommended that two separate 1.8 V supplies be used: one for analog (AVDD) and one for digital (DRVDD). The AD9271 also requires a 3.3 V supply (CWVDD) as well for the crosspoint section. If only one 1.8 V supply is available, it should be routed to the AVDD first and then tapped off and isolated with a ferrite bead or a filter choke preceded by decoupling capacitors for the DRVDD. The user should employ several decoupling capacitors on all supplies to cover both high and low frequencies. These should be located close to the point of entry at the PC board level and close to the parts with minimal trace lengths.

A single PC board ground plane should be sufficient when using the AD9271. With proper decoupling and smart partitioning of the PC board's analog, digital, and clock sections, optimum performance is easily achieved.

Exposed Paddle Thermal Heat Slug Recommendations

It is required that the exposed paddle on the underside of the ADC is connected to analog ground (AGND) to achieve the best electrical and thermal performance of the AD9271. An exposed continuous copper plane on the PCB should mate to the AD9271 exposed paddle, Pin 0. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be solder filled or plugged.

To maximize the coverage and adhesion between the ADC and PCB, partition the continuous copper plane by overlaying a silkscreen on the PCB into several uniform sections. This provides several tie points between the two during the reflow process. Using one continuous plane with no partitions only guarantees one tie point between the AD9271 and PCB. See Figure 64 for a PCB layout example. For more detailed information on packaging and the PCB layout, see the AN-772 Application Note.

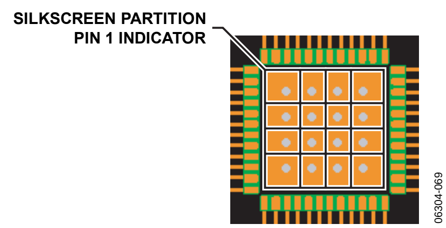

Figure 64. Typical PCB Layout

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EVALUATION BOARD

The AD9271 evaluation board provides all of the support circuitry required to operate the ADC in its various modes and configurations. The LNA is driven differentially through a transformer. Figure 65 shows the typical bench characterization setup used to evaluate the ac performance of the AD9271. It is critical that the signal sources used for the analog input and clock have very low phase noise (<1 ps rms jitter) to realize the optimum performance of the signal chain. Proper filtering of the analog input signal
to remove harmonics and lower the integrated or broadband noise at the input is also necessary to achieve the specified noise performance.

See Figure x to Figure x for the complete schematics and layout diagrams that demonstrate the routing and grounding techniques that should be applied at the system level.

POWER SUPPLIES

This evaluation board comes with a wall-mountable switching power supply that provides a 6 V, 2 A maximum output. Simply connect the supply to the rated 100 V ac to 240 V ac wall outlet at 47 Hz to 63 Hz. The other end is a 2.1 mm inner diameter jack that connects to the PCB at P701. Once on the PC board, the 6 V supply is fused and conditioned before connecting to www.DataSheet three low dropout linear regulators that supply the proper bias to each of the various sections on the board.

When operating the evaluation board in a nondefault condition, L702 to L704 can be removed to disconnect the switching power supply. This enables the user to bias each section of the board individually. Use P501 to connect a different supply for each section. At least one 1.8 V supply is needed with a 1 A current capability for AVDD_DUT and DRVDD_DUT; however, it is recommended that separate supplies be used for both analog and digital domains. To operate the evaluation board using the SPI and alternate clock options, a separate 3.3 V analog supply is needed in addition to the other supplies. The 3.3 V supply, or AVDD_3.3 V, should have a 1 A current capability.

To bias the crosspoint switch circuitry or CW section, separate +5 V and −5 V supplies are required. These should have 1 A current capability each. This section cannot be biased from a 6 V, 2 A wall supply. Separate supplies are required.

INPUT SIGNALS

When connecting the clock and analog source, use clean signal generators with low phase noise, such as Rohde & Schwarz SMHU or HP8644 signal generators or the equivalent. Use a 1 m, shielded, RG-58, 50 Ω coaxial cable for making connections to the evaluation board. Enter the desired frequency and amplitude from the specifications tables. The evaluation board is set up to be clocked from the crystal oscillator, OSC401. If a different or external clock source is desired, follow the instructions for CLOCK outlined in the Default Operation and Jumper Selection Settings section. Typically, most Analog Devices evaluation boards can accept ~2.8 V p-p or 13 dBm sine wave input for the clock. When connecting the analog input source, it is recommended to use a multipole, narrow-band, band-pass filter with 50 Ω terminations. Analog Devices uses TTE and K&L Microwave, Inc., band-pass filters. The filter should be connected directly to the evaluation board.

OUTPUT SIGNALS

The default setup uses the HSC-ADC-FPGA-8 high speed deserialization board to deserialize the digital output data and convert it to parallel CMOS. These two channels interface directly with the Analog Devices standard dual-channel FIFO data capture board (HSC-ADC-EVALB-DC). Two of the eight channels can then be evaluated at the same time. For more information on channel settings on these boards and their optional settings, visit www.analog.com/FIFO.

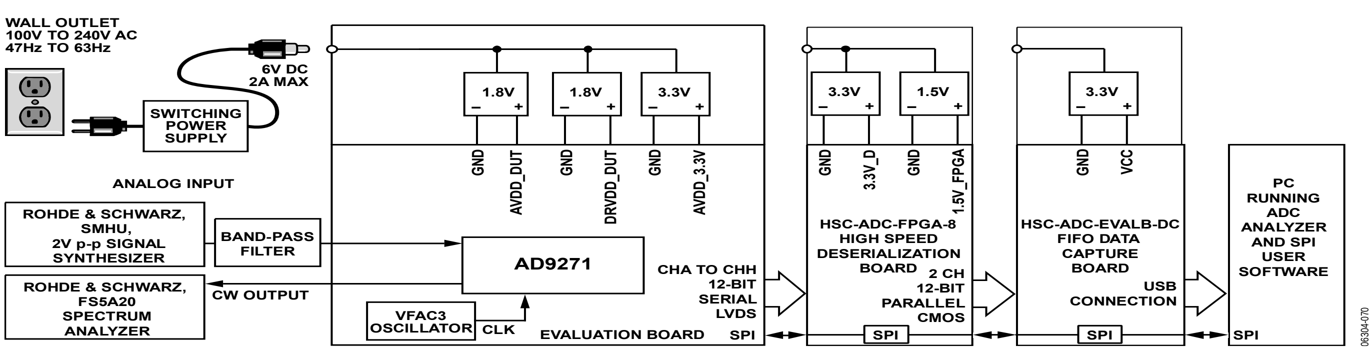

Figure 65. Evaluation Board Connection

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DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

The following is a list of the default and optional settings or modes allowed on the AD9271 Rev. A evaluation board.

- POWER: Connect the switching power supply that is supplied in the evaluation kit between a rated 100 V ac to 240 V ac wall outlet at 47 Hz to 63 Hz and P701.
- AIN: The evaluation board is set up for a transformer-coupled analog input with optimum 50 Ω impedance matching out to 18 MHz (see Figure 66). For a different bandwidth response, change the 22 pF capacitor at the LNA (LI-x) analog input.

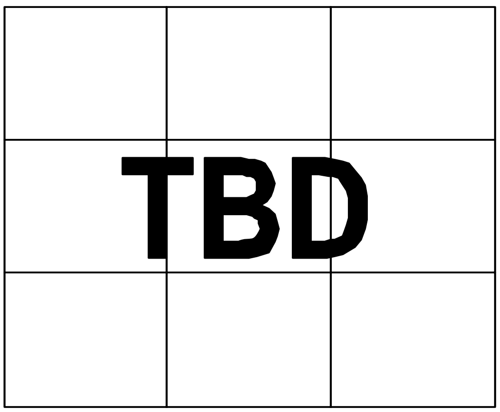

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Figure 66. Evaluation Board Full Power Bandwidth

- VREF: VREF is set to 1.0 V by tying the SENSE pin to ground, R317. This causes the ADC to operate in 2.0 V p-p full-scale range. A separate external reference option using the ADR510 or ADR520 is also included on the evaluation board. Populate R311 and R315 with 0 Ω resistors and remove C307. Proper use of the VREF options is noted in the Voltage Reference section.
- RBIAS: RBIAS has a default setting of 10 kΩ (R301) to ground and is used to set the ADC core bias current. To further lower the core power (excluding the LVDS driver supply), change the resistor setting. However, performance of the ADC may degrade depending on the resistor chosen. See RBIAS section for more information.
- CLOCK: The default clock input circuitry is derived from a simple transformer-coupled circuit using a high bandwidth 1:1 impedance ratio transformer (T401) that adds a very low amount of jitter to the clock path. The clock input is 50 Ω terminated and ac-coupled to handle single-ended sine wave types of inputs. The transformer converts the single-ended input to a differential signal that is clipped before entering the ADC clock inputs.

  The evaluation board is already set up to be clocked from the crystal oscillator, OSC401. This oscillator is a low phase noise oscillator from Valpey Fisher (VFAC3-BHL-50MHz). If a different clock source is desired, remove R403, set Jumper J401 to disable the oscillator from running, and connect the external clock source to the SMA connector, P401.

  A differential LVPECL clock driver can also be used to clock the ADC input using the AD9515 (U401). Populate R406 and R407 with 0 Ω resistors and remove R415 and R416 to disconnect the default clock path inputs. In addition, populate C405 and C406 with a 0.1 μF capacitor and remove C409 and C410 to disconnect the default cloth path outputs. The AD9515 has many pin-strappable options that are set to a default mode of operation. Consult the AD9515 data sheet for more information about these and other options.

- PDWN: To enable the power-down feature, short P303 to the on position (AVDD) on the PDWN pin.
- STDBY: To enable the standby feature, simply short P302 to the on position (AVDD) on the STDBY pin.
- GAIN: To change the gain on the VGA, drive these pins from 0 V to 1 V on J301. This changes the VGA gain from 0 dB to 30 dB. This feature can also be driven from the R335 and R336 on-board resistive dividers by installing a 0 Ω resistor in R337.
- Non-SPI Mode: For users who wish to operate the DUT without using SPI, remove the jumpers on J501. This disconnects the CSB, SCLK, and SDIO pins from the control bus, allowing the DUT to operate in its simplest mode. Each of these pins has internal termination and will float to its respective level. Note that the device will only work in its default condition.
- CWD+,CWD−: To view muiltple CW outputs, jumper together the appropriate outputs on P403 and P404. All outputs are summed together on IOP and ION buses, fed to a 1:4 impedance ratio transformer, and buffered so that the user can view the output on a spectrum analyzer. This can be configured to be viewed in single-ended mode (default) or in differential mode. To set the voltage for the appropriate number of channels to be summed, change the value of R447 and R448 on the primary transformer (T402).
- D+, D−: If an alternative data capture method to the setup described in Figure 67 is used, optional receiver terminations, R318, R320 to R330, can be installed next to the high speed backplane connector.

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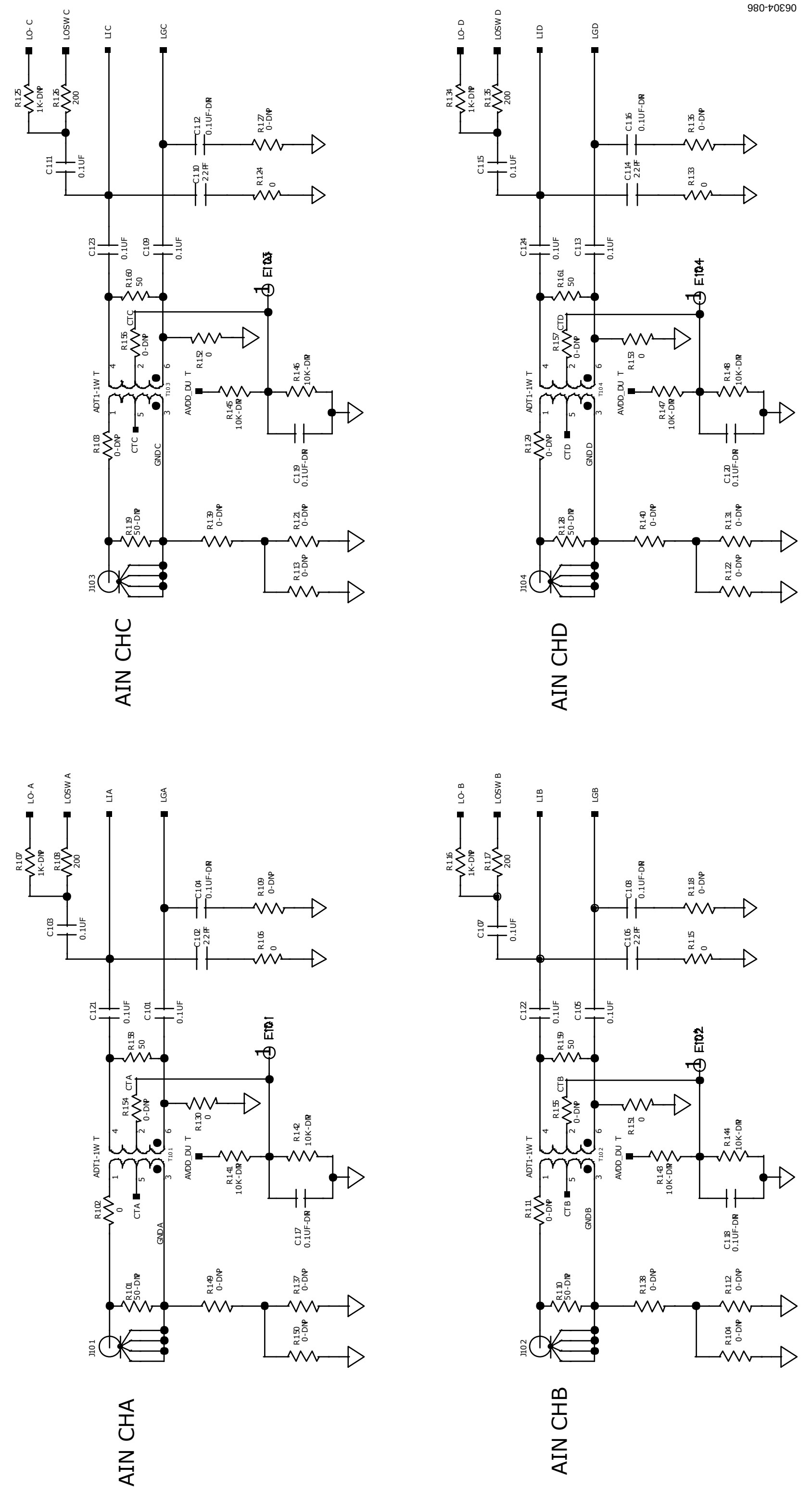

Figure 67. Evaluation Board Schematic, DUT Analog Inputs

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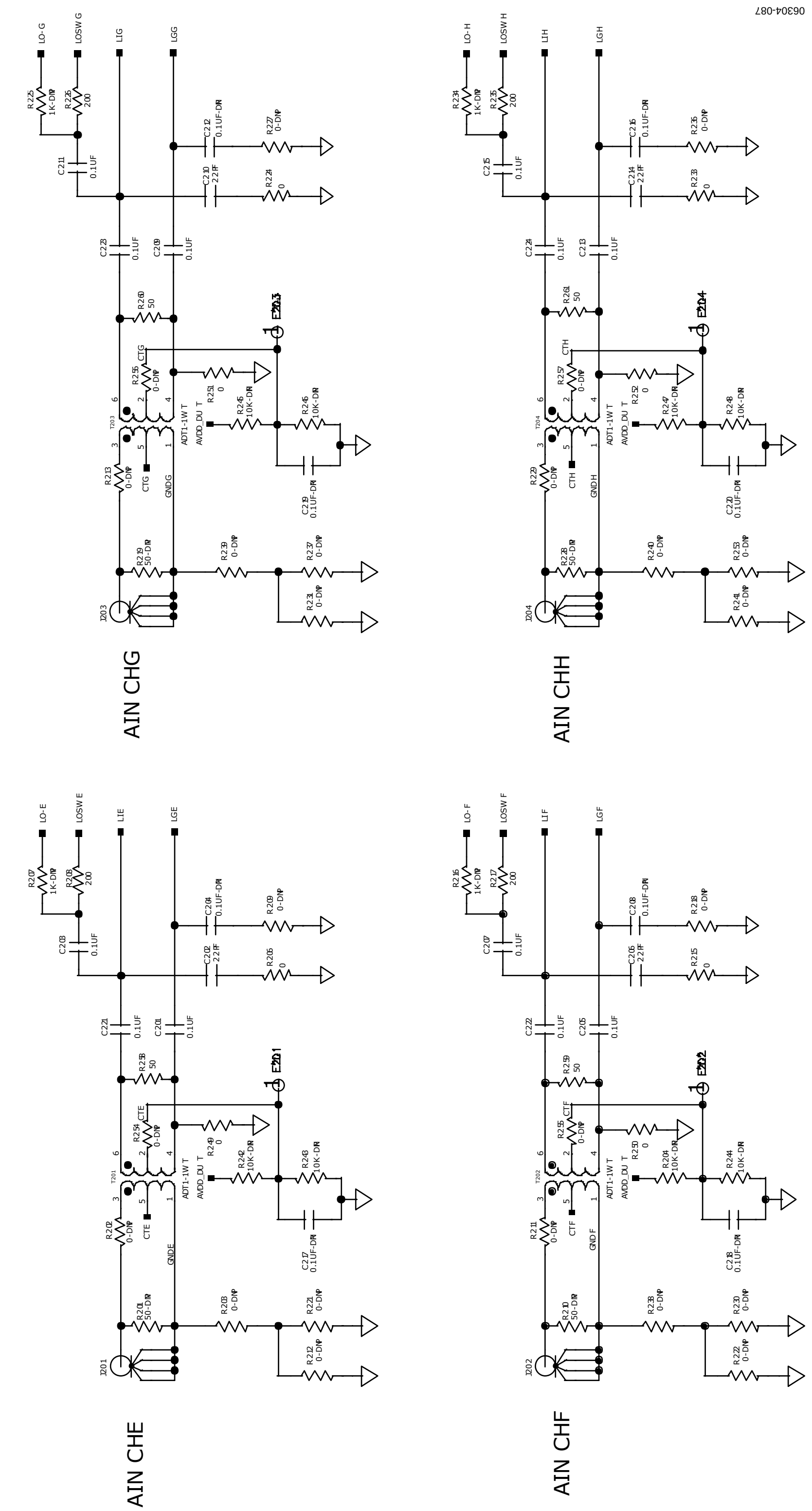

Figure 68. Evaluation Board Schematic, DUT Analog Inputs (Continued)

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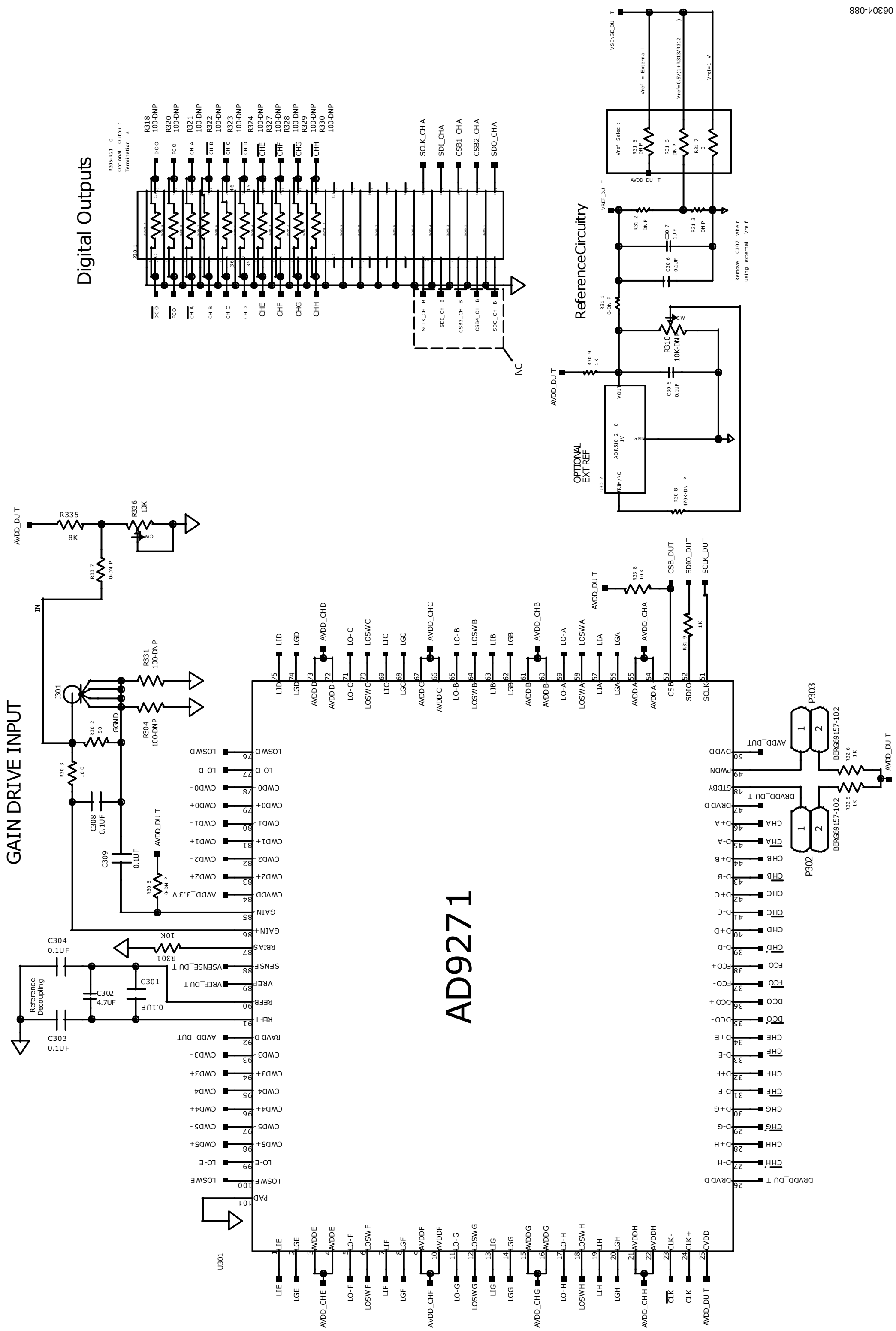

Figure 69. Evaluation Board Schematic, DUT, VREF, and Digital Output Interface

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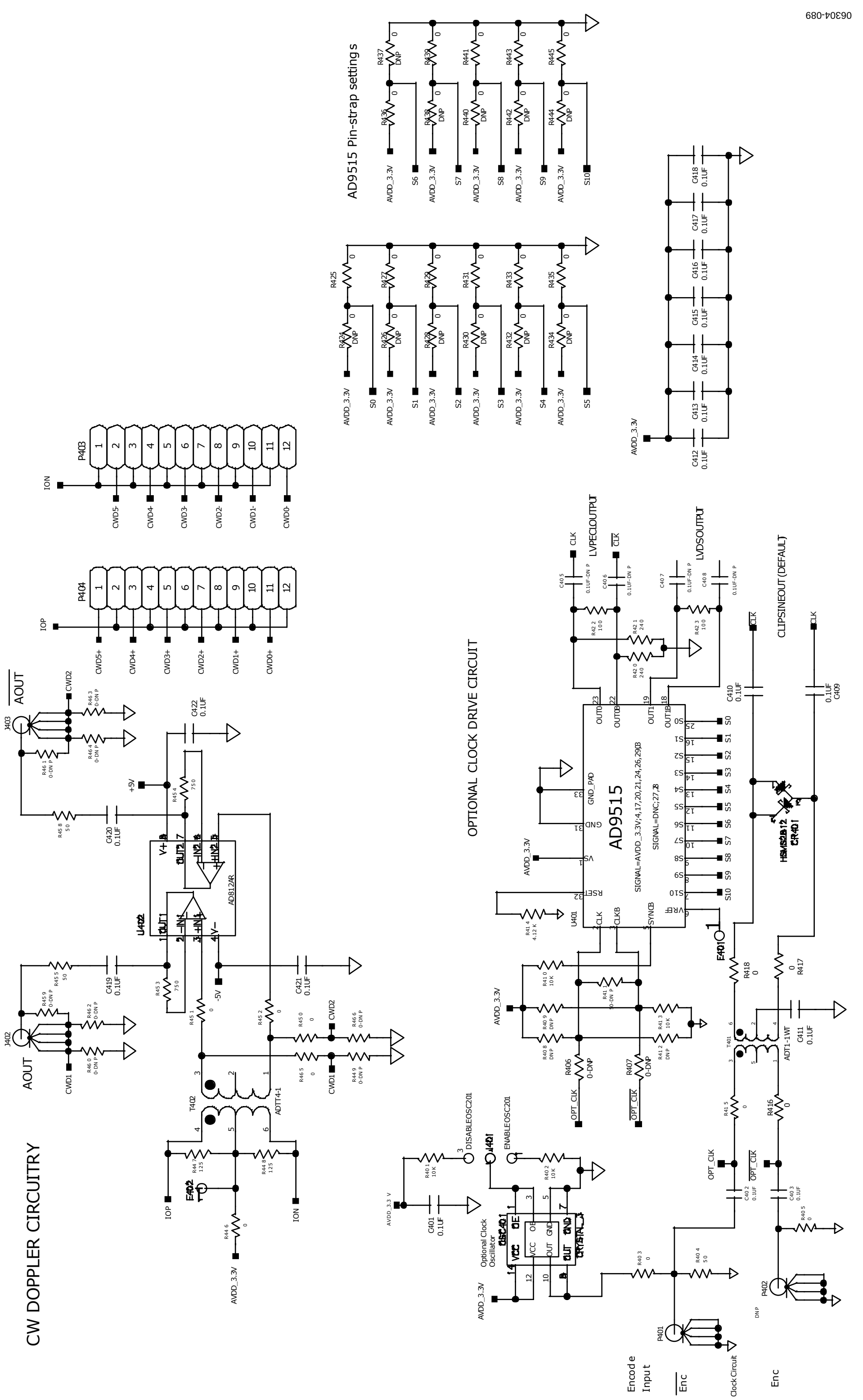

Figure 70. Evaluation Board Schematic, Clock and CW Doppler Circuitry

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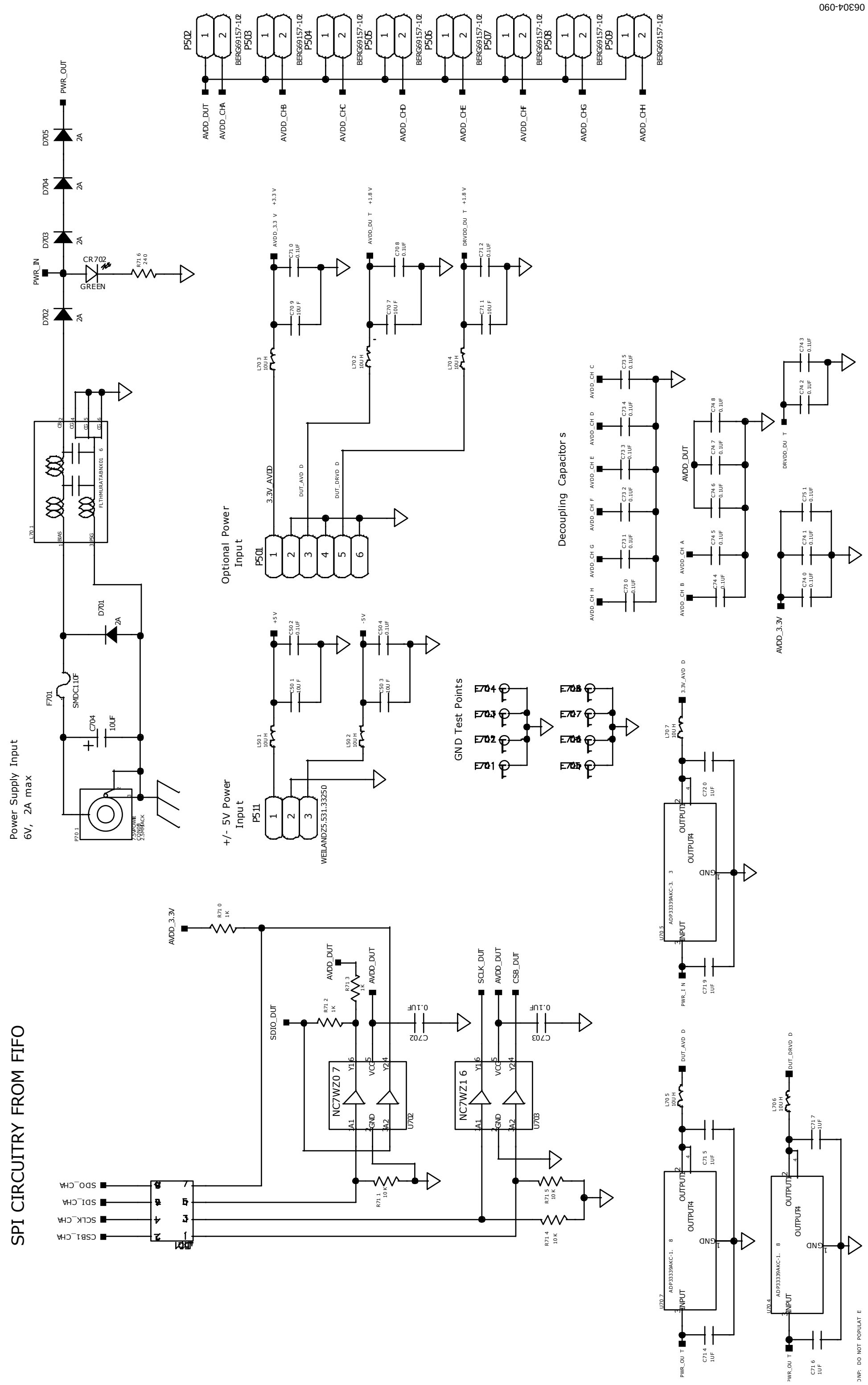

Figure 71. Evaluation Board Schematic, Power Supply Inputs and SPI Interface Circuitry

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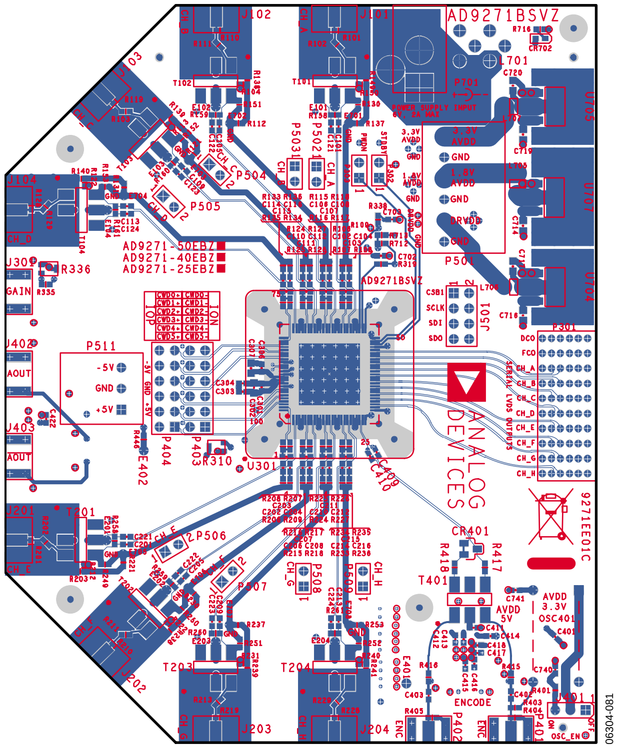

Figure 72. Evaluation Board Layout, Top Side

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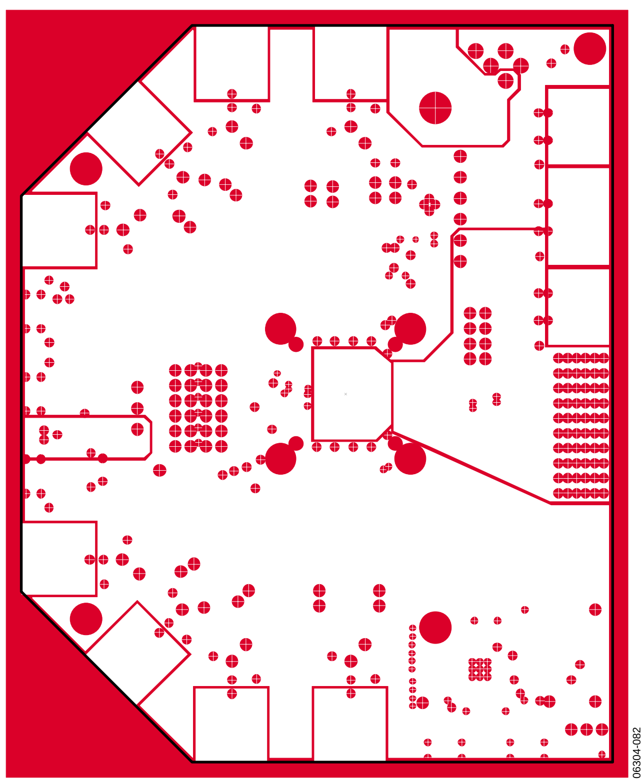

Figure 73. Evaluation Board Layout, Ground Plane (Layer 2)

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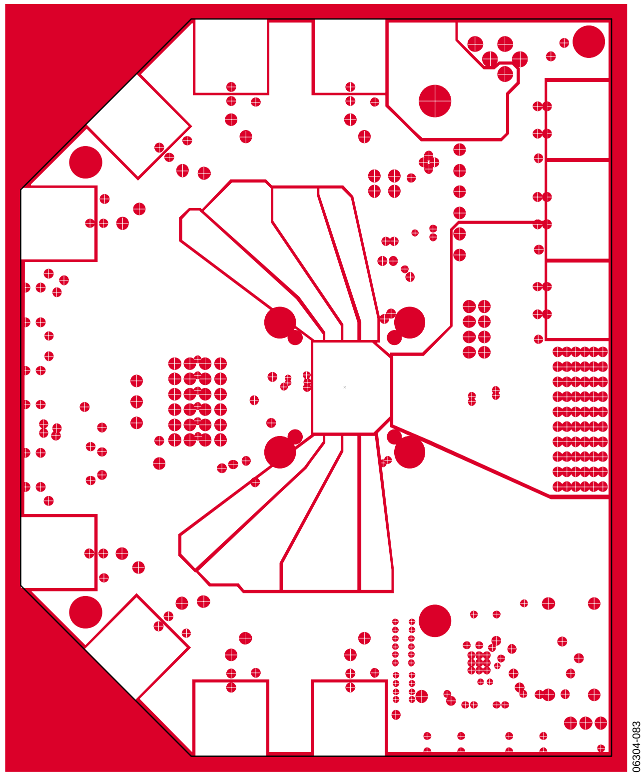

Figure 74. Evaluation Board Layout, Power Plane (Layer 3)

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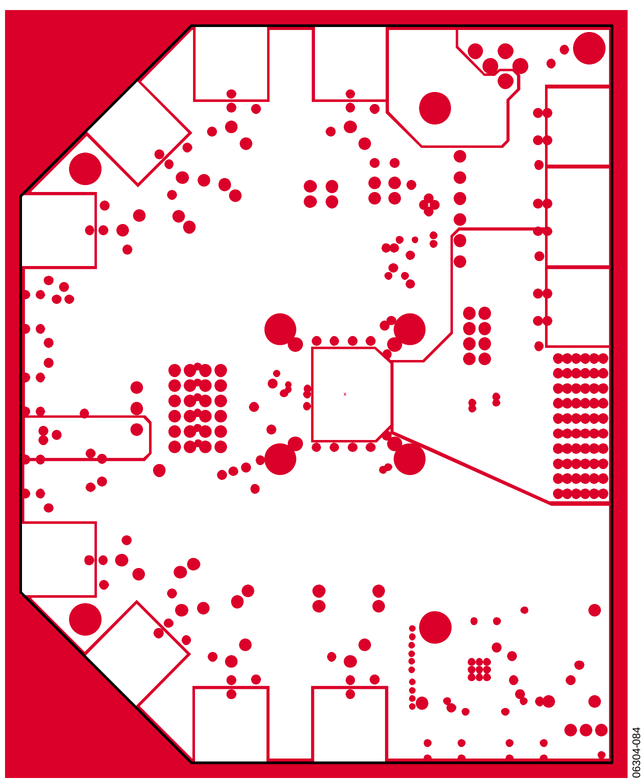

Figure 75. Evaluation Board Layout, Power Plane (Layer4)

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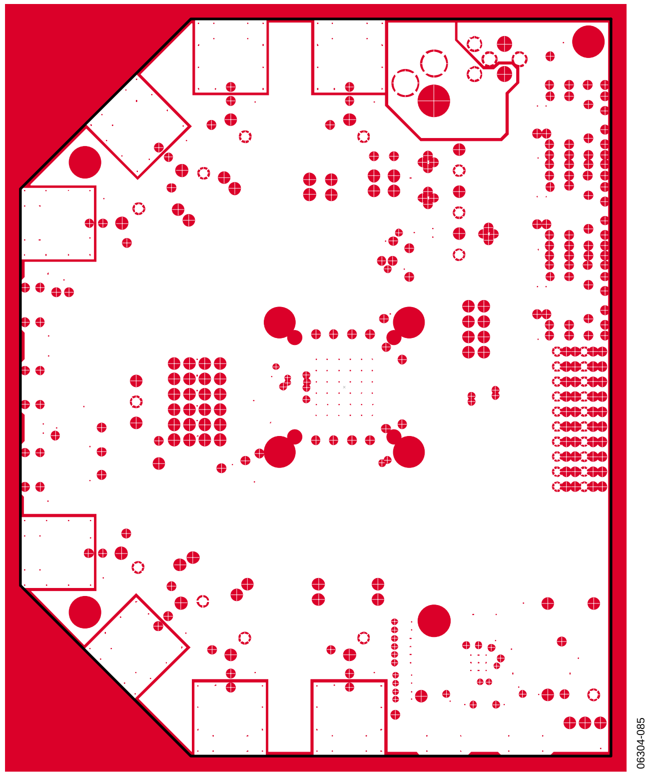

Figure 76. Evaluation Board Layout, Ground Plane (Layer 5)

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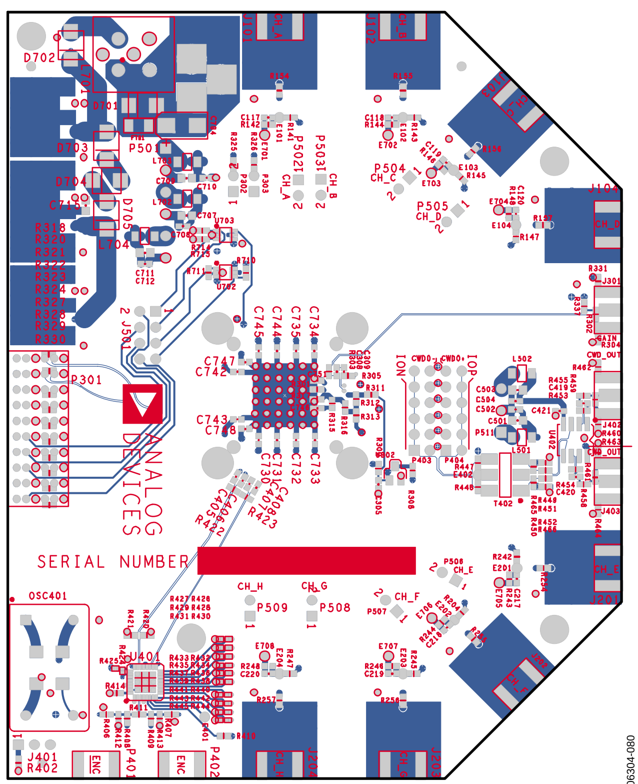

Figure 77. Evaluation Board Layout, Bottom Side

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Table 17. Evaluation Board Bill of Materials (BOM)[1]

Item	Qnty. per Board	REFDES	Device	Pkg.	Value	Mfg.	Mfg. Part Number
1	1	AD9271BSVZ_REVC	PCB	PCB	PCB		
2	71	C101, C103, C105, C107, C109, C111, C113, C115, C121 to C124, C201, C203, C205, C207, C209, C211, C213, C215, C221 to C224, C301, C303 to C306, C308 to C309, C401 to C403, C409 to C422, C502, C504, C702 to C703, C708, C710, C712, C730 to C735, C740 to C748, C751	Capacitor	C0402	0.1 µF 10 V ceramic X5R 0402	Panasonic	ECJ-0EB1A104K
3	8	C102, C106, C110, C114, C202, C206, C210, C214	Capacitor	C0402	Ceramic 22 pF 5% 50 V NP0 0402	AVX	04025A220JAT2A
4	1	C302	Capacitor	C0603	Ceramic 4.7 µF 6.3 V X5R 0603	AVX	C0603C475K9PACTU
5	7	C307, C714 to C717, C719 to C720	Capacitor	C0603	1 µF 6.3 V ceramic X5R 0603	Panasonic	ECJ-1VB0J105K
6	5	C501, C503, C707, C709, C711	Capacitor	C0603	Ceramic 10 µF 6.3 V X5R 0603	Panasonic	ECJ-1VB0J106M
7	1	C704	Capacitor	C6032	10 µF, 6032-28, tantalum, 16 V, 10% tol	Kemet	T491C106K016AS
8	1	CR401	Diode	SOT23	Schottky GP LN 20 mA	AVAGO (Agilent)	HSMS-2812-TR1G
9	1	CR702	LED	LED0603	Green USS Type 0603 4 V, 5 m candela	Panasonic	LNJ314G8TRA
10	5	D701 to 705	Diode	SMBJ	Rectifier SIL 2 A 50 V DO-214AA	Micro Commercial Co.	S2A-TP
11	1	F701	Fuse		Polyswitch 1.10 A reset fuse SMD	Tyco/Raychem	NANOSMDC110F-2
12	13	J101 to J104, J201 to J204, J301, J402 to J403, P401 to P402	Connector	CNSAMTEC-SMA-J-	CONN-PCB coax SMA end launch	Samtec/Johnson	SMA-J-P-X-ST-EM1/ 142-0711-821
13	1	J401	Connector	CNBERG1X3H205LD	Header, 3-pin, male, single row, straight	Samtec	TSW-103-08-G-S
14	1	J501	Connector	CNBERG2X4H350LD	Header, 8-pin, male, double row, straight	Samtec	TSW-105-08-T-D

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Item	Qnty. per Board	REFDES	Device	Pkg.	Value	Mfg.	Mfg. Part Number
15	10	P302 to P303, P502 to P509	Connector	CNBERG69157-102	100 mil header jumper, 2-pin	Samtec	TSW-102-07-G-S
16	2	P403 to P404	Connector	CNBERG2X6H330LD	100 mil header, male, 2 × 6 double row straight	Samtec	TSW-110-08-G-D/ TSW-106-08-G-D
17	8	L501 to L502, L702 to L707	Ferrite Bead	L1210	Bead core 3.2 × 2.5 × 1.6 SMD 1210, 10 μH	Panasonic	EXC-CL3225U1
18	1	L701	Choke coil		Filter, BNX016-01, EMIFIL LC block	Murata	BNX016-01
19	1	OSC401	Oscillator	OSC14P4_CB3	Crystal, dual footprint, see eng	Valpey Fisher	VFAC3-BHL-50MHz
20	1	P301	Connector		Header, right angle, 2-pair, 25 mm, header assembly	Tyco/AMP	6469169-1
21	1	P701	Connector	0.08", PCMT	DC power, PC mount	Switchcraft	RAPC722X
23	38	R102, R103, R106, R111, R115, R124, R129, R130, R133, R151, R152, R153, R202, R206, R211, R213, R215, R224, R229, R233, R249 R252, R305, R317, R403, R405, R415 to R418, R446, R450 to R452, R465, R466	Resistor	R0402	0 Ω 1/16 W 5% 0402 SMD	Panasonic	ERJ-2GE0R00X
24	8	R108, R117, R126, R135, R208, R217, R226, R235	Resistor	R0402	200 Ω 1/16 W 0.5% 0402 SMD	Yageo America	RR0510P-201-D
25	12	R158 to R161, R258 to R261, R302, R404, R455, R458	Resistor	R0402	49.9 Ω 1/16 W 0.5% 0402 SMD	Susumu Co.	RR0510R-49R9-D
26	9	R301, R338, R401 to R402, R410, R413, R711, R714 to R715	Resistor	R0402	10 kΩ 1/16 W 5% 0402 SMD	Panasonic	ERJ-2GEJ103X
27	3	R303, R422 to R423	Resistor	R0402	100 Ω 1/16 W 1% 0402 SMD	Panasonic	ERJ-2RKF1000V
28	1	R308	Resistor	R0402	470 kΩ 1/16 W 5% 0402 SMD	Panasonic	RC0402JR-07470KL
29	7	R309, R319, R325, R326, R710, R712, R713	Resistor	R0402	1.00 kΩ 1/16 W 1% 0402 SMD	Panasonic	ERJ-2RKF1001X
30	1	R335	Resistor	R0402	8.06 kΩ 1/16 W 1% 0402 SMD	Yageo	RC0402FR-078K06L

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Item	Qnty. per Board	REFDES	Device	Pkg.	Value	Mfg.	Mfg. Part Number
31	2	R310, R336	Potentiometer	3-lead	10 kΩ, one turn, SMT	Murata	PVA2A103A01R00
32	1	R414	Resistor	R0402	4.12 kΩ 1/16 W 1% 0402 SMD	Panasonic	ERJ-2RKF4121X
33	3	R420 to R421, R716	Resistor	R0402	Thick film, SMT 0402, 240		
34	11	R424, R427, R429, R431, R433, R435 to R436, R439, R441, R443, R445	Resistor	R0201	0.0 Ω 1/20 W 5% 0201 SMD	Panasonic	ERJ-1GE0R00C
35	2	R447 to R448	Resistor	R0402	124 Ω 1/16 W 0.1% 0402 SMD	Susumu Co.	RG10P124BCT-ND
36	2	R453 to R454	Resistor	R0402	750 Ω 1/16 W 0.1% 0402 SMD	Susumu Co.	RG10P750BCT-ND
37	9	T101 to T104, T201 to T204, T401	Transformer	MINICD542	XFMR RF	Mini Circuits	ADT1-1WT
38	1	T402	Transformer	MINICKCD637	ADTT4-1, CD542	Mini Circuits	ADTT4-1
39	1	U301	IC	SV-100-3	Octal LNA/ VGA/AAF/ADC	Analog Devices	AD9271BSVZ
40	1	U302	IC	SOT23	ADR510, 1.0 V precision low noise shunt V REF	Analog Devices	ADR510
41	1	U401	IC	LFCSP32-5X5-LP	AD9515, CLK DIST, 32 LFCSP, 5 × 5 mm	Analog Devices	AD9515
42	1	U402	IC	SO8	AD812AR, dual, current feedback op amp, SO8	Analog Devices	AD812AR
43	1	U702	IC	SC88	NC7WZ07, dual buffer, SC88	Fairchild	NC7WZ07P6X_NL
44	1	U703	IC	SC88	NC7WZ16P6X, UHS dual buffer, SC88	Fairchild	NC7WZ16P6X_NL
45	2	U704, U707	IC	SOT223-2	Regulator, high accuracy, ADP3339AKC-1.8, 1.8 V	Analog Devices	ADP3339AKC-1-8
46	1	U705	IC	SOT223-2	Regulator, high accuracy, ADP3339AKC-3.3, 3.3 V	Analog Devices	ADP3339AKC-3-3

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Item	Qnty. per Board	REFDES	Device	Pkg.	Value	Mfg.	Mfg. Part Number
47	4	MP101 to MP104	Assembly	Insert into four large holes on corners of board from the bottom side	CBSB-14-01, 7/8" height, standoffs for circuit board support, no adhesive	Richco	CBSB-14-01
48	6	MP105 to MP108	Assembly	Place into J502-509	SNT-100-BK-G-H, 100 mil jumpers	Samtec	SNT-100-BK-G-H

[1] This BOM is RoHS compliant.

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OUTLINE DIMENSIONS

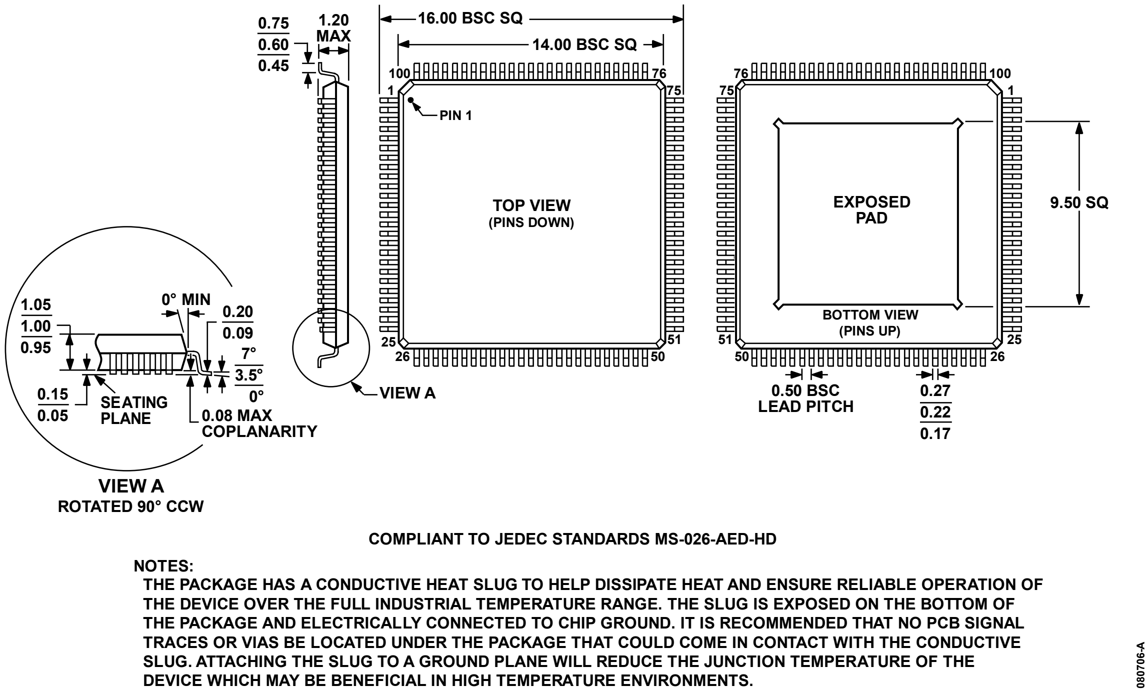

Figure 78. 100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-100-3)
Dimensions shown in millimeters

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ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9271BSVZ-50[1]	–40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-100-3
AD9271BSVZRL7-50[1]	–40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP] Tape and Reel	SV-100-3
AD9271BSVZ-40[1]	–40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-100-3
AD9271BSVZRL7-40[1]	–40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP] Tape and Reel	SV-100-3
AD9271BSVZ-25[1]	–40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-100-3
AD9271BSVZRL7-25[1]	–40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP] Tape and Reel	SV-100-3
AD9271-50EBZ[1]		Evaluation Board	

[1] Z = Pb-free part.

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