Ordering number : EN7637

SANYO Semiconductors
DATA SHEET

# LA75695VA — Monolithic Linear IC For Use in TV/VTR Applications IF Signal Processing (VIF+SIF+SIF converter)

## Overview

The LA75695VA is a NTSC Support VIF/SIF signal-processing IC that makes the minimum number of adjustments possible. The system is designed so that VCO adjustment makes AFT adjustment unnecessary, thus simplifying the adjustment steps in endproduct manufacturing. PLL detection is adopted in the FM detector, allowing the LA75695VA to support multichannel detection for the audio signal. In addition, it also incorporates a buzz canceller that suppresses Nyquist buzz for improved audio quality.

## Functions

- VIF Block: VIF Amplifier, Buzz Canceller, PLL Detector, IF AGC, RF AGC, AFT, Equalizer Amplifier
- 1st SIF Block: 1st SIF Amplifier, 1st SIF Detector
- SIF Block: Limiter Amplifier, PLL-FM Detector

## Specifications

### Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{CC}1$ max | | 6 | V |
| | $V_{CC}2$ max | | 12 | V |
| Circuit voltage | $V_{13}$, $V_{17}$ | | $V_{CC}$ | V |
| Circuit current | $I_6$ | | -3 | mA |
| | $I_{10}$ | | -10 | mA |
| | $I_{24}$ | | -2 | mA |
| Allowable power dissipation | Pd max | Ta ≤ 70°C, Mounted on a board. * | 600 | mW |
| Operating temperature | Topr | | -20 to +75 | °C |
| Storage temperature | Tstg | | -55 to +150 | °C |

* When mounted on a 114.3×76.1×1.6mm$^3$, glass epoxy circuit board.




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## Recommended Operating Conditions at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Recommended supply voltage | $V_{CC}1$ | | 5 | V |
| | $V_{CC}2$ | | 9 | V |
| Operating voltage | $V_{CC}1$ op | | 4.5 to 5.5 | V |
| | $V_{CC}2$ op | | 4.5 to 9.5 | V |

## Electrical Characteristics at Ta = 25°C, $V_{CC}1$ = 5V, $V_{CC}2$ = 9V, fp = 45.75MHz

### VIF Block

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Circuit current 1 | $I_5$ | | 35.7 | 42 | 48.3 | mA |
| Circuit current 2 | $I_4$ | | 6.7 | 7.9 | 9.1 | mA |
| Maximum RF AGC voltage | $V_{14}H$ | | $V_{CC}2$-0.5 | $V_{CC}2$ | | V |
| Minimum RF AGC voltage | $V_{14}L$ | | | 0 | 0.5 | V |
| Input sensitivity | $V_i$ | S1 = OFF | 30 | 36 | 42 | dBμV |
| AGC range | GR | | 50 | 56 | | dB |
| Maximum allowable input | $V_i$ max | | 95 | 100 | | dBμV |
| No-signal video output voltage | $V_6$ | | 3.1 | 3.4 | 3.7 | V |
| Sync. signal tip voltage | $V_6$ tip | | 0.8 | 1.1 | 1.3 | V |
| Video output level | $V_O$ | | 1.7 | 2.0 | 2.3 | Vp-p |
| Black noise threshold voltage | $V_{BTH}$ | | 0.5 | 0.8 | 1.1 | V |
| Black noise clamp voltage | $V_{BCL}$ | | 1.7 | 2.1 | 2.4 | V |
| Video S/N | S/N | | 48 | 52 | | dB |
| C-S best | IC-S | | 38 | 43 | | dB |
| Frequency characteristics | $f_C$ | 6MHz | -3 | -1.5 | | dB |
| Differential gain | DG | | | 3 | 6.5 | % |
| Differential phase | DP | | | 3 | 5 | °C |
| No-signal AFT voltage | $V_{13}$ | | 2.0 | 2.5 | 3.0 | V |
| Maximum AFT voltage | $V_{13}H$ | | $V_{CC}2$-1.0 | $V_{CC}2$-0.5 | $V_{CC}2$ | V |
| Minimum AFT voltage | $V_{13}L$ | | 0 | 0.18 | 1.0 | V |
| AFT detection sensitivity | Sf | | 17 | 25 | 34 | mV/kHz |
| VIF input resistance | $R_i$ | 45.75MHz | | 1.5 | | kΩ |
| VIF input capacitance | $C_i$ | 45.75MHz | | 3 | | pF |
| APC pull-in range (U) | fpu | | 0.7 | 1.5 | | MHz |
| APC pull-in range (L) | fpl | | | -1.5 | -0.9 | MHz |
| AFT tolerance frequency 1 | ΔFa1 | | -150 | 0 | 150 | kHz |
| VCO1 maximum variable range (U) | dfu | | 1.0 | 1.5 | | MHz |
| VCO1 maximum variable range (L) | dfl | | | -1.5 | -1 | MHz |
| VCO control sensitivity | β | | 1.2 | 3.2 | 5.0 | kHz/mV |
| Synchronization ratio | $V_S$ | | 25.0 | 28.5 | 31.5 | % |

### 1st SIF Block

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Conversion gain | $V_G$ | | 22 | 28 | 32 | dB |
| 4.5MHz output level | $S_O$ | | 80 | 120 | 160 | mVrms |
| 1st SIF maximum input | $S_i$ max | | 50 | 100 | | mVrms |
| 1st SIF input resistance | $R_i$ (SIF) | 41.25MHz | | 2 | | kΩ |
| 1st SIF input capacitance | $C_i$ (SIF) | 41.25MHz | | 3 | | pF |

SIF Block

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Limiting sensitivity | $V_i$ (lim) | | 48 | 52 | 58 | dBμV |
| FM detector output voltage | $V_O$ (FM) | 4.5MHz±25kHz * | 420 | 500 | 620 | mVrms |
| AM rejection ratio | AMR | | 50 | 60 | | dB |
| Distortion | THD | | | 0.3 | 0.8 | % |
| SIF S/N | S/N (FM) | | 63 | 69 | | dB |

* IF the dynamic range of the FM detection output needs to be widened, connect a resistor and a capacitor in series between pin 23 and GND for level adjustment.

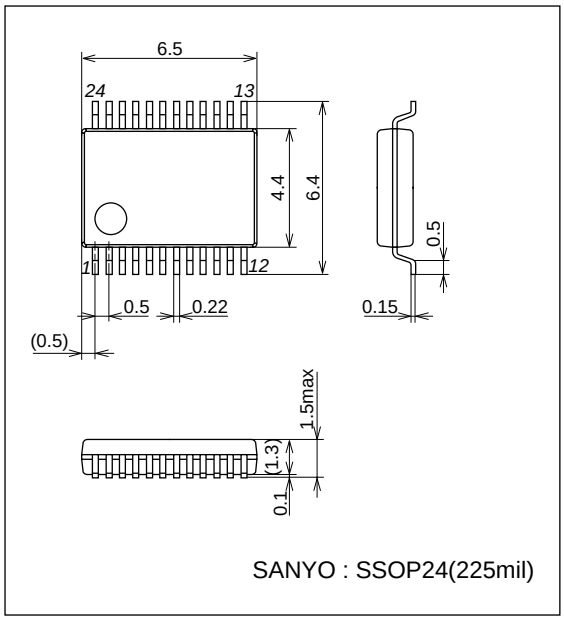
SIF Converter

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Maximum output level | V max | | 110 | 116 | 122 | dBμV |

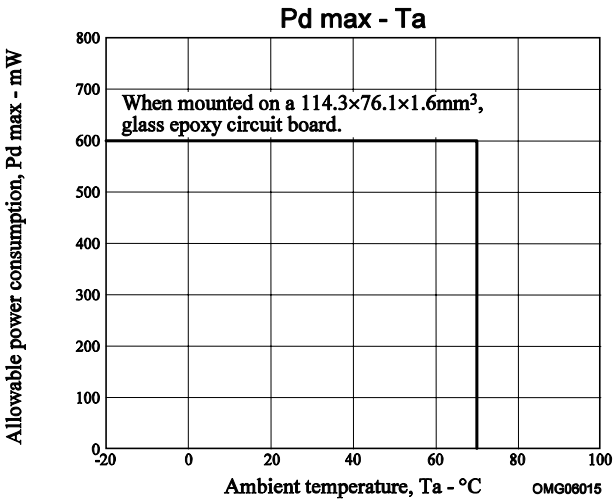
## Package Dimensions

unit : mm

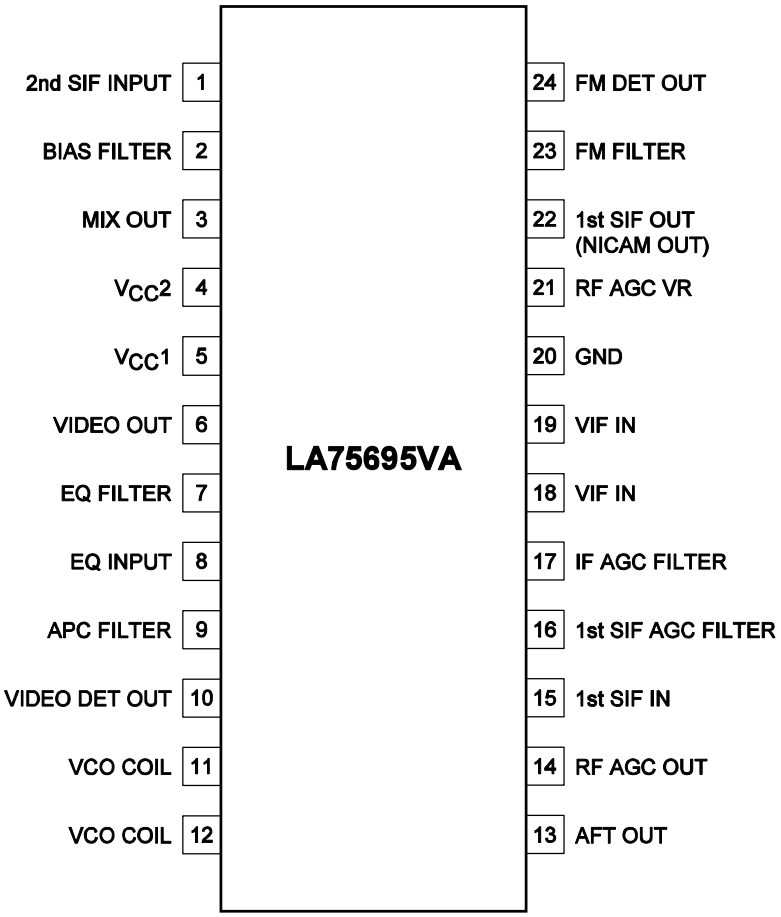
3287




SANYO : SSOP24(225mil)



## Pin Assignment




Top view

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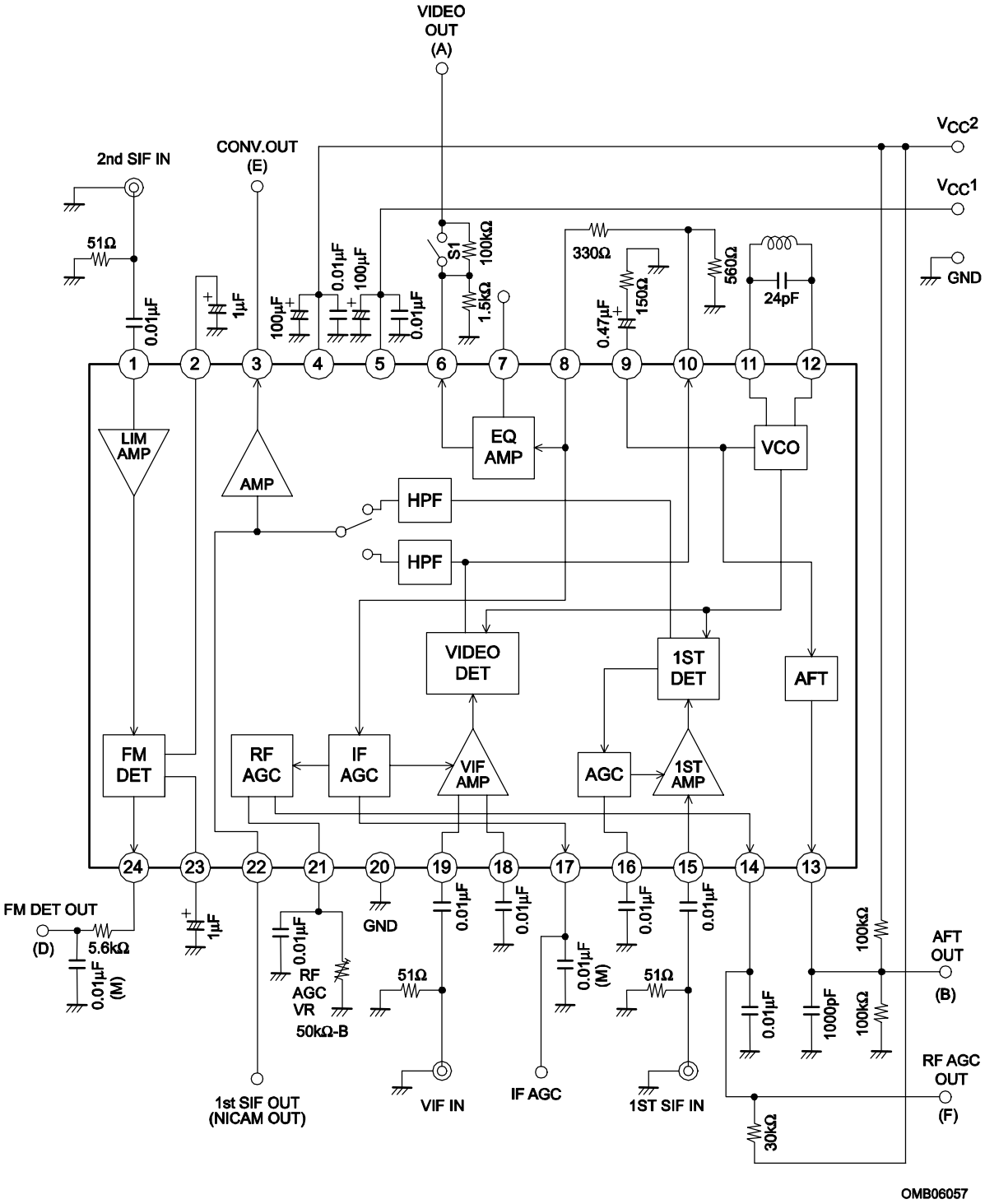
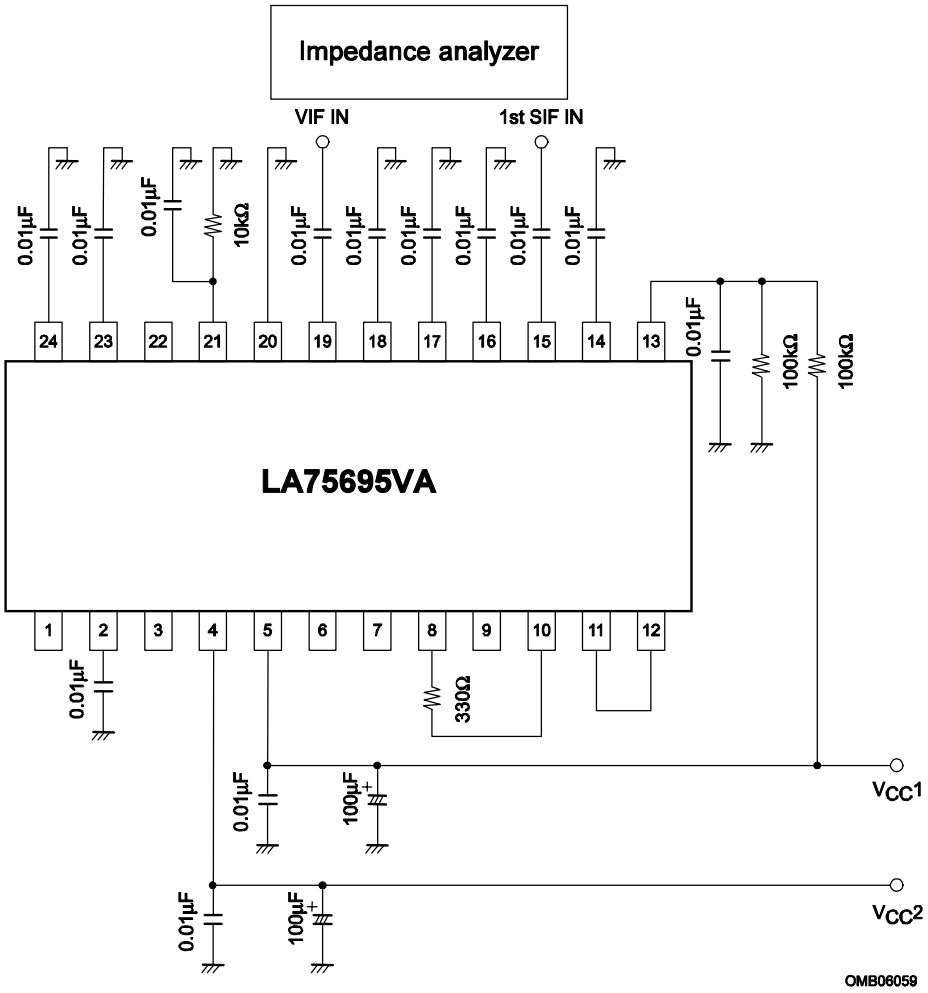
## Block Diagram and AC Characteristics Test Circuit



## Input Impedance Test Circuit




## Test Conditions

V1. Circuit current [$I_5$]
(1) Internal AGC
(2) Input a 45.75MHz 10mVrms continuous wave to the VIF input pin.
(3) RF AGC Vr MAX
(4) Connect an ammeter to the $V_{CC}1$ and measure the incoming current.

V2. Circuit current [$I_4$]
(1) Internal AGC
(2) Input a 45.75MHz 10mVrms continuous wave to the VIF input pin.
(3) RF AGC Vr MAX
(4) Connect an ammeter to the $V_{CC}2$ and measure the incoming current.

V3. V4. Maximum RF AGC voltage, Minimum RF AGC voltage [$V_{14}H$, $V_{14}L$]
(1) Internal AGC
(2) Input a 45.75MHz 10mVrms continuous wave to the VIF input pin.
(3) Adjust the RF AGC Vr (resistor value max.) and measure the maximum RF AGC voltage. ····· F
(4) Adjust the RF AGC Vr (resistor value min.) and measure the minimum RF AGC voltage. ····· F

V5. Input sensitivity [Vi]
(1) Internal AGC
(2) fp = 45.75MHz 15kHz 78% AM (VIF input)
(3) Turn off the S1 and put 100kΩ through.
(4) VIF input level at which the 15kHz detection output level at test point A becomes $V_O$ -3dB.

V6. AGC range [GR]

(1) Apply the $V_{CC}$ voltage to the external AGC, IF AGC (pin 17).
(2) In the same manner as for the V5 (input sensitivity), measure the VIF input level at which the detection output level becomes Vo -3dB. ····· Vil
(3) GR = Vil–Vi

V7. Maximum allowable input [Vi max]

(1) Internal AGC
(2) fp = 45.75MHz 15kHz 78% AM (VIF input)
(3) VIF input level at which the detection output level at test point A is video output ($V_O$) ±1dB.

V8. No-signal video output voltage [$V_6$]

(1) Apply the $V_{CC}$ voltage to the external AGC, IF AGC (pin 17).
(2) Measure the DC voltage of VIDEO output (A).

V9. Sync. signal tip voltage [$V_6$tip]

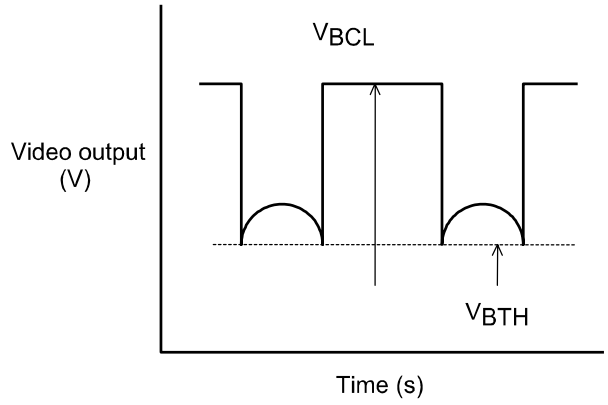
(1) Internal AGC
(2) Input a 45.75MHz 10mVrms continuous wave to the VIF input pin.
(3) Measure the DC voltage of VIDEO output (A).

V10. Video output level [$V_O$]

(1) Internal AGC
(2) fp = 45.75MHz 15kHz 78% AM $V_i$ = 10mVrms (VIF input)
(3) Measure the peak value of the detection output level at test point A. (Vp-p)

V11.V12. Black noise threshold level and clamp voltage [$V_{BTH}$, $V_{BCL}$]

(1) Apply DC voltage to the external AGC, IF AGC (pin 17) and adjust the voltage.
(2) fp = 45.75MHz 400Hz 40% AM 10mVrms (VIF input)
(3) Adjust the IF AGC (pin 17) voltage to operate the noise canceller.
Measure the $V_{BTH}$, $V_{BCL}$ at test point A.

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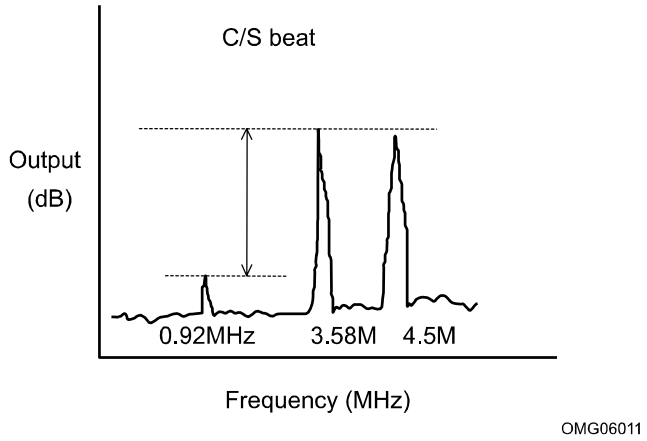
V13. Video S/N [S/N]

(1) Internal AGC
(2) fp = 45.75MHz CW = 10mVrms (VIF input)
(3) Measure the noise voltage at test point A in RMS volts through a 10kHz to 4MHz band-pass filter.
····· Noise voltage (N)
(4) $S/N = 20\log \frac{\text{Video portion (Vp-p)}}{\text{Noise voltage (Vrms)}} = 20\log \frac{1.12\text{Vp-p}}{\text{Noise voltage (Vrms)}}$ (dB)

V14. C/S beat [IC-S]

(1) Apply DC voltage to the external AGC IF AGC (pin 17) and adjust the voltage.
(2) fp = 45.75MHz CW; 10mVrms
fc = 42.17MHz CW; 10mVrms – 10dB
fs = 41.25MHz CW; 10mVrms – 10dB
(3) Adjust the IF AGC (pin 17) voltage so that the output DC level at test point A becomes 2.4V.
(4) Measure the difference between the levels for 3.58MHz and 0.92MHz components at test point A.




V15. Frequency characteristics [fc]

(1) Apply DC voltage to the external AGC IF AGC (pin 17) and adjust the voltage.
(2) SG1 : 45.75MHz continuous wave 10mVrms
SG2 : 45.65MHz to 39.75MHz continuous wave 2mVrms
Add the SG1 and SG2 signals using a T pat and adjust each SG signal level so that the above-mentioned levels are reached and input the added signals to the VIF IN.
(3) First set the SG2 frequency to 45.65MHz, and then adjust the IF AGC voltage (V17) so that the output level at test point A becomes 0.5Vp-p. ····· V1
(4) Set the SG2 frequency to 39.75MHz and measure the output level. ····· V2
(5) Calculate as follows :

$$fc = 20\log \frac{V2}{V1} \text{ (dB)}$$

V16.V17. Differential gain, differential phase [DG, DP]

(1) Internal AGC
(2) fp = 45.75MHz APL50% 87.5% modulation video signal $V_i$ = 10mVrms
(3) Measure the DG and DP at test point A.

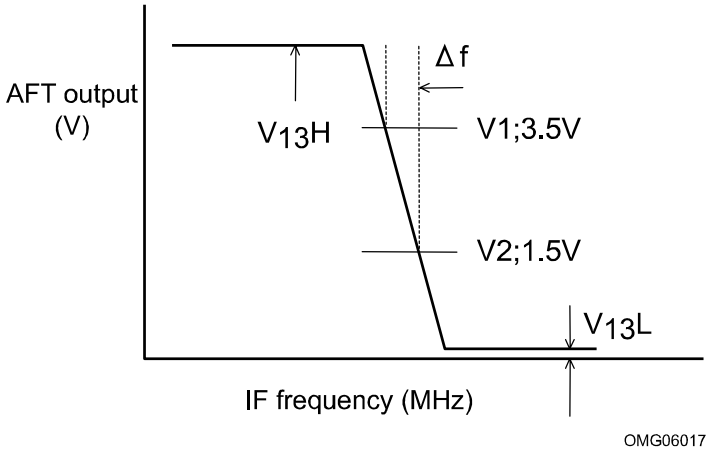
V18. No-signal AFT voltage [$V_{13}$]

(1) Internal AGC
(2) Measure the DC voltage at the AFT output (B).

V19.V20.V21. Maximum, minimum AFT output voltage, AFT detection sensitivity [$V_{13}H$, $V_{13}L$, Sf]

(1) Internal AGC
(2) fp = 45.75MHz ±1.5MHz  Sweep = 10mVrms (VIF input)
(3) Maximum voltage : $V_{13}H$, minimum voltage : $V_{13}L$.
(4) Measure the frequency deviation at which the voltage at test point B changes from V1 to V2. ····· Δf

$$Sf = \frac{2000(mV)}{\Delta f(kHz)}\ mV/kHz$$




V22.V23. VIF input resistance, Input capacitance [$R_i$, $C_i$]

(1) Referring to the Input Impedance Test Circuit, measure $R_i$ and $C_i$ with an impedance analyzer.

V24.V25. APC pull-in range [fpu, fpl]

(1) Internal AGC
(2) fp = 39MHz to 51MHz  continuous wave; 10mVrms
(3) Adjust the SG signal frequency to be higher than fp = 45.75MHz to bring the PLL to unlocked state.
Note : The PLL is assumed to be in unlocked state when a beat signal appears at test point A.
(4) When the SG signal frequency is lowered, the PLL is brought to locked state again. ····· f1
(5) Lower the SG signal frequency to bring the PLL to unlock state.
(6) When the SG signal frequency is raised, the PLL is brought to locked state again. ····· f2
(7) Calculate as follows :
fpu = f1–45.75MHz
fpl = f2–45.75MHz

V26. AFT tolerance frequency 1 [dfa1]

(1) Internal AGC
(2) SG1 : 43.75MHz to 47.75MHz variable  continuous wave 10mVrmns
(3) Adjust the SG1 signal frequency so that the AFT output DC voltage (test point B) becomes 2.5V; that SG1 signal frequency is f1.
(4) External AGC (Adjust the $V_{17}$.)
(5) Apply 5V to the IF AGC (pin 17) and then pick up the VCO oscillation frequency from GND, etc.; and measure the frequency ····· f2
(6) Calculate as follows :
AFT tolerance frequency : dfa1 = f2–f1 (kHz)

V27.V28. VCO maximum variable range (U, L) [dfu, dfl]

(1) Apply the $V_{CC}$ voltage to the external AGC, IF AGC (pin 17).
(2) Pick up the VCO oscillation frequency from the VIDEO output (A), GND, etc. and adjust the VCO coil so that the frequency becomes 45.75MHz.
(3) fl is taken as the frequency when 1V is applied to the APC pin (pin 9).
In the same manner, fu is taken as the frequency when 5V is applied to the APC pin (pin 9).
dfu = fL–45.75MHz
dfl = fL–45.75MHz

V29. VCO control sensitivity [β]

(1) Apply the $V_{CC}$ voltage to the external AGC, IF AGC (pin 17).
(2) Pick up the VCO oscillation frequency from the VIDEO output (A), GND, etc. and adjust the VCO coil so that the frequency becomes 45.75MHz.
(4) f1 is taken as the frequency when 3.0V is applied to the APC pin (pin 9).
In the same manner, f2 is taken as the frequency when 3.4V is applied to the APC pin (pin 9).

$$\beta = \frac{f2-f1}{400} \text{ (kHz/mV)}$$

V30. Synchronization ratio [$V_S$]

(1) Internal AGC
(2) fp = 45.75MHz 87.5% 10STEP B/W
$V_i$ = 10mVrms
(3) Measure the output amplitude at the measuring point A. ····· Vvideo
(4) Measure the pedestal voltage (DC) at the measuring point A. ····· Vped
$V_S$ = (Vped–V6tip) / Vvideo×100 (%)

F1. 1st SIF conversion gain [$V_G$]

(1) Internal AGC
(2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; 500μV (1st SIF input) ····· V1
(3) Detection output level at test point C (Vrms) ····· V2 (4.5MHz)

(4) $V_G = 20\log \frac{V2}{V1}$ dB

F2. 4.5MHz output level [$S_O$]

(1) Internal AGC
(2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; 10mV (1st SIF input) ····· V1
(3) Detection output level at test point C (4.5MHz) ····· $S_O$ (mVrms)

F3. 1st SIF maximum input [$S_i$ max]

(1) Internal AGC
(2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; variable (1st SIF input)
(3) Input level at which the detection output at test point C (4.5MHz) becomes $S_O$ ±2dB. ····· $S_i$ max

F4.F5. 1st SIF input resistance, Input capacitance [$R_i$ (SIF1), $C_i$ (SIF1)]

(1) Using an input analyzer, measure $R_i$ and $C_i$ in the input impedance measuring circuit.

S1. SIF limiting sensitivity [$V_i$ (lim)]

(1) Apply the $V_{CC}$ voltage to the external AGC, IF AGC (pin 17).
(2) fs = 4.5MHz fm = 400Hz ΔF = ±25kHz (SIF input)
(3) Set the SIF input level to 100mVrms and then measure the level at test point D. ····· V1
(4) Lower the SIF input level until V1 -3dB occurs. Measure the input level at that moment.

S2.S4. FM detection output voltage, distortion factor [$V_O$ (FM), THD]

(1) Apply the $V_{CC}$ voltage to the external AGC, IF AGC (pin 17).
(2) fs = 4.5MHz fm = 400Hz ΔF = ±25kHz (SIF input $V_i$ = 100mVrms)
(3) Assign the level at test point D to the FM detection output voltage and measure the distortion factor.

S3. AM rejection ratio [AMR]

(1) Apply the $V_{CC}$ voltage to the external AGC, IF AGC (pin 17).
(2) fs = 4.5MHz fm = 400Hz AM = 30% (SIF input $V_i$ = 100mVrms)
(3) Measure the output level at test point D. ····· VAM

(4) $AMR = 20\log \frac{V_O\text{ (FM)}}{VAM}$ dB

S5. SIF S/N [S/N (FM)]

(1) External AGC ($V_{17} = V_{CC}$)

(2) fs = 4.5MHz NO MOD Vi = 100mVrms

(3) Measure the output level at test point D. ····· Vn

(4) S/N (FM) = $20\log \frac{V_O\ (FM)}{Vn}$ dB

C2. SIF converter maximum output level [V max]

(1) Internal AGC

(2) fp = 45.75MHz CW; 10mV (VIF input)

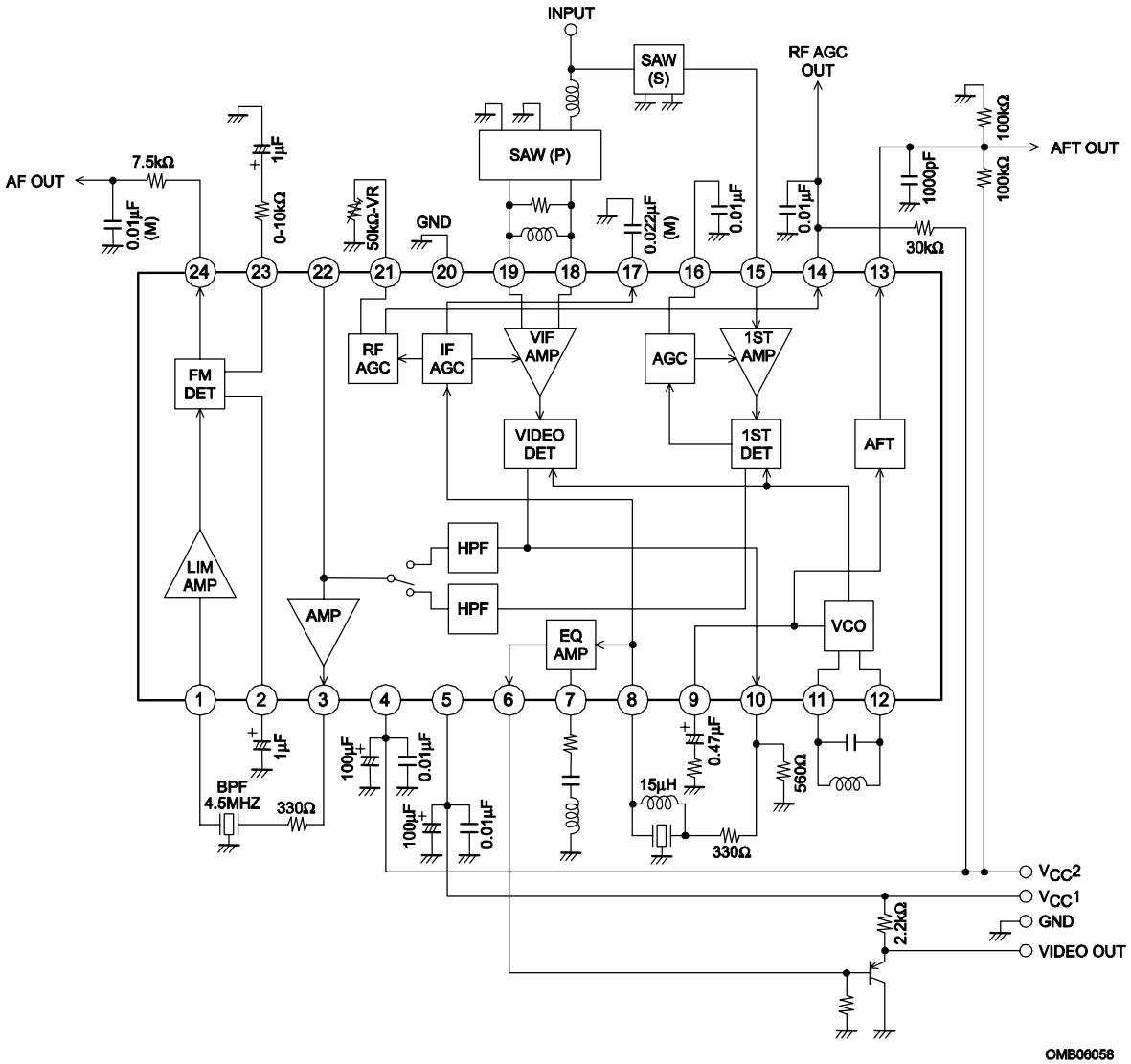
fs = 41.25MHz CW; 10mV (1st SIF input)

(3) Measure the 4.5MHz component at test point E (MIX output). ····· V max (dBμV)

Note 1) Unless otherwise specified for VIF test, apply the $V_{CC}$ voltage to the IF AGC and adjust the VCO coil so that oscillation occurs at 45.75MHz.

2) Unless otherwise specified, the SW1 must be ON.

## Sample Application Circuit




* When using a 5V common power supply for $V_{CC}1$ and $V_{CC}2$, connect an L (= 10μH) across pins 4 to 5, and disconnect C (100μF and 0.01μF) from pin 4.