5-Port Gigabit Ethernet Switch with Embedded Memory

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Features

- 5-Port Gigabit Ethernet switch integrating MACs, packet buffer memory and switching engine with GMII/MII interface
- Full Duplex 1000 Mbit/s.
- Full and Half Duplex 10/100 Mbit/s
- Supports auto-sensing or manual selection for speed and duplex capability with an embedded MPU
- Store-and-forward operation support
- Performs full wire-speed switching with no HOL blocking
- Broadcast storm control
- Quality-of-Service provisioning on 802.1P tag and port-pairs with two priority queues
- Embedded 128K Byte SRAM for packet buffer
- Integrated two-way Address-Lookup engine and table for 4K MAC addresses
- Programmable aging mechanism for the two-way 4K MAC addresses table
- Full-duplex IEEE 802.3x flow control
- Half-duplex back pressure flow control
- Port trunking for high-bandwidth links
- Provides 5 GPIO ports
- Provides EEPROM interface for auto-configuration
- System clock input is one 27MHz Crystal and one 125MHz Oscillator
- 2.5 and 3.3V operations
- 3.3 I/Os and packaged in 256-pin PQFP

Product Description

The AX88655 is a 5-Port 10/100/1000 Mbps Ethernet switch with GMII or MII Interface. The switch controller provides network system manufacturers the ideal platform for building smart and cost-effective backbone switches for small to medium sized businesses.

The AX88655 5-Port 10/100/100 BASE-T single chip switch controllers combine the benefits of network simplicity, flexibility and high integration. Its highly integrated feature set enables network system manufacturers to build smart switches for the fast-growing small to medium business market segment.

Benefits of AX88655 Switches are below.

- Simplicity
  Provides a smart, simple and low maintenance plug-and-play network interconnect system for small to medium size businesses
- Flexibility
  Highly scalable configuration allows system manufacturers to enable or disable a range of features to best meet their target price point
- Integration
  Highly integrated design drives down overall switch manufacturing costs.

Target Applications

- ✓ 5-Port Gigabit Layer 2 Switches for workgroup
- ✓ High-port count Layer 2 switches with trunking
- ✓ High performance solution of Ethernet backbone

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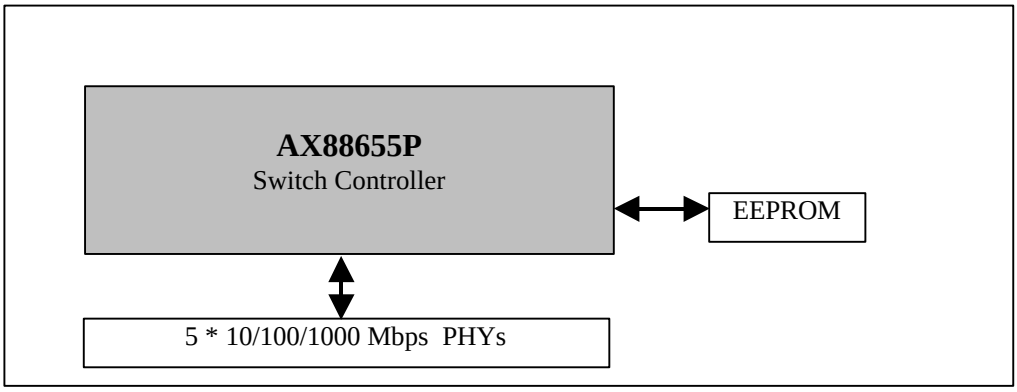
ASIX ELECTRONICS CORPORATION **First Released Date: 01/31/2002**
4F, NO.8, Hsin Ann Rd., Science-based Industrial Park, Hsin-Chu City, Taiwan, R.O.C.
TEL: 886-3-579-9500 **FAX: 886-3-563-9799** **http://www.asix.com.tw**

System Block Diagram



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1.0 AX88655 Overview

1.1 General Description

The AX88655 Gigabit switch controller supports five 10/100/1000 Mbps ports in wire-speed operation. The AX88655 Gigabit switch controller provides five 10/100/1000 Ethernet ports with GMII/MII interface. For each ports, the AX88655 supports GMII (802.3ab) interface with full-duplex operation at Gigabit speed, full- or half-duplex operation at 10/100 Mbps speed and polls the status of PHYs with an embedded MPU.

Embedded 128K bytes SRAM as a packet buffer operates with an internal 90MHz clock. For efficient utilization of the packet buffer, there are 1024 128-byte page-links totally in the buffer.

The device supports 4K internal MAC addresses which are shared by all ports with an embedded 32K byte SSRAM. The learning/routing engine is implemented with a two-way hash/linear algorithm to reduce possibility of routing collision.

Basically the AX88655 supports non-blocking wire speed forwarding rate and no Head-of-Line (HOL) blocking issue. The AX88655 provides two flow-control mechanisms to avoid loss of data: an optional jamming based backpressure flow control in the half-duplex operation and IEEE 802.3x in the full-duplex mode.

To support Quality of Service (QoS), each output port has two priority queues and their assignment can be based on the 802.1p priority field or Port-Pair setting. Each output port retrieves the frames from the shared buffer based on queuing and sends them to the transmitting (Tx) FIFO.

1.2 AX88655 Block Diagram

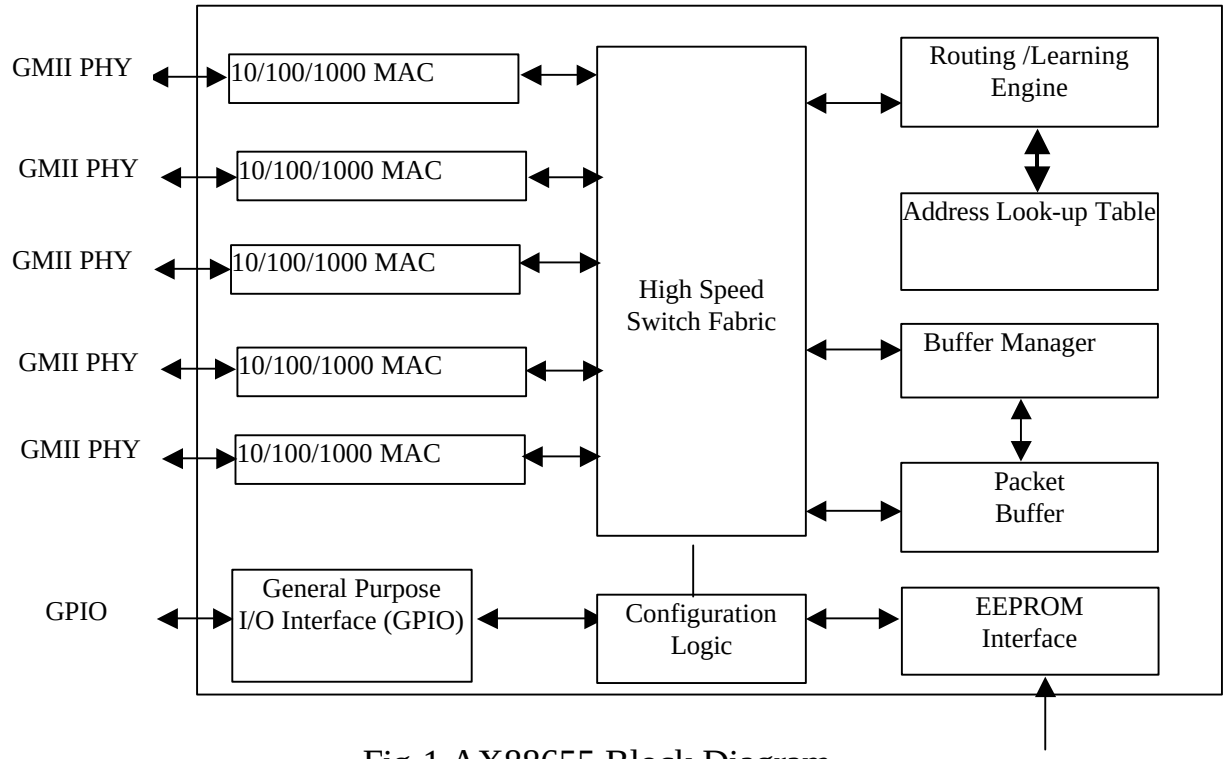


Fig-1 AX88655 Block Diagram

1.3 Pin Connection Diagram

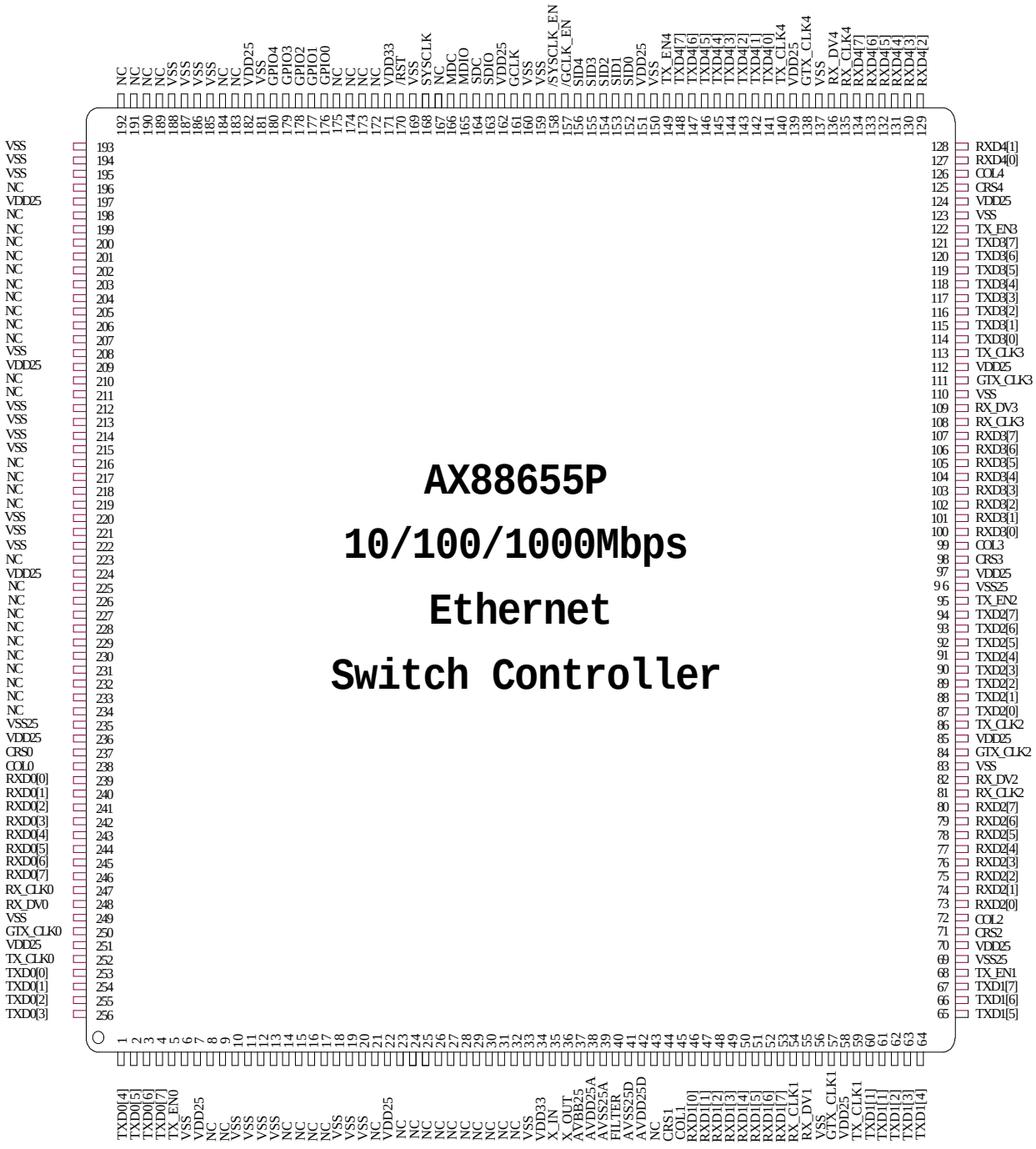


Fig-2 AX88655 Pin Diagram

2.0 Pin Descriptions

2.0 I/O Definition

The following terms describe the AX88655 pin-out:
All pin names with the "/" suffix are asserted low.
The following abbreviations are used in following Tables.

I	**Input**	**PU**	**Pull Up**
O	**Output**	**PD**	**Pull Down**
I/O	**Input/Output**	**P**	**Power Pin**
OD	**Open Drain**		

2.1 GMII/MII Interface

2.1.1 GMII Interface Port 0

Signal Name	I/O	Pin No.	Description
GTX_CLK0	O	250	**125MHz Clock Output:** it is a continuous 125 MHz clock output to giga-PHY operating at 1000BASE-T. That is, it is a timing reference for TX_EN0 and TXD0[7:0]
TX_EN0	O	5	**Transmit Enable:** When TX_EN0 is asserted, data on TXD0[7:0] are transmitted onto PHY. TX_EN0 is synchronous to GTX_CLK0 in 1000BASE-T mode and synchronous to TX_CLK0 in 10/100BASE-T mode.
TXD0[7:0]	O	4 – 1, 256 – 253	**Transmit Data:** Synchronous to the rising of GTX_CLK0 in 1000BASE-T mode. And synchronous to rising edge of TX_CLK0 in 10/100BASE-T mode.
TX_CLK0	I/PD	252	**MII Transmit Clock Input:** TX_EN0 and TXD0[3:0] are synchronous to the rising edge of this clock in 10/100BASE-T mode.
COL0	I/PD	238	**Collision Detect:** Active high to indicate that there is collision occurred in half duplex mode. In full duplex mode COL0 is always low.
CRS0	I/PD	237	**Carrier Sense:** Active high if there is carrier on medium. In half duplex mode CRS0 is also asserted during transmission and asynchronous to any clock.
RX_DV0	I	248	**Receive Data Valid:** Active high to indicate that data presented on RXD0[7:0] is valid and synchronous to RX_CLK0.
RX_CLK0	I	247	**Receive Clock Input:** 125, 25 and 2.5 MHz is running at 1000/100/10 BASE-T mode respectively. RX_DV0 and RXD0[7:0] are synchronous to rising edge of this clock.
RXD0[7:0]	I/PD	246 - 239	**Receive Data:** Data received by the PHY are presented on RXD0 and synchronous to RX_CLK0. RXD0[3:0] is valid in 10/100/1000BASE-T and RXD[7:4] is valid only in 1000BASE-T modes.

2.1.2 GMII Interface Port 1

Signal Name	I/O	Pin No.	Description
GTX_CLK1	O	57	**125MHz Clock Output:** Please references section 2.1.1.
TX_EN1	O	68	**Transmit Enable:** Please references section 2.1.1.
TXD1[7:0]	O	67 – 60	**Transmit Data:** Please references section 2.1.1.
TX_CLK1	I/PD	59	**MII Transmit Clock Input:** Please references section 2.1.1.
COL1	I/PD	45	**Collision Detect:** Please references section 2.1.1.
CRS1	I/PD	44	**Carrier Sense:** Please references section 2.1.1.
RX_DV1	I	55	**Receive Data Valid:** Please references section 2.1.1.
RX_CLK1	I	54	**Receive Clock Input:** Please references section 2.1.1.
RXD1[7:0]	I/PD	53 - 46	**Receive Data:** Please references section 2.1.1.

2.1.3 GMII Interface Port 2

Signal Name	I/O	Pin No.	Description
GTX_CLK2	O	84	**125MHz Clock Output:** Please references section 2.1.1.
TX_EN2	O	95	**Transmit Enable:** Please references section 2.1.1.
TXD2[7:0]	O	94 – 87	**Transmit Data:** Please references section 2.1.1.
TX_CLK2	I/PD	86	**MII Transmit Clock Input:** Please references section 2.1.1.
COL2	I/PD	72	**Collision Detect:** Please references section 2.1.1.
CRS2	I/PD	71	**Carrier Sense:** Please references section 2.1.1.
RX_DV2	I	82	**Receive Data Valid:** Please references section 2.1.1.
RX_CLK2	I	81	**Receive Clock Input:** Please references section 2.1.1.
RXD2[7:0]	I/PD	80 - 73	**Receive Data:** Please references section 2.1.1.

2.1.4 GMII Interface Port 3

Signal Name	I/O	Pin No.	Description
GTX_CLK3	O	111	**125MHz Clock Output:** Please references section 2.1.1.
TX_EN3	O	122	**Transmit Enable:** Please references section 2.1.1.
TXD3[7:0]	O	121 – 114	**Transmit Data:** Please references section 2.1.1.
TX_CLK3	I/PD	113	**MII Transmit Clock Input:** Please references section 2.1.1.
COL3	I/PD	99	**Collision Detect:** Please references section 2.1.1.
CRS3	I/PD	98	**Carrier Sense:** Please references section 2.1.1.
RX_DV3	I	109	**Receive Data Valid:** Please references section 2.1.1.
RX_CLK3	I	108	**Receive Clock Input:** Please references section 2.1.1.
RXD3[7:0]	I/PD	107 - 100	**Receive Data:** Please references section 2.1.1.

2.1.5 GMII Interface Port 4

Signal Name	I/O	Pin No.	Description
GTX_CLK4	O	138	**125MHz Clock Output:** Please references section 2.1.1.
TX_EN4	O	149	**Transmit Enable:** Please references section 2.1.1.
TXD4[7:0]	O	148 – 141	**Transmit Data:** Please references section 2.1.1.
TX_CLK4	I/PD	140	**MII Transmit Clock Input:** Please references section 2.1.1.
COL4	I/PD	126	**Collision Detect:** Please references section 2.1.1.
CRS4	I/PD	125	**Carrier Sense:** Please references section 2.1.1.
RX_DV4	I	136	**Receive Data Valid:** Please references section 2.1.1.
RX_CLK4	I	135	**Receive Clock Input:** Please references section 2.1.1.
RXD4[7:0]	I/PD	134 - 127	**Receive Data:** Please references section 2.1.1.

2.2 Miscellaneous

Signal Name	I/O	Pin No.	Description
X_IN	I	35	**Crystal or OSC 27MHz Input:** This is a clock source of PLL. The PLL will generate a 90MHz internal clock.
X_OUT	O	36	**Crystal 27MHz Output:** This pin should be floating with single-ended external clock.
GCLK	I	161	**OSC 125MHz Input:** 125MHz Clock for GMII
SYSCLK	I	168	**System Clock Input:** 85 ~ 90MHz Clock for switch kernel
/GCLK _EN	I/PU	157	**GCLK Enable:** 0) use GCLK; 1) Reserved
/SYSCLK_EN	I/PU	158	**System Clock Enable:** 0) use SYSCLK; 1) 90MHz generated by internal PLL circuit from X_IN clock source.
FILTER	I	40	**FILTER**: For internal PLL circuit use.
/RST	I	170	**Reset:** Active Low
MDIO	I/O/PU	165	**Station Management Data In/Out:** PHY Management Data Input and Output.
MDC	O	166	**Station Management Data Clock Out:** PHY Management Clock.
SDIO	I/O/PU	163	**EEPROM Data In/Out:** EEPROM Serial Data Input and Output.
SDC	I/O/PU	164	**EEPROM Data Clock In/Out:** EEPROM Serial Clock. (Note: It is output pin if the embedded MPU is active; otherwise as input pin)
SID[4:0]	I/PD I/PD I/PD I/UP I/UP	156, 155, 154, 153, 152	**Switch ID:** MPU can identify the switch and PHYs with this ID. Default is “00011b”.
GPIO[4:0]	I/O/PU	180 - 176	**General Purpose I/O:** The 5 GPIOs can be programmed for special application. (Note: The function is not released to user normally. Please contact with ASIX directly if any requirement)

NC	N/A	8, 9, 41, 15, 16, 17, 21, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 43, 167, 172, 173, 174, 175, 183, 184, 189, 190, 191, 192, 196, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207, 210, 211, 216, 217, 218, 219, 223, 225, 226, 227, 228, 229, 230, 231, 232, 233, 234	**NC:** No Connect.
VDD33	I	34, 171,	**3.3V +/-5% Supply Voltage.**
VDD25	P	7, 22, 58, 70, 85, 97, 112, 124, 139, 151, 162, 182, 197, 209, 224, 236, 251	**2.5V +/-5% Supply Voltage.**
VSS	P	6, 10, 11, 12, 13, 18, 19, 20, 33, 56, 69, 83,96, 110, 123, 137, 150, 157, 159, 160, 167, 169, 181, 185, 186, 187, 188, 193, 194, 195, 208, 212, 213, 214, 215, 220, 221, 222, 235, 249	**Ground**
AVBB25	P	37	**Ground for PLL**
AVDD25A	P	38	**2.5V +/-5% Supply Voltage for PLL.**
AVSS25A	P	39	**Ground for PLL**
AVDD25D	P	42	**2.5V +/-5% Supply Voltage for PLL.**
AVSS25D	P	41	**Ground for PLL**

3.0 Functional Description

3.1 Introduction

In general, the AX88655 device is a highly integrated Layer 2 switch. It supports five 10/100/1000 ports with on-chip MACs. It also supports integrated switching logic, packet queuing memory and packet storage memory. The AX88655 is capable of routing-and-forwarding packets at wire speed on all ports regardless of packet size.
It is a low cost solution for five ports Gigabit Ethernet backbone switch design. No CPU interface is required; After power on reset, AX88655 provide an auto load configuration setting function through a 2 wire serial EEPROM interface to access external EEPROM device, and AX88655 can easily be configured to support trunking, QoS, IEEE 802.3x flow control threshold setting, broadcast storm control ...etc functions. An overview of AX88658's major functional blocks is shown in Fig-1.

3.2 Packet Filtering and Forwarding Process

The switch use simple store-and-forward algorithm as packet switching method. After receives incoming packets, the packets will be stored to the embedded memory first. The AX88655 searches in the Address-Lookup Table with DA of the packet. The packet will be forward to its destination port, if this packet's DA hits; otherwise this packet will be broadcasted. Of course, only good packets will be forward. Conditions of good packets are below:

1. CRC is correct.
2. 64 Bytes < PacketLength < 1518/1522 Bytes
3. Not local packets, That is, it is a local packets if its SourcePort is its DestinationPort.
4. Not PAUSE or other control packets.
5. Not the same trunking group.

3.3 MAC Address Routing, Learning and Aging Process

The switch supports 4K MAC entries for switching. Two-way dynamic address learning is performed by each good unicast packet is completely received. And linear/XOR hash algorithm of the static address learning is achieved by EEPROM configuration. On the other hand, the routing process is performed whenever the packet's DA is captured. If the DA can not get a hit result, the packet is going to broadcast.

Only the learned address entries are scheduled in the aging machine. If one station does not transmit any packet for a period of time, the belonging MAC address will be kicked out from the address table. The aging out time can be program automatically through the EEPROM configuration. (Default value is 300 seconds)

3.4 Full Duplex 802.3x Flow Control

In full duplex mode, AX88655 supports the standard flow control mechanism defined in IEEE 802.3x standard. It enables the stopping of remote node transmissions via a PAUSE frame information interaction. When space of the packet buffer is less than the initialization setting threshold value, AX88655 will send out a PAUSE-ON packet with pause time equal to "xFFF" to stop the remote node transmission. And then AX88655 will send out a PAUSE-OFF packet with pause time equal to zero to inform the remote node to retransmit packet if has enough space to receive packets.

3.5 Half Duplex Back Pressure Control

In half duplex mode, AX88655 provide a backpressure control mechanism to avoid dropping packets during network conjection situation. When space of the packet buffer is less than the initialization setting threshold value, AX88655 will send a JAM pattern in the input port when it senses an incoming packet, thus force a collision to make the remote node transmission back off and will effectively avoid dropping packets. And then AX88655 will not send out a JAM packet any more if has enough space to receive one packet.

3.6 MII Polling

The AX88655 supports PHY management through the serial MDIO/MDC interface. That is, the AX88655 access related

register of PHYs via MDIO/MDC interface after power on reset. The AX88655 will periodically and continuously poll and update the link status and link partner's ability which include speed, duplex mode, and 802.3x flow control capable status of the connected PHY devices through MDIO/MDC serial interface.

3.7 Port-Based QoS: Port-Pair

AX88655 provides 4 Port-Pairs for bandwidth management. Users can assign any two ports as one Port-Pair with internal registers basically. Any packets will put the high priority queue of the Port-Pair when send the packets each other. That is, two ports of each Port-Pair will obtain more bandwidth than other ports when congestion.

In addition, one port can be as the highest priority port if one All_Bit of a Port-Pair is active. That is, user can assign format of the Port-Pair as OnePort-to-All and every packets of the OnePort will put in the high priority transmit queue of other ports.

4.0 Register Descriptions

Registers Table Summary:

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
00 H	Reserved																0000 H
01 H	Reserved																0000 H
02 H	Reserved				RxFlowCtrl[4:0]				Reserved				TxFlowCtrl[4:0]				0000 H
03 H	Reserved																0000 H
04 H	Reserved																0000 H
05 H	Reserved																0000 H
06 H	Reserved																0000 H
07 H	Reserved																1215 H
08 H	Reserved																7777 H
09 H	Reserved																7777 H
0A H	PortPair1[7:0]								PortPair0[7:0]								0000 H
0B H	PortPair3[7:0]								PortPair2[7:0]								0000 H
0C H	LowQueueWeight[3:0]				Reserved				lw_LowQueueDiscardLimit [9:0]								1060 H
0D H	HighQueueWeight[3:0]				MaxStorm				lw_HighQueueDiscardLimit [9:0]								1060 H
0E H	Res.	PTO	MPL	Reserved		SR	SP	NSB	Reserved				QoS[1:0]		AE	HM	Res.	8880 H
0F H	Reserved								MaxAge[8:0]								1865 H
10 H	Reserved				Trunk30[2:0]				Reserved								00C0 H
11 H	Reserved								LowQueueFlowCtrlMark[9:0]								0010 H
12 H	MaxJam[5:0]								HighQueueFlowCtrlMark[9:0]								2810 H
13 H	Reserved								hw_LowQueueDiscardLimit[9:0]								0070 H
14 H	Reserved								hw_HighQueueDiscardLimit[9:0]								0070 H

Notes: 1. The word “Reserved” = “Res.” on the above table.

Notes: 2. Care must be taken that the “Reserved” registers should keep the default value always. Change of any reserved value may be resulting in unpredictable conditions.

Notes: 3. The registers can be accessed by internal MPU only. The MPU will read in configuration table, located on EEPROM at somewhere address, and programs the above registers when every time power on or after system reset.

4.1 Register 00

BIT	R/W	DESCRIPTION
15:0	**R/W**	Reserved

4.2 Register 01

BIT	R/W	DESCRIPTION
15:0	**R/W**	Reserved

4.3 Register 02

BIT	R/W	DESCRIPTION
15:13	**R/W**	Reserved

12:8	**R/W**	FlowCtrlEnable for MAC's receive part of Port[4:0] are configured by internal 8051 0: not identify PAUSE frames by receive part of MAC 1: can identify PAUSE frames. That is, PauseTimer of MAC will be active.
7:5	**R/W**	Reserved
4:0	**R/W**	FlowCtrlEnable for MAC's transmit part of Port[4:0] are configured by internal 8051 0: not send PAUSE frames or JAM 1: send PAUSE frames for full-duplex when the packet buffer is empty. send JAM frames for half-duplex when the packet buffer is empty.

4.4 Register 03

BIT	R/W	DESCRIPTION
15:0	**R/W**	Reserved

4.5 Register 04

BIT	R/W	DESCRIPTION
15:0	**R/W**	Reserved

4.6 Register 05

BIT	R/W	DESCRIPTION
15:0	**R/W**	Reserved

4.7 Register 06

BIT	R/W	DESCRIPTION
15:0	**R/W**	Reserved

4.8 Register 07

BIT	R/W	DESCRIPTION
15:0	**R/W**	Reserved

4.9 Register 08

BIT	R/W	DESCRIPTION
15:0	**R/W**	Reserved

4.10 Register 09

BIT	R/W	DESCRIPTION
15:0	**R/W**	Reserved

4.11 Register 0A

BIT	R/W	DESCRIPTION
15	**R/W**	All_Bit of PortPair #1 when QoS[0] is high
14:12	**R/W**	Port_ID of PortPair #1 when QoS[0] is high

11	**R/W**	All_Bit of PortPair #1 when QoS[0] is high
10:8	**R/W**	Port_ID of PortPair #1 when QoS[0] is high
7	**R/W**	All_Bit of PortPair #0 when QoS[0] is high
6:4	**R/W**	Port_ID of PortPair #0 when QoS[0] is high
3	**R/W**	All_Bit of PortPair #0 when QoS[0] is high
2:0	**R/W**	Port_ID of PortPair #0 when QoS[0] is high

4.12 Register 0B

BIT	R/W	DESCRIPTION
15	**R/W**	All_Bit of PortPair #3 when QoS[0] is high
14:12	**R/W**	Port_ID of PortPair #3 when QoS[0] is high
11	**R/W**	All_Bit of PortPair #3 when QoS[0] is high
10:8	**R/W**	Port_ID of PortPair #3 when QoS[0] is high
7	**R/W**	All_Bit of PortPair #2 when QoS[0] is high
6:4	**R/W**	Port_ID of PortPair #2 when QoS[0] is high
3	**R/W**	All_Bit of PortPair #2 when QoS[0] is high
2:0	**R/W**	Port_ID of PortPair #2 when QoS[0] is high

4.13 Register 0C

BIT	R/W	DESCRIPTION
15:12	**R/W**	WeightForLowQue: Weight for low priority queues when QoS is active (see Appendix C)
11:10	**R/W**	Reserved
9:0	**R/W**	LowWaterMark of low priority queues when drop packets

4.14 Register 0D

BIT	R/W	DESCRIPTION
15:12	**R/W**	WeightForHighQue: Weight for high priority queues when QoS is active (see Appendix C)
11:10	**R/W**	Maximum number of broadcast frames that can be accumulated in each input frame buffer. 00: disable broadcast storm control 01: 32 frames 10: 48 frames 11: 64 frames
9:0	**R/W**	LowWaterMark of high priority queues when drop packets

4.15 Register 0E

BIT	R/W	DESCRIPTION
15	**R/W**	Reserved
14	**R/W**	802.3x Flow control frame recognition control 0: check for MAC control frame DA MAC address in addition to the MAC control type field 1: check only the MAC control type field
13	**R/W**	Setting for maximum length of packet that received 0: 1518 byte 1: 1522 byte
12:11	**R/W**	Reserved
10	**R/W**	Software Reset (Only reset the switch kernel) 0: active 1: disable

9	**R/W**	Back-off algorithm selection 0: disable. Device will perform the IEEE standard exponential back off algorithm when a collision occurs. 1: enable. When collisions occur, the MACs will back off up to 7 slots.
8	**R/W**	0: stop generate JAM patterns after some collision that is defined by MaxJam[5:0] 1: Never stop back-pressure
7:5	**R/W**	Reserved
4:3	**R/W**	QoS selection 00: disable QoS function 01: Port-Pair Priority algorithm 10: 802.1p
2	**R/W**	AgingEnable Switch Table Entry Aging Control. Only the dynamically learned addresses will be aged. All explicit entries will not age. The aging time is programmed in register 0F. 0: disable. The table aging process is disabled. 1: enable. The table aging process is enabled and a hardware process ages every dynamically learned table entry.
1	**R/W**	Hash algorithm selection 0: XOR mapping 1: Linear mapping
0	**R/W**	Reserved

4.16 Register 0F

BIT	R/W	DESCRIPTION
15:9	**R/W**	Reserved
8:0	**R/W**	MaxAge. This is a seven-bit register containing unsigned integer for determining the address-aging timer. The resolution of the normal address aging is (64 M* MaxAge[8:0]) / FreqencyOfSystemClock. Default value is 300 seconds.

4.17 Register 10

BIT	R/W	DESCRIPTION
15:13	**R/W**	Reserved
12:10	**R/W**	Trunking selection for Port[3:0] 000: disable trunking 001: disable trunking 010: one 2-Port Trunking for Port[1:0] 011: one 2-Port Trunking for Port[1:0] 100: one 2-Port Trunking for Port[3:2] 101: one 4-Port Trunking 110: two 2-Port Trunkings for Port[3:2] and Port[1:0] 111: one 4-Port Trunking
9:0	**R/W**	Reserved

4.18 Register 11

BIT	R/W	DESCRIPTION
15:10	R/W	Reserved
9:0	R/W	**Low**WaterMarkFor**FlowCtrl.** This is a ten-bit register containing unsigned integer for transmit queues whether generate PAUSE-ON or not.

4.19 Register 12

BIT	R/W	DESCRIPTION
15:10	R/W	**MaxJam.** This is a six-bit register containing unsigned integer for determining the JAM counter whether generate JAM or not.
9:0	R/W	**High**WaterMarkFor**FlowCtrl.** This is a ten-bit register containing unsigned integer for transmit queues whether generate PAUSE-OFF or not.

4.20 Register 13

BIT	R/W	DESCRIPTION
15:10	R/W	Reserved
9:0	R/W	HighWaterMark of low priority queues when drop packets

4.21 Register 14

BIT	R/W	DESCRIPTION
15:10	R/W	Reserved
9:0	R/W	HighWaterMark of high priority queues when drop packets

5.0 ELECTRICAL SPECIFICATION AND TIMING

5.1 Absolute Maximum Ratings

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+70	°C
Storage Temperature	Ts	-55	+150	°C
Supply Voltage	Vcc	-0.3	+4.0	V
Input Voltage	Vin	-0.3	Vdd+0.5	V
Output Voltage	Vout	-0.3	Vdd+0.5	V
Lead Temperature (soldering 10 seconds maximum)	Tl	-55	+220	°C

Note: Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Ratings conditions for extended period, adversely affect device life and reliability

5.2 General Operation Conditions

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+70	°C
Supply Voltage	Vdd	+3.0	+3.6	V

5.3 DC Characteristics

(Vdd=3.0V to 3.6V, Vss=0V, Ta=0°C to 70°C)

Description	SYM	Min	Max	Units
Low Input Voltage	Vil	Vss-0.3	0.8	V
High Input Voltage	Vih	2	Vdd+0.5	V
Low Output Voltage	Vol		0.4	V
High Output Voltage	Voh	2.4		V
Input Leakage Current 1 (Note 1)	Iil1		10	uA
Input Leakage Current 2 (Note 2)	Iil1		500	uA
Output Leakage Current	Iol		10	uA

Description	SYM	Min	Tpy	Max	Units
Power Consumption	Pc		TBD		mA

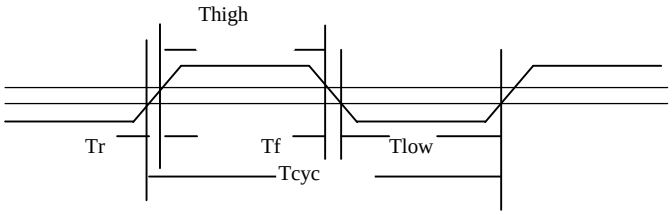
Note:

1. All the input pins without pull low or pull high.
2. Those pins had been pull low or pull high.

5.4 AC specifications

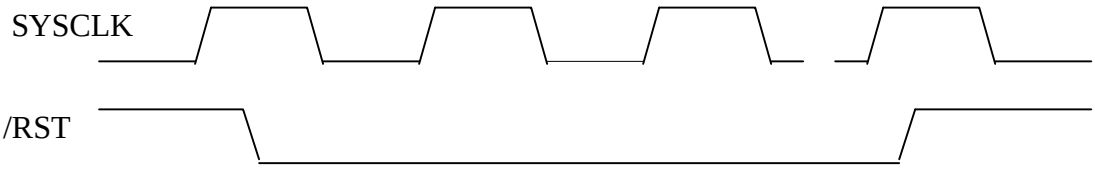
5.4.1 X_IN Signal Timing

X_IN



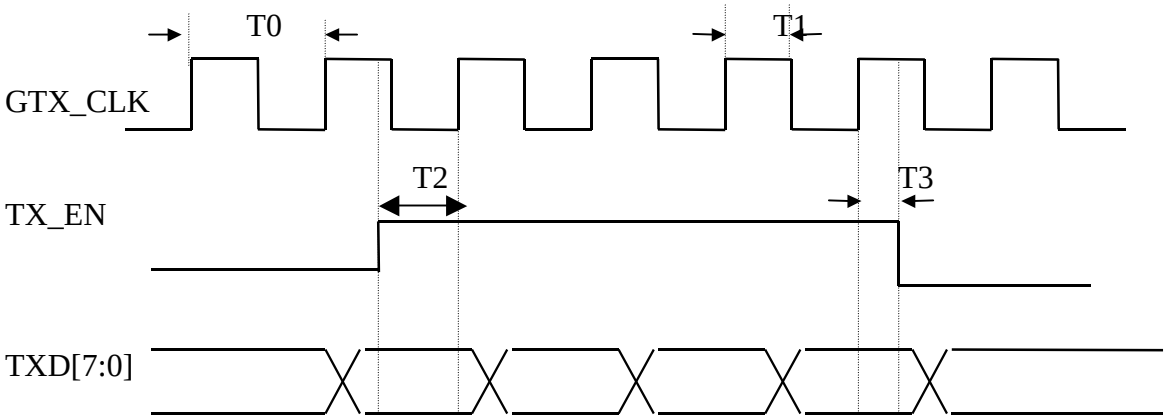
Symbol	Description	Min	Typ.	Max	Units
Tcyc	CYCLE TIME		20		ns
Thigh	CLK HIGH TIME	8	10	12	ns
Tlow	CLK LOW TIME	8	10	12	ns
Tr/Tf	CLK SLEW RATE	1	-	4	ns

5.4.2 Reset Signal Timing

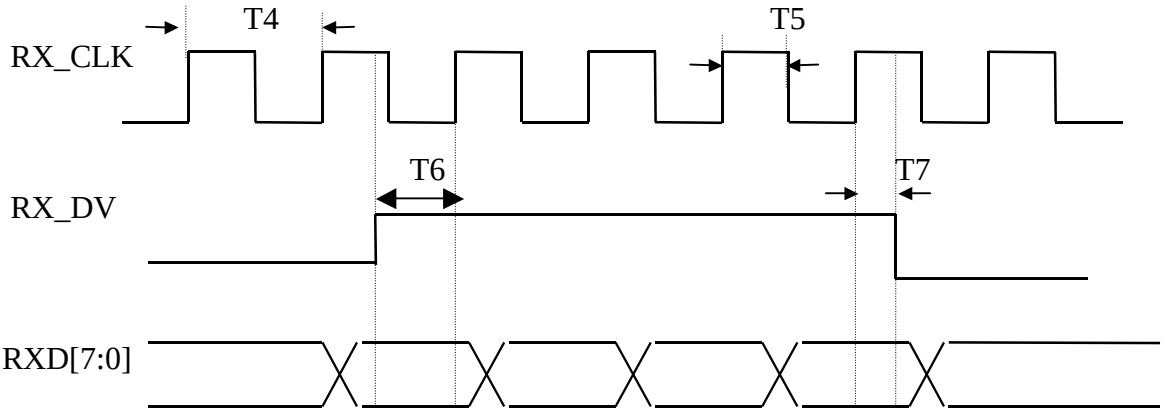


Symbol	Description	Min	Typ.	Max	Units
Trst	Reset pulse width	10	-	-	SYSCLK

5.4.3 GMII Transmit/Receive Signals Timing

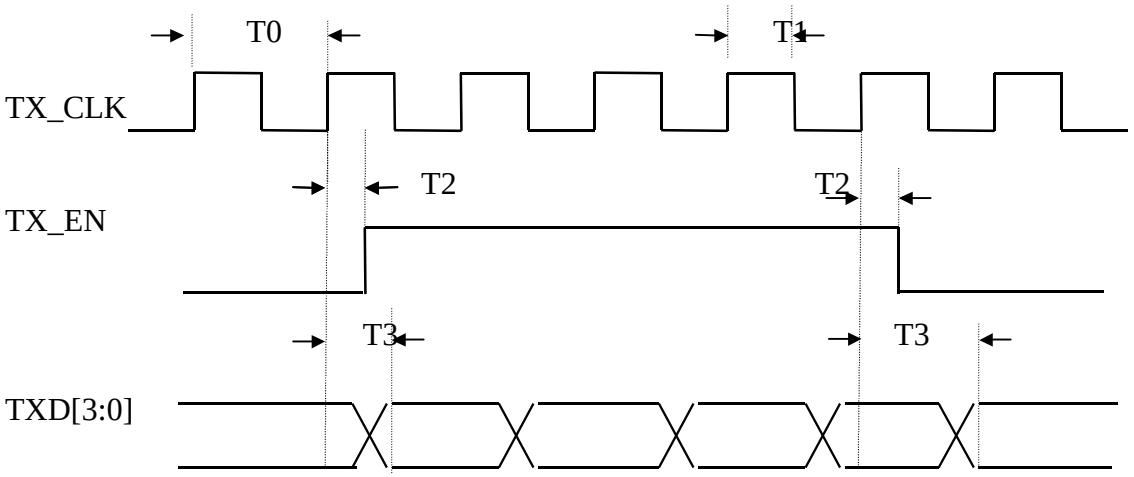


Symbol	Description	Min	Typ.	Max	Units
T0	GTX_CLK Clock Cycle Time	7.998	8	8.002	ns
T1	GTX_CLK Clock High Time		4		ns
T2	TX_EN and TXD data setup to GTX_CLK rising edge	2.5			ns
T3	TX_EN and TXD data hold from GTX_CLK rising edge	0.5			ns

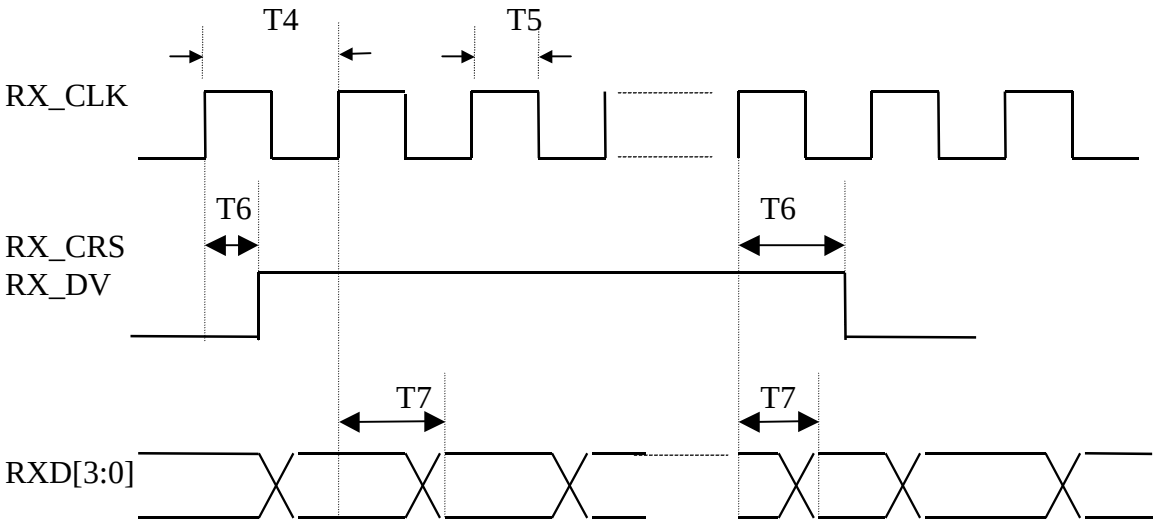


Symbol	Description	Min	Typ.	Max	Units
T4	RX_CLK Clock Cycle Time	7.998	8	8.002	ns
T5	RX_CLK Clock High Time		4		ns
T6	RX_DV and RXD data setup to RX_CLK rising edge	2.5			ns
T7	RX_DV and RXD data hold from RX_CLK rising edge	0.5			ns

5.4.4 100 Mbps MII Transmit/Receive Signals Timing

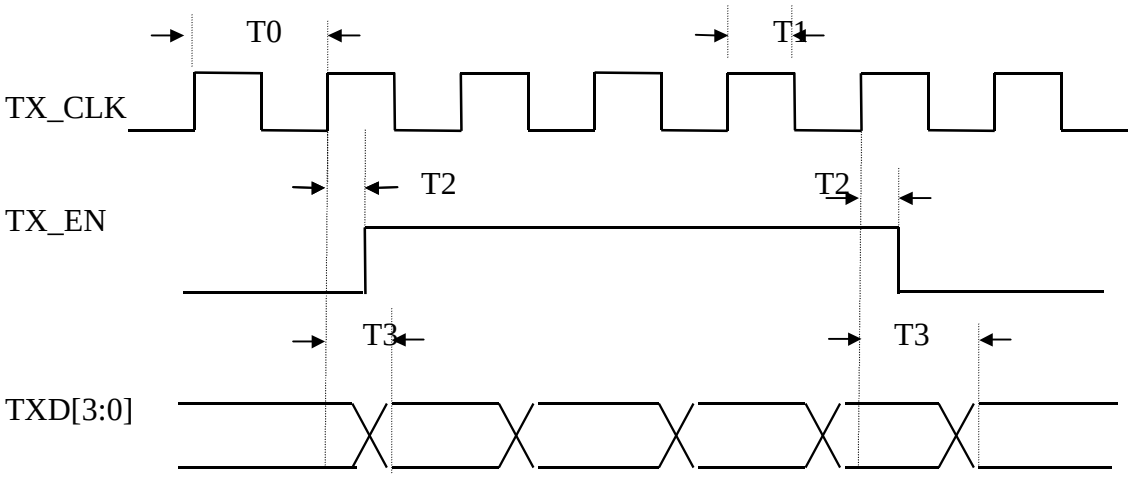


Symbol	Description	Min	Typ.	Max	Units
T0	TX_CLK Cycle Time	39.996	40	40.004	ns
T1	TX_CLK High Time	14	20	26	ns
T2	TX_CLK rising edge to TX_EN Delay	7.440		21.760	ns
T3	TX_CLK rising edge to TXD Delay	3.410		13.320	ns

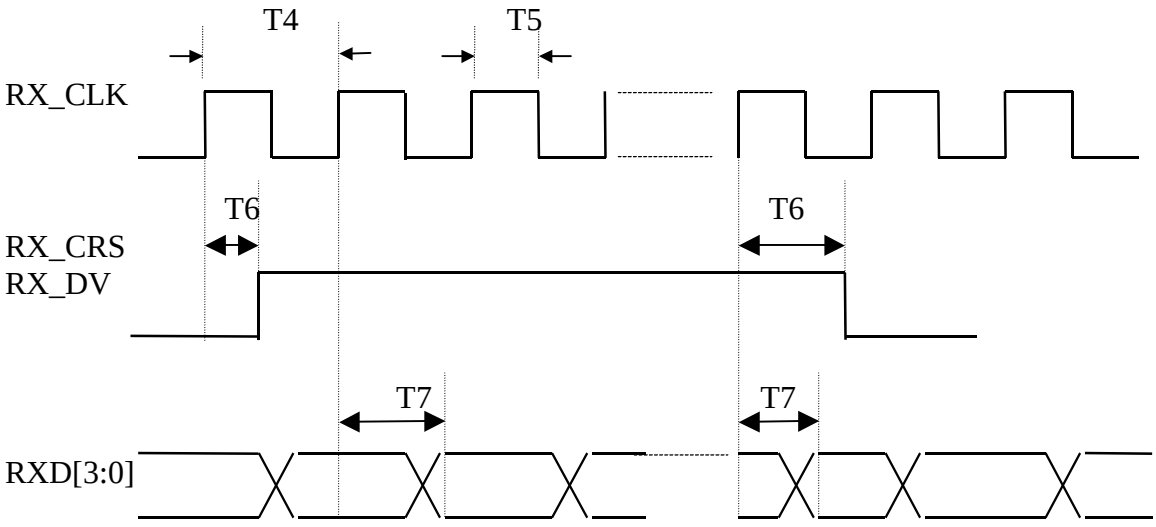


Symbol	Description	Min	Typ.	Max	Units
T4	RX_CLK Clock Cycle Time	39.996	40	40.004	ns
T5	RX_CLK Clock High Time	14	20	26	ns
T6	RX_CLK rising edge to RX_DV and RX_CRS Delay	3.0		13.0	ns
T7	RX_CLK rising edge to RXD Delay	3.0		13.0	ns

5.4.5 10 Mbps MII Transmit/Receive Signals Timing

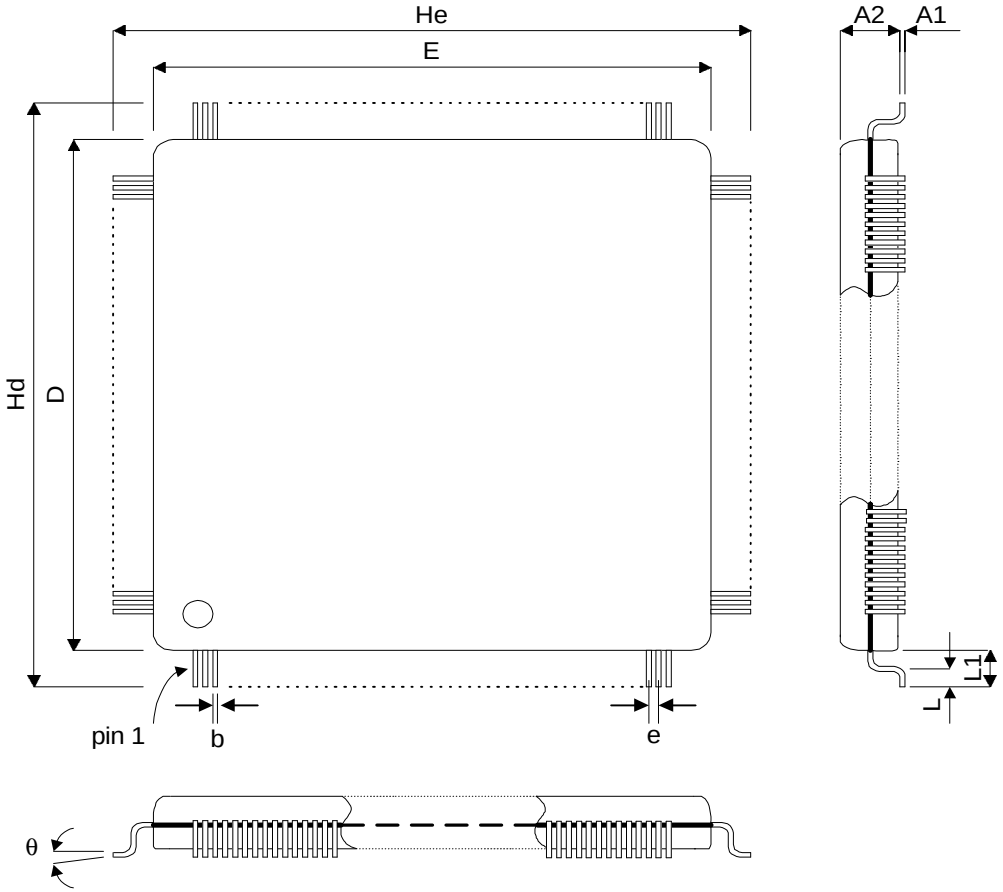


Symbol	Description	Min	Typ.	Max	Units
T0	TX_CLK Cycle Time	399.96	400	400.04	ns
T1	TX_CLK High Time	14	20	26	ns
T2	TX_CLK rising edge to TX_EN Delay	7.440		21.760	ns
T3	TX_CLK rising edge to TXD Delay	3.410		13.320	ns



Symbol	Description	Min	Typ.	Max	Units
T4	RX_CLK Clock Cycle Time	399. 96	400	400. 04	ns
T5	RX_CLK Clock High Time	140	200	260	ns
T6	RX_CLK rising edge to RX_DV and RX_CRS Delay	3.0		13.0	ns
T7	RX_CLK rising edge to RXD Delay	3.0		13.0	ns

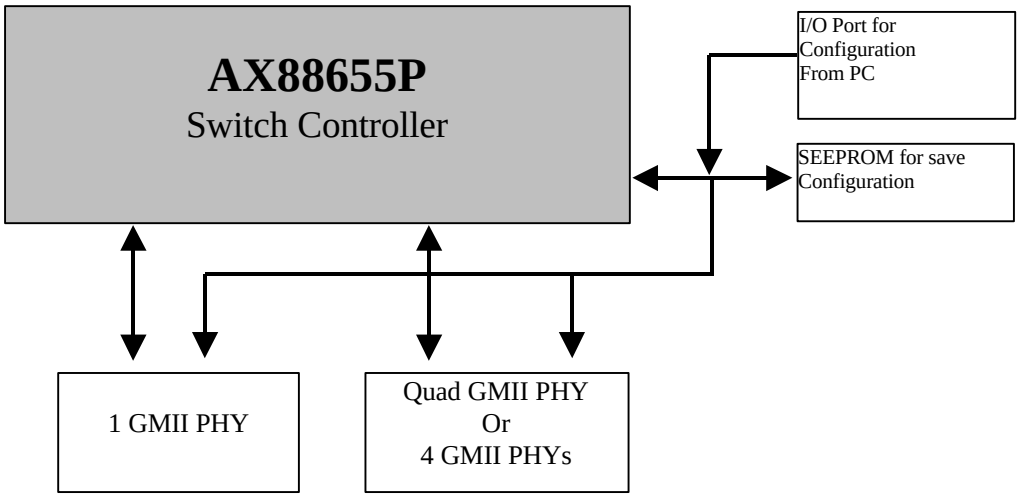
6.0 PACKAGE INFORMATION



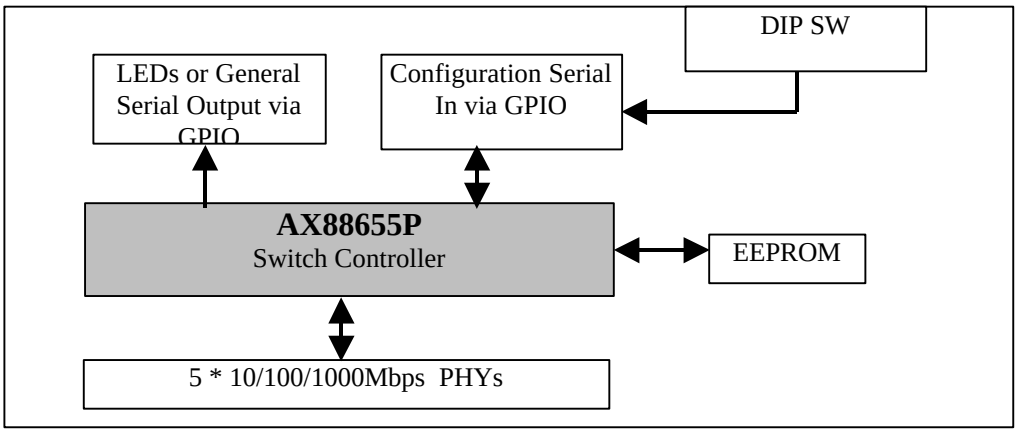
SYMBOL	MILIMETER		
	MIN.	NOM	MAX
A1	**0.25**		
A2		**3.4**	
b		**0.16**	
D		**28.00**	
E		**28.00**	
e		**0.4**	
Hd		**30.6**	
He		**30.6**	
L	**0.45**		**0.75**
L1		**1.3**	
θ	**0**		**7**

Appendix A: System Applications

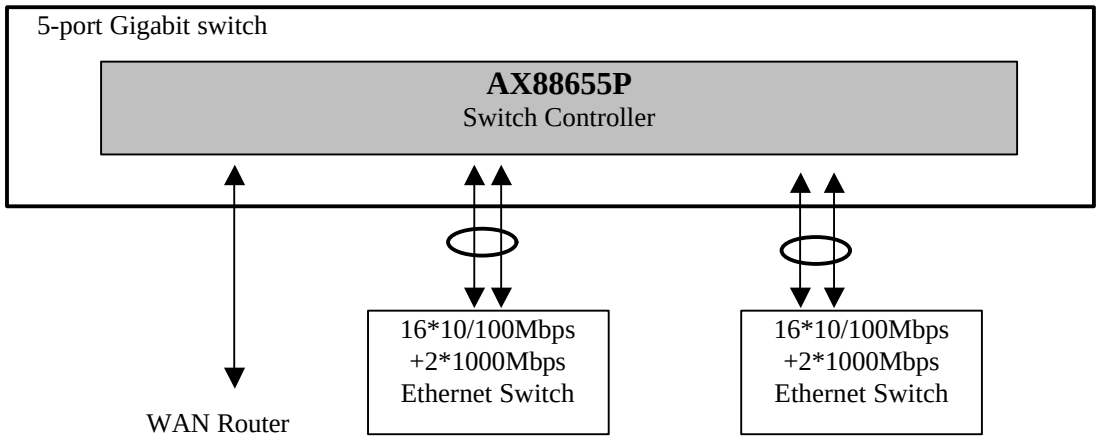
A.1 AX88655 as 5-Port SOHO high traffic power user switch



A.2 AX88655 as 5-Port Smart switch (DIP switch configurable)

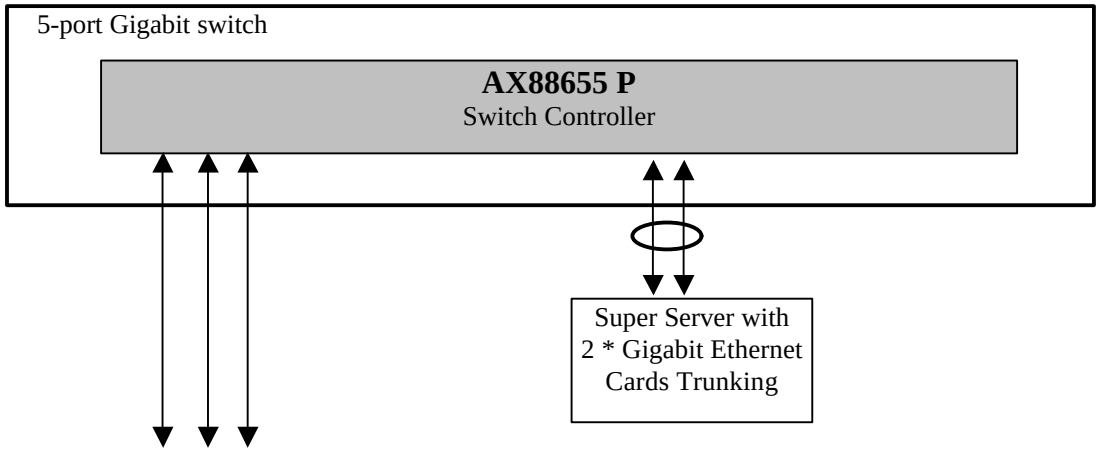


A.3 AX88655 for 10/100Mbps Ethernet Backbone



Using 2 Gigabit Ports Up-link and Trunking form a 12.8G Non-blocking backbone

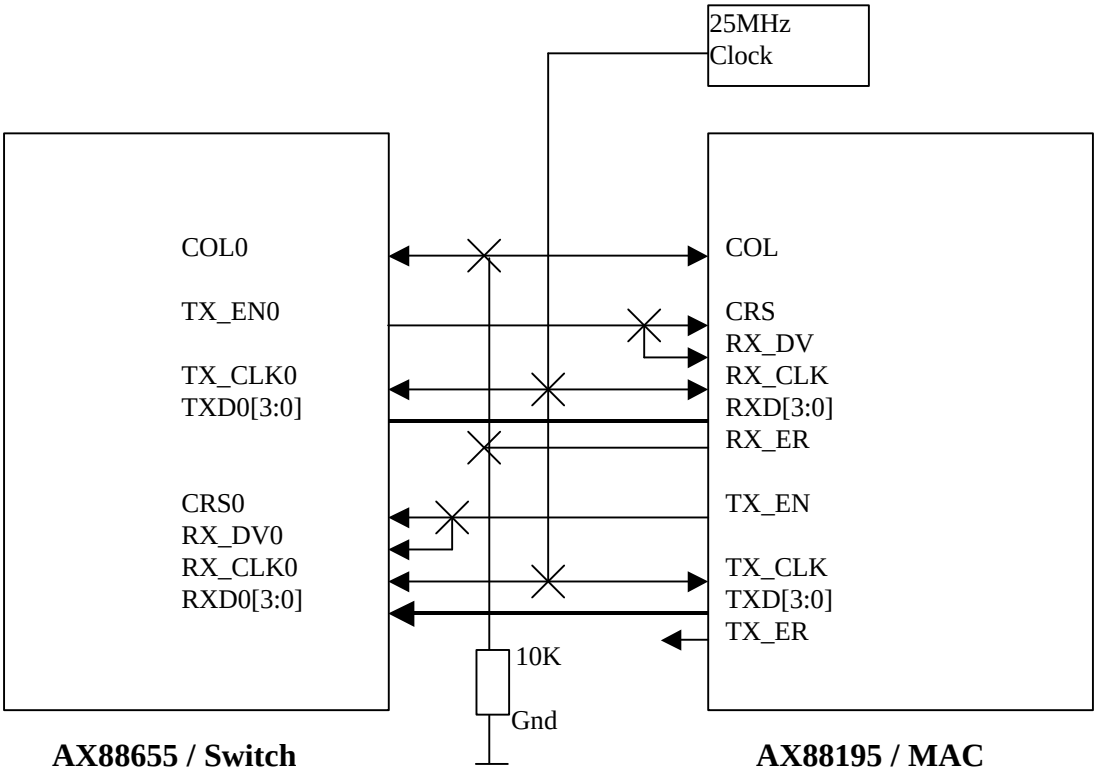
A.4 AX88655 for Super Server Trunking Application



Appendix B: Design Note

B.1 Using MII I/F connects to MAC

Using MII interface to connect to MAC type device application for AX88655 is illustrated bellow.



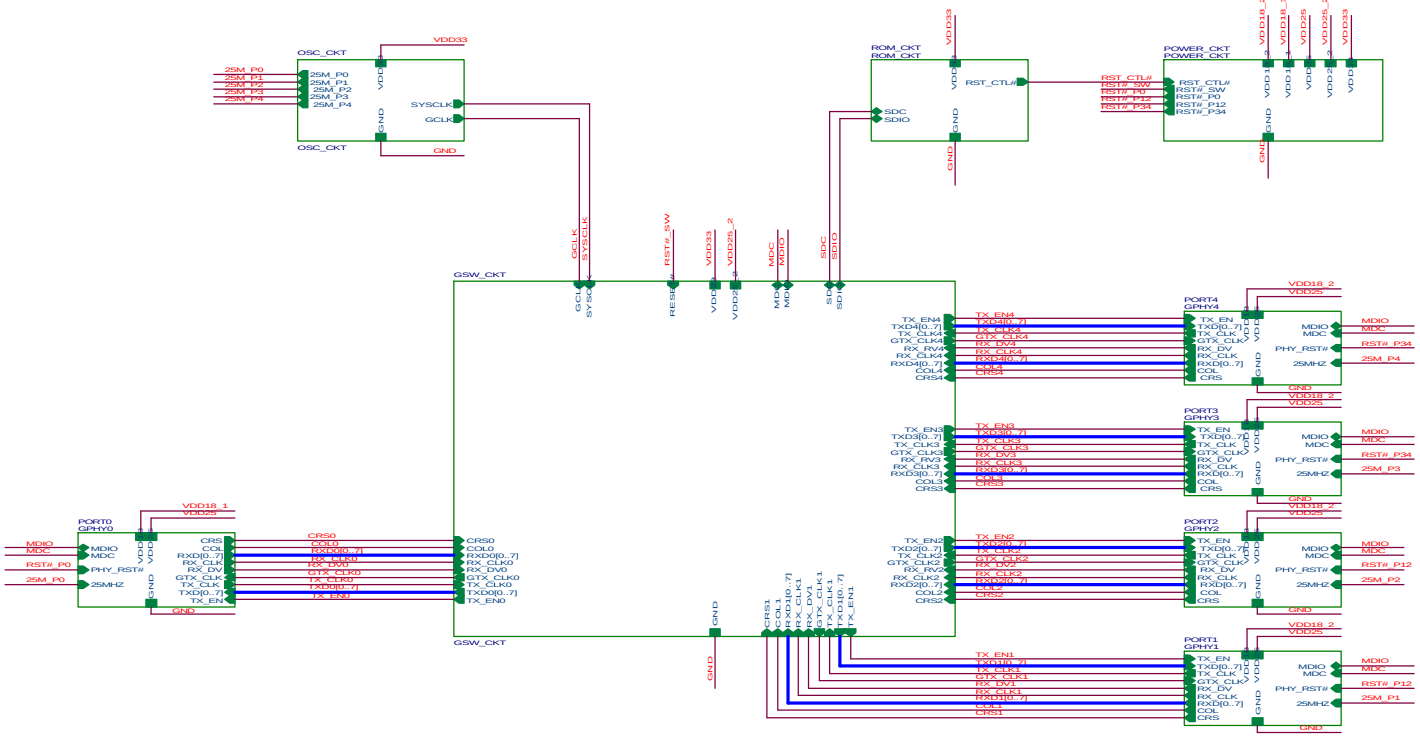
Note: 1. The MAC needs to run at full-duplex mode.
2. Care must be taken that the receive side has enough setup and/or hold time
3. Some kind of CPU with embedded MAC can also refer to this example

Appendix C: Weight Setting for QoS

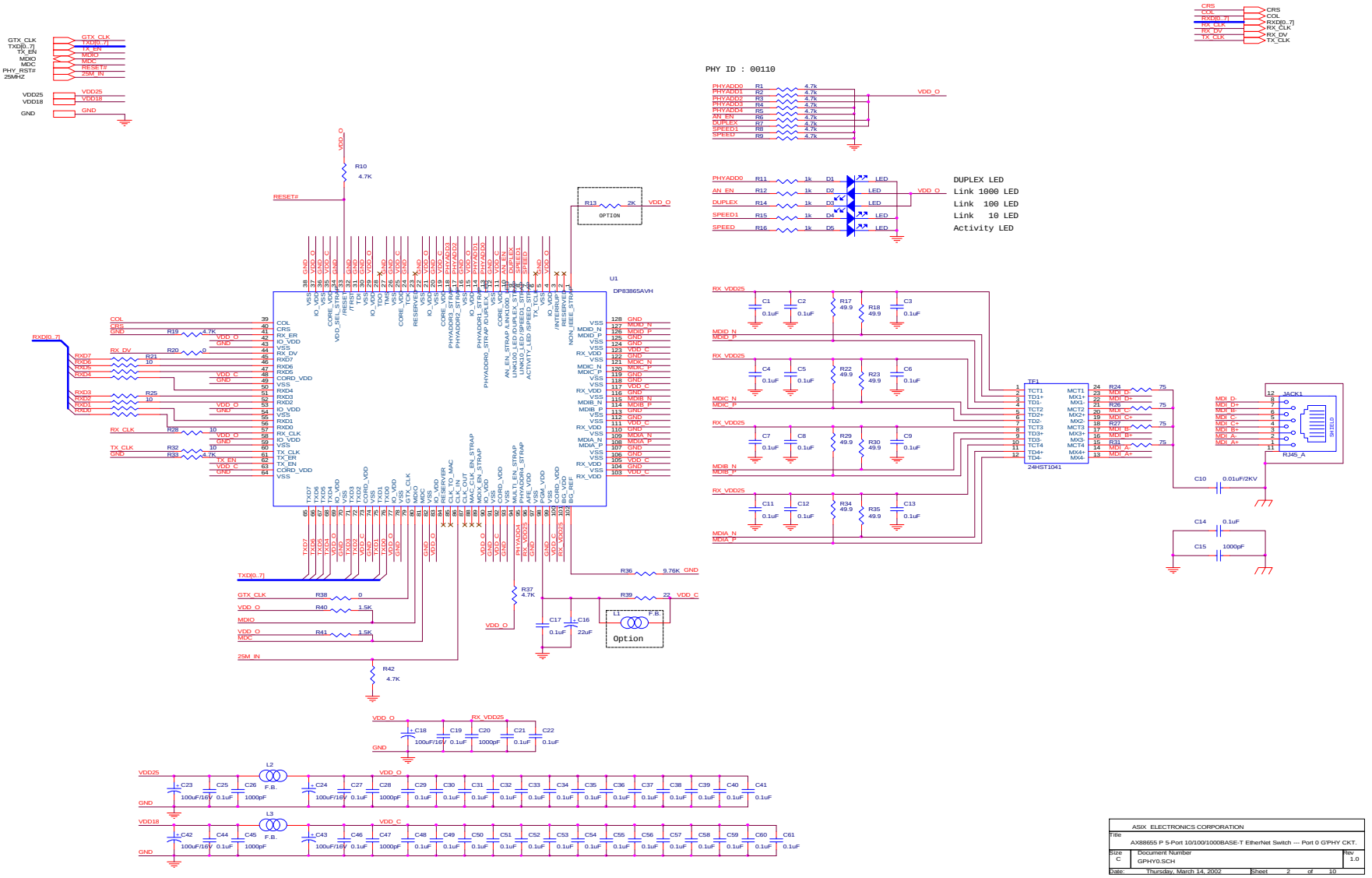
Service Ratio (High : Low)	WeightForHighQue[3:0]	WeightForLowQue[3:0]
1 : 1	4'b0100	4'b0100
2 : 1	4'b0100	4'b0010
3 : 1	4'b0110	4'b0010
4 : 1	4'b0100	4'b0001
5 : 1	4'b0101	4'b0001
6 : 1	4'b0110	4'b0001
7 : 1	4'b0111	4'b0001
8 : 1	4'b1000	4'b0001
9 : 1	4'b1001	4'b0001
10 : 1	4'b1010	4'b0001
11 : 1	4'b1011	4'b0001
12 : 1	4'b1100	4'b0001
13 : 1	4'b1101	4'b0001
14 : 1	4'b1110	4'b0001
15 : 1	4'b1111	4'b0001

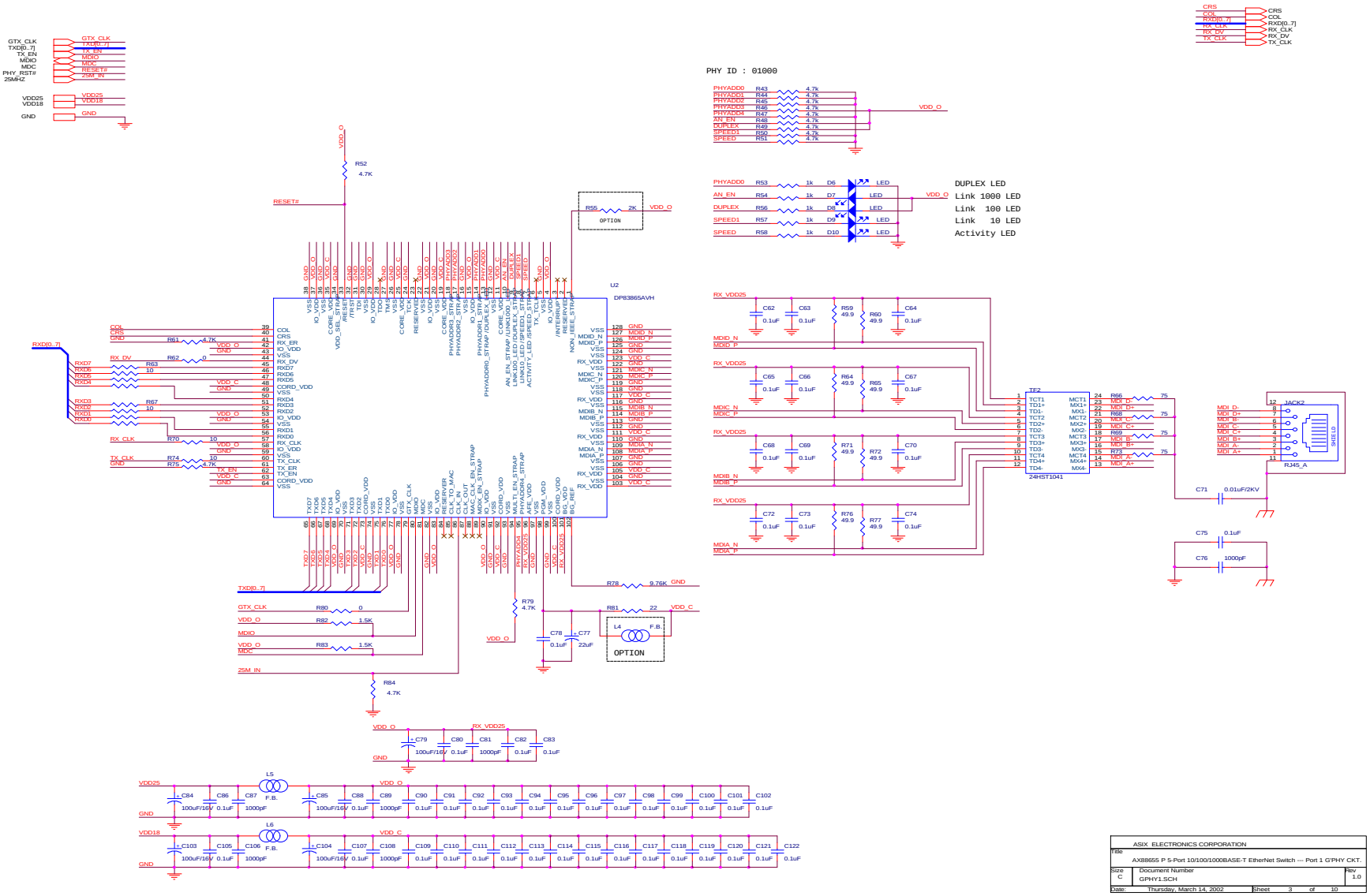
Demonstration Circuit (A) : AX88658 Smart Switch

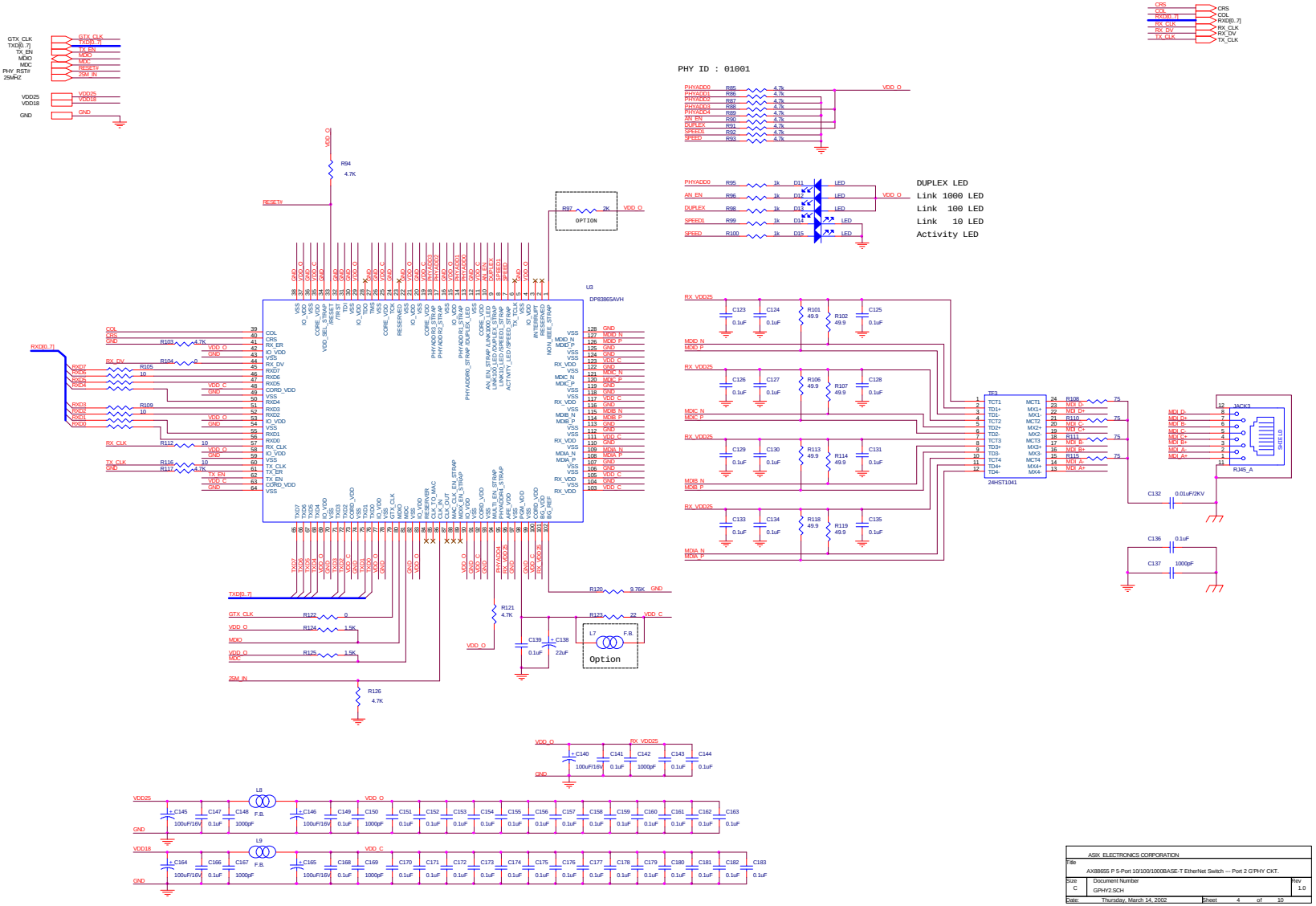
AX88655 P 5-Port 10/100/1000BASE-T Ethernet Switch Application.

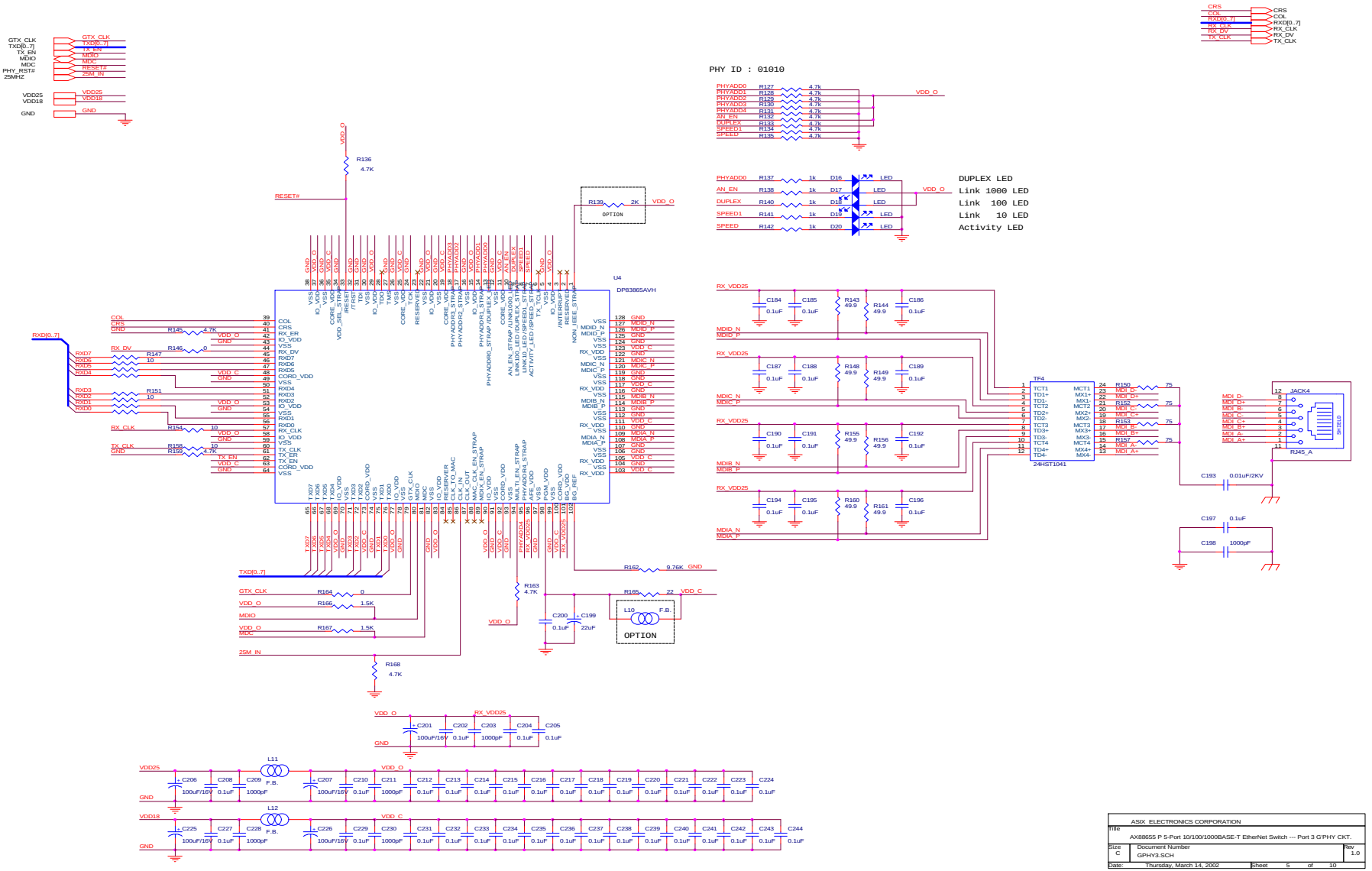


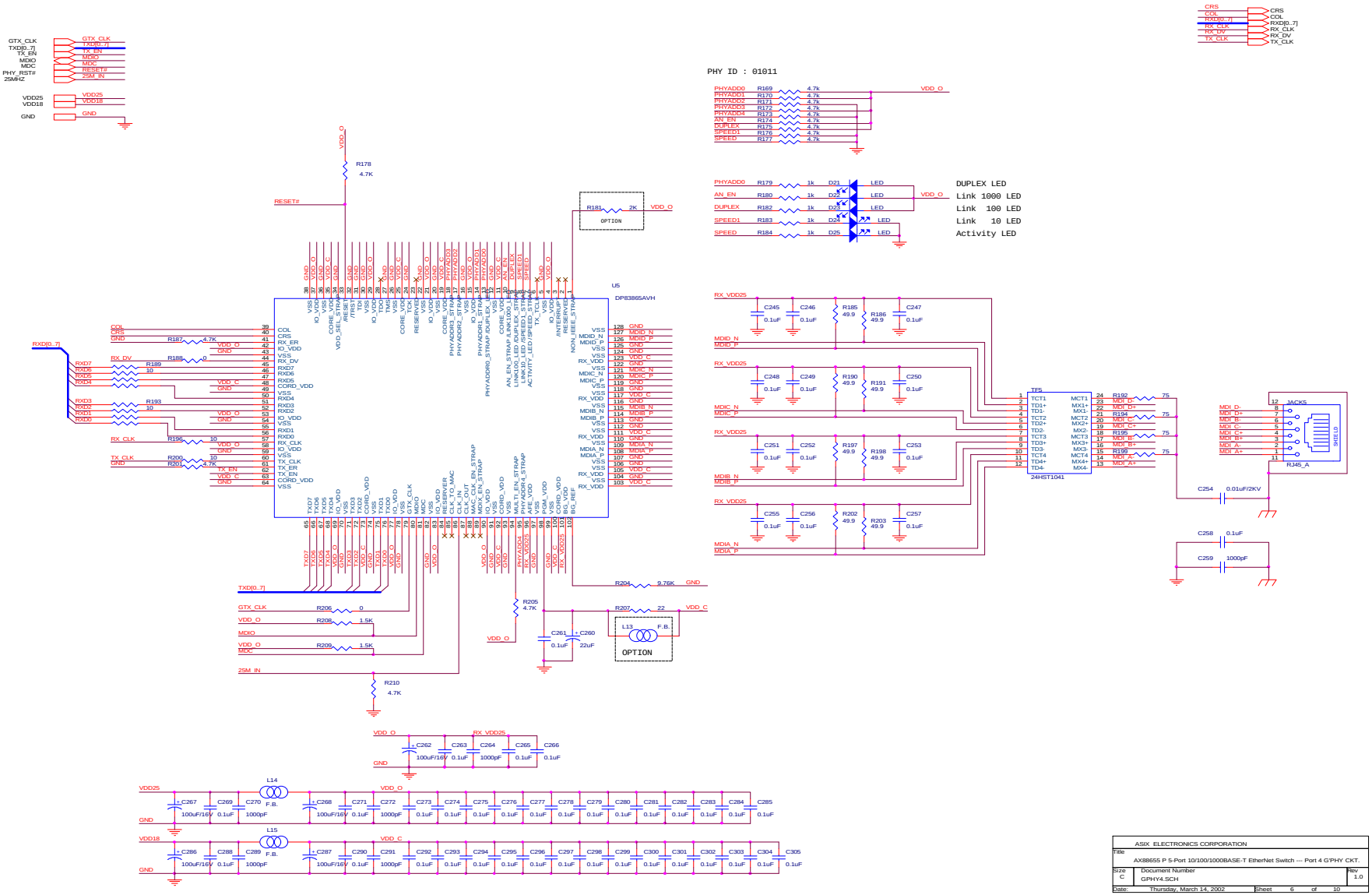
ASIX ELECTRONICS CORPORATION		
Title: AX88655 P 5-Port 10/100/1000BASE-T EtherNet Switch --- ROOT CKT.		
Size: C	Document Number: GSW_ROOT.SCH	Rev: 1.0
Date: Thursday, March 14, 2002	Sheet 1 of 10	

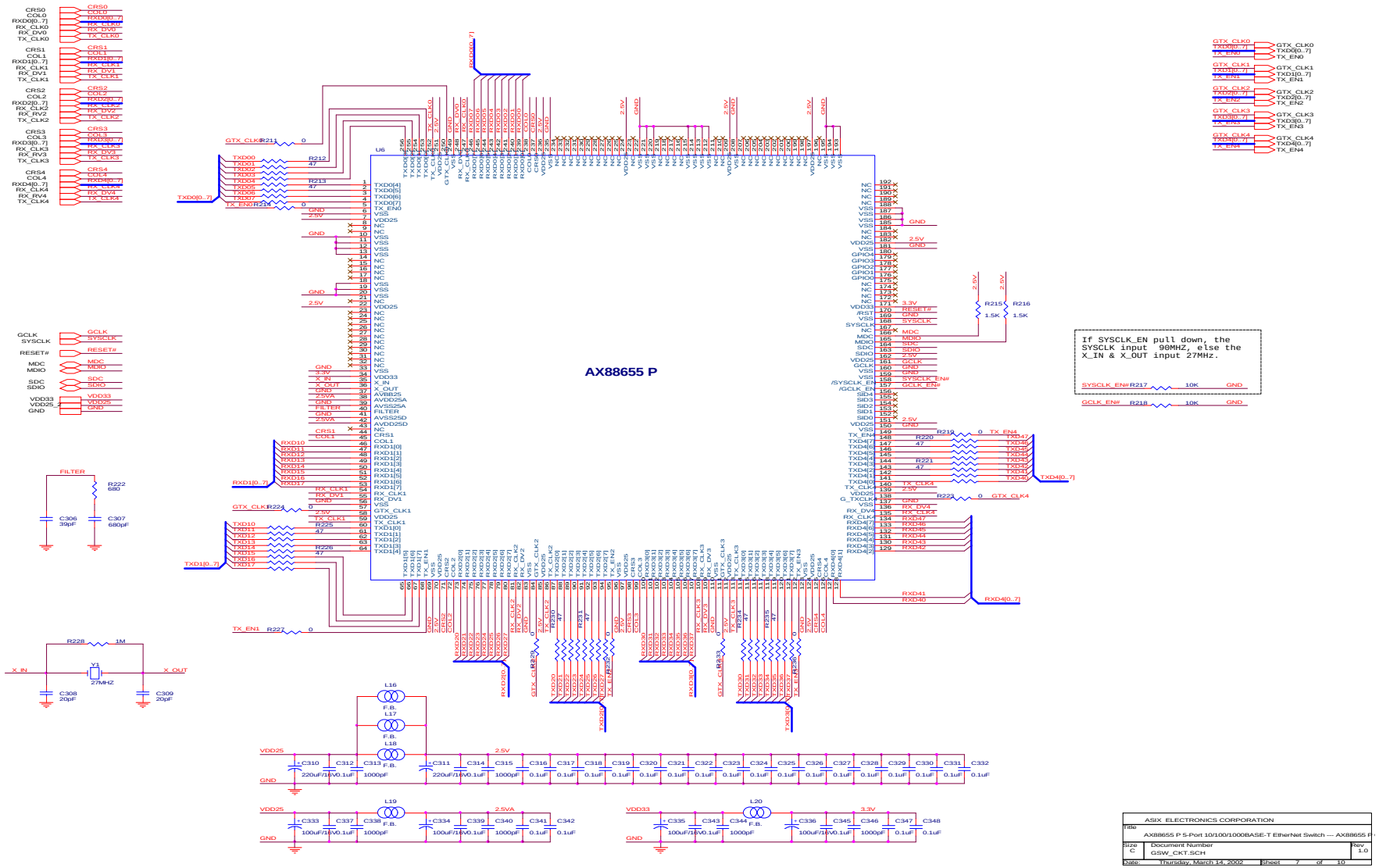

PHY ID : 00110
DUPLEX LED
Link 1000 LED
Link 100 LED
Link 10 LED
Activity LED
U1
DP83865AVH
TF1
24HST1041
JACK1
RJ45_A
OPTION
Option
ASIX ELECTRONICS CORPORATION
Title
AX88655 P 5-Port 10/100/1000BASE-T EtherNet Switch --- Port 0 G'PHY CKT.
Size C
Document Number GPHY0.SCH
Rev 1.0
Date: Thursday, March 14, 2002
Sheet 2 of 10

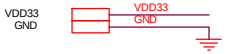

PHY ID : 01000
DUPLEX LED
Link 1000 LED
Link 100 LED
Link 10 LED
Activity LED
DP83865AVH
24HST1041
JACK2
RJ45_A
OPTION
ASIX ELECTRONICS CORPORATION
AX88655 P 5-Port 10/100/1000BASE-T EtherNet Switch — Port 1 G'PHY CKT.
GPHY1.SCH
Thursday, March 14, 2002

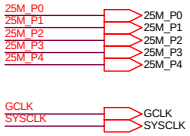

PHY ID : 01001
DUPLEX LED
Link 1000 LED
Link 100 LED
Link 10 LED
Activity LED
DP83865AVH
24HST1041
RJ45_A
Option
ASIX ELECTRONICS CORPORATION
AX88655 P 5-Port 10/100/1000BASE-T EtherNet Switch -- Port 2 G'PHY CKT.
GPHY2.SCH
Thursday, March 14, 2002

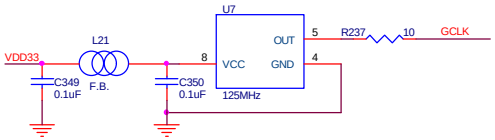

PHY ID : 01010
DUPLEX LED
Link 1000 LED
Link 100 LED
Link 10 LED
Activity LED
U4
DP83865AVH
TF4
24HST1041
JACK4
RJ45_A
OPTION
ASIX ELECTRONICS CORPORATION
AX88655 P 5-Port 10/100/1000BASE-T EtherNet Switch --- Port 3 G'PHY CKT.
Document Number
GPHY3.SCH
Thursday, March 14, 2002

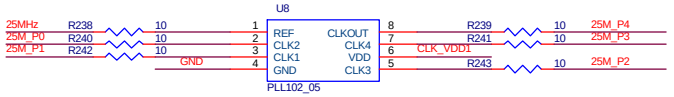

PHY ID : 01011
DUPLEX LED
Link 1000 LED
Link 100 LED
Link 10 LED
Activity LED
U5
DP83865AVH
24HST1041
JACKS
RJ45_A
OPTION
ASIX ELECTRONICS CORPORATION
AX88655 P 5-Port 10/100/1000BASE-T EtherNet Switch --- Port 4 G'PHY CKT.
GPHY4.SCH
Thursday, March 14, 2002

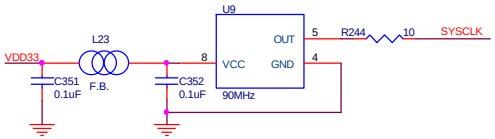

AX88655 P
If SYSCLK_EN pull down, the SYSCLK input 90MHZ, else the X_IN & X_OUT input 27MHz.
ASIX ELECTRONICS CORPORATION
AX88655 P 5-Port 10/100/1000BASE-T EtherNet Switch --- AX88655 P
Document Number GSW_CKT.SCH
Thursday, March 14, 2002

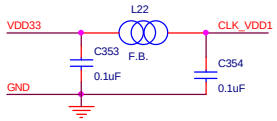


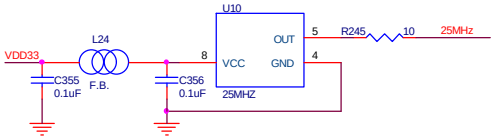




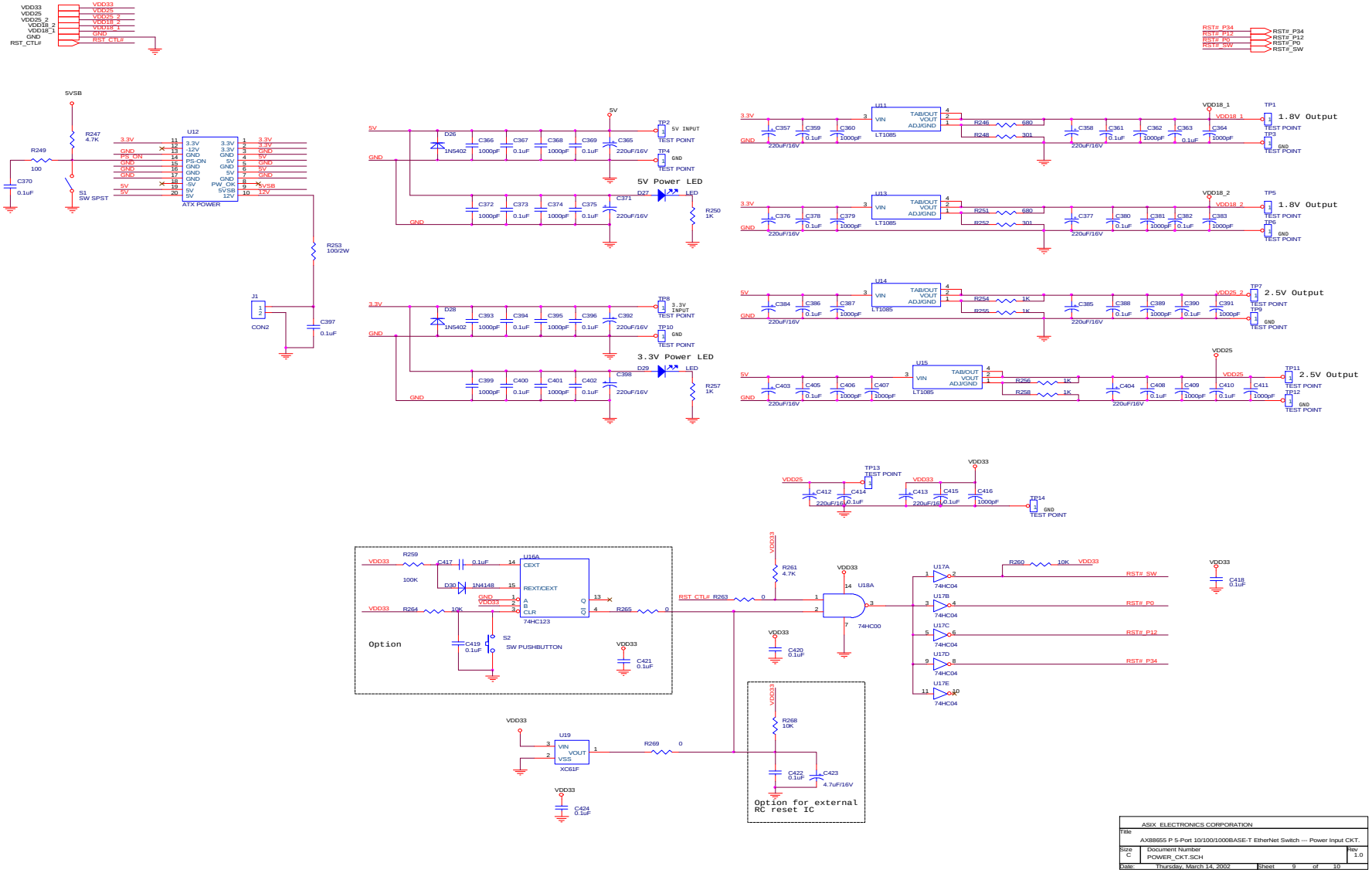








ASIX ELECTRONICS CORPORATION		
Title: AX88655 P 5-Port 10/100/1000BASE-T EtherNet Switch --- OSC CKT.		
Size: B	Document Number: OSC_CKT.SCH	Rev: 1.0
Date: Thursday, March 14, 2002	Sheet 8 of 10	

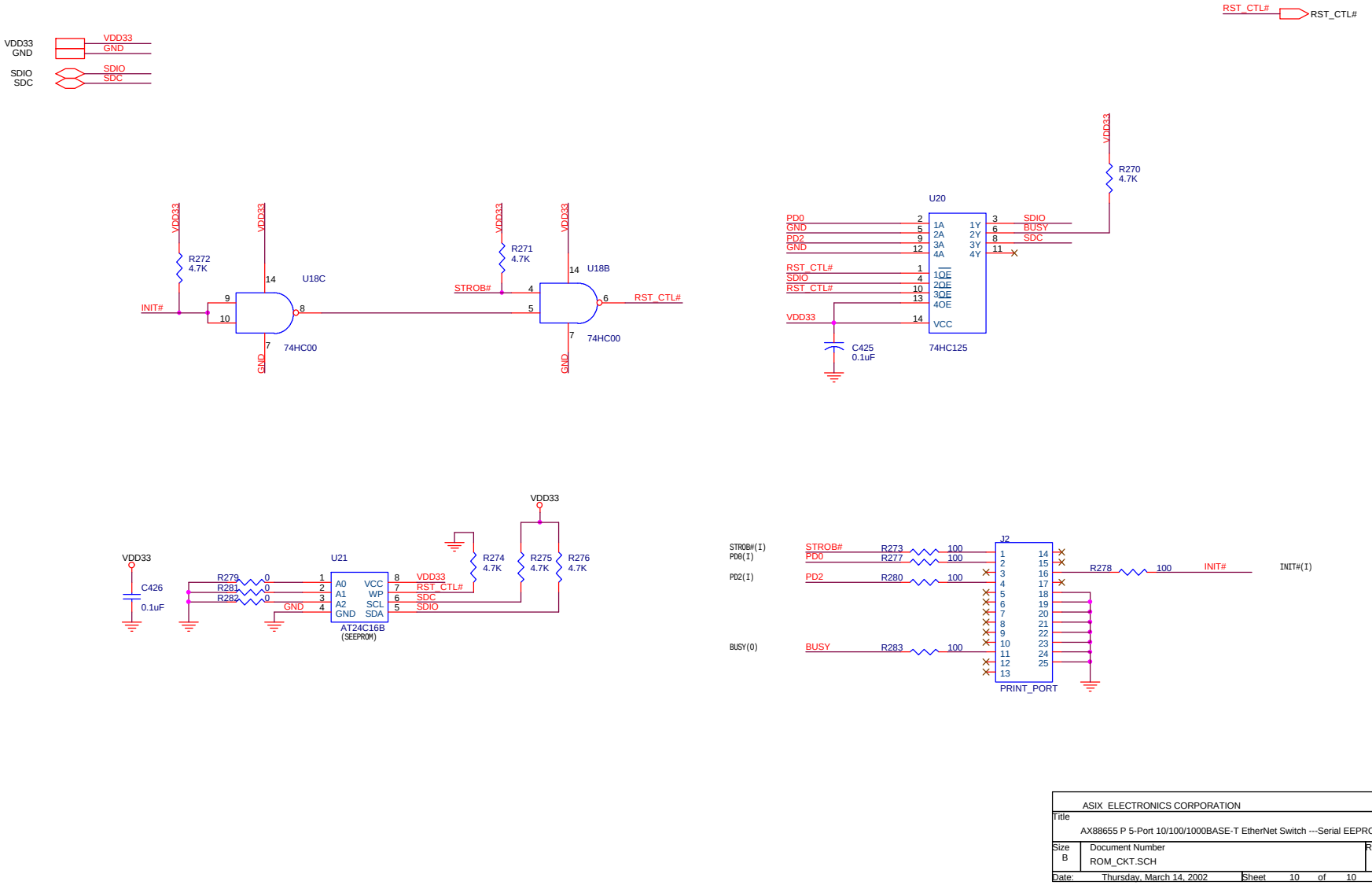


ASIX ELECTRONICS CORPORATION

Title: AX88655 P 5-Port 10/100/1000BASE-T EtherNet Switch --- Power Input CKT.

Size: C | Document Number: POWER_CKT.SCH | Rev: 1.0

Date: Thursday, March 14, 2002 | Sheet 9 of 10



ASIX ELECTRONICS CORPORATION		
Title: AX88655 P 5-Port 10/100/1000BASE-T EtherNet Switch ---Serial EEPROM CK		
Size: B	Document Number: ROM_CKT.SCH	Rev: 1.0
Date: Thursday, March 14, 2002	Sheet 10 of 10	

Revision	Date	Comment
V. 1.0	3/14/02	Initial release.

ASIX Electronics Corporation.

4F, NO.8, HSIN ANN RD., SCIENCE-BASED

INDUSTRIAL PARK, HSINCHU, TAIWAN, R.O.C.

TEL: 886-3-5799500

FAX: 886-3-5799558

Email: support@asix.com.tw

Web: http://www.asix.com.tw