2-CH, 600mA Synchronous Step-down Converter

DESCRIPTION

The EP3003 is a dual channel, 1.5MHz constant frequency, slope compensated current mode PWM step-down converter. The EP3003 can supply 600mA of load current from a 2.5V to 5.5V input voltage. Each output voltage is adjustable from 0.6V to 5V. It is ideal for powering portable equipment that runs from a single cell lithium-Ion (Li+) battery. Internal synchronous 0.35Ω, 1A power switches provide high efficiency without the need for external Schottky diodes. The EP3003 can also run at 100% duty cycle for low dropout operation, extending battery life in portable system. Pulse Skipping Mode operation at light loads provides very low output ripple voltage for noise sensitive applications. Burst Mode operation provides higher efficiency at light loads.

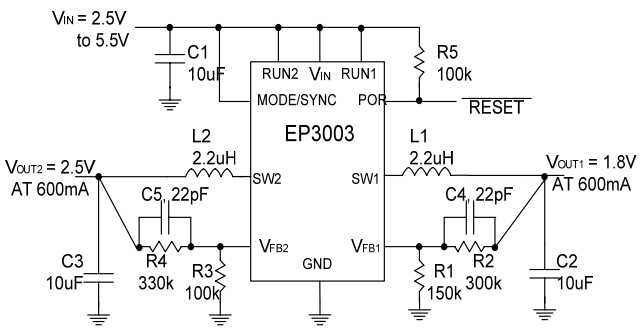
APPLICATIONS

- Cellular and Smart Phones
- Microprocessors and DSP Core Supplies
- Wireless and DSL Modems
- PDAs
- Portable Instruments / Media Players
- Digital Cameras
- PC Cards

FEATURES

- High Efficiency: Up to 96%
- 1.5MHz Constant Switching Frequency
- 600mA Output Current
- Integrated Main Switch and Synchronous Rectifier
- High Switch Current: 1A on Each Channel
- 2.5V to 5.5V Input Voltage Range
- Output Voltage as Low as 0.6V
- 100% Duty Cycle in Dropout
- Low Quiescent Current: 50μA
- Slope Compensated Current Mode Control for Excellent Line and Load Transient Response
- Can be synchronized to an external oscillator
- Short Circuit Protection
- Power-on Reset Output
- Thermal Fault Protection
- <1uA Shutdown Current
- Small Thermally Enhanced 10-Pin MSOP and 3mm × 3mm DFN Packages

Typical Application



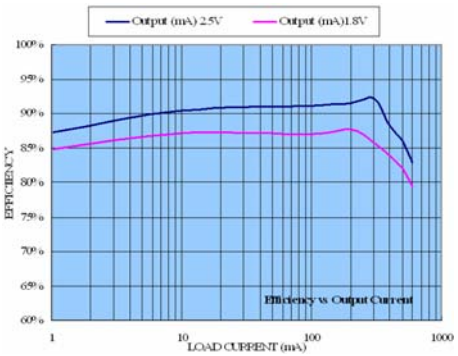
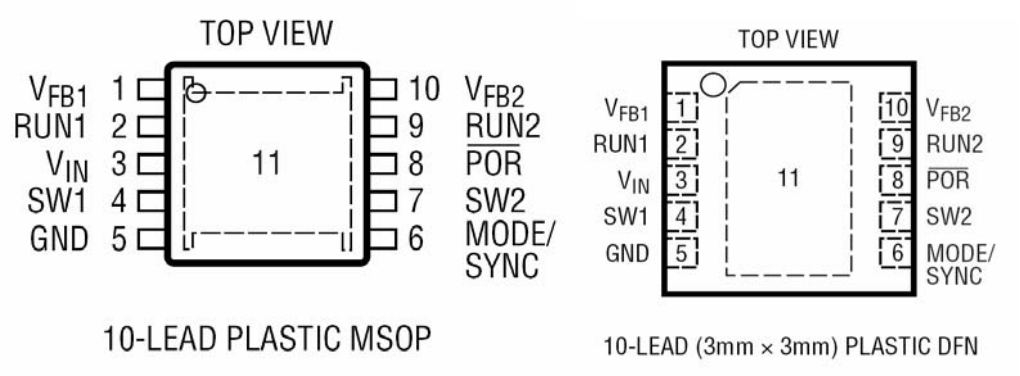


Figure 1. Basic Application Circuit for 2.5V and 1.8V Output Voltages

Package/Order Information

MSOP: **DFN:**



Eorex	Power Management	Buck Regulator	Series Number
E	***P***	***30***	***03***

Absolute Maximum Rating *(Note1)*

Input Supply Voltage..... ..... -0.3V to +6V

RUN, V_{FB} Voltages .... -0.3V to VIN+0.3V

SW Voltages.....…...-0.3V to VIN+0.3V

MODE/SYNC Voltages.....-0.3V to VIN+0.3V

/POR Voltages..... ...…... ..... -0.3V to +6V

P-Channel Switch Source Current (DC).…....800mA

N-Channel Switch Sink Current (DC).....……...800mA

Operating Temperature Range..... -40°C to +85°C

Junction Temperature…….....+125°C

Storage Temperature Range (MSOP) -65°C to +150°C

Storage Temperature Range (DFN) .. -65°C to +125°C

Lead Temperature (Soldering, 10s) .....…..+300°C

Note 1. Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

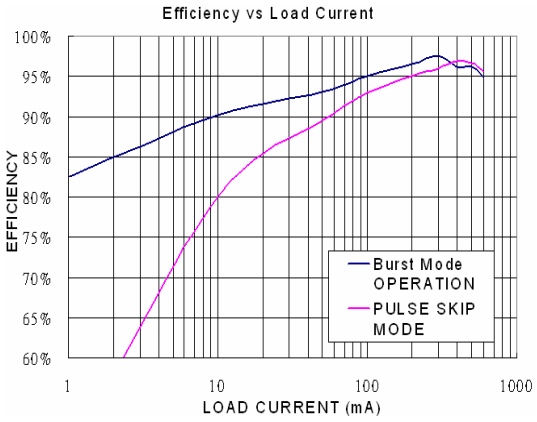
Electrical Characteristics (Note 2) :

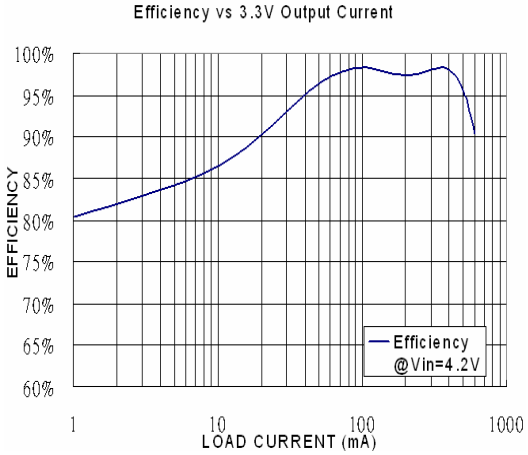
(V_{IN} =V_{RUN}= 3.6V, T_A = 25°C, unless otherwise noted.)

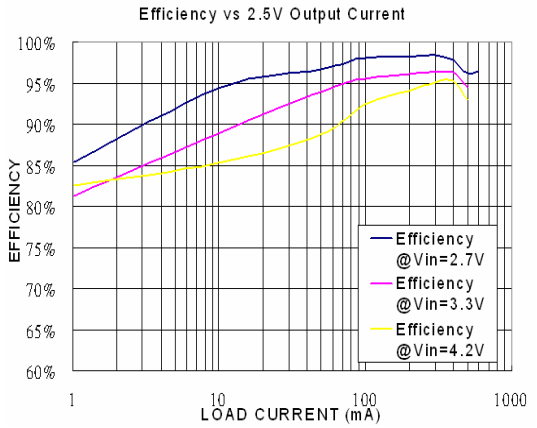
Parameter	Conditions	MIN	TYP	MAX	unit
Input Voltage Range		2.5		5.5	V
Input DC Supply Current					
Active Mode	V_{FB}=0.5V		600	800	μA
Shutdown Mode	RUN=0V, V_{IN}=5.5V, MODE/SYNC=0V		0.1	1.0	μA
Regulated Feedback Voltage	T_A = +25°C	0.588	0.600	0.612	V
	T_A= 0°C ≦ T_A ≦ 85°C	0.586	0.600	0.613	V
	T_A= -40°C ≦ T_A ≦ 85°C	0.582	0.600	0.618	V
V_{FB} Input Bias Current				30	nA
Reference Voltage Line Regulation	V_{IN} = 2.5V to 5.5V		0.3	0.5	%/V
Power-On Reset (POR)	Threshold:				
	V_{FBX} Ramping Up, MODE/SYNC = 0V		8.5		%
	V_{FBX} Ramping Down, MODE/SYNC = 0V		-8.5		%
	Power-On Reset On-Resistance		100	200	**Ω**
	Power-On Reset Delay		270K		Cycles
Output Voltage Load Regulation			0.5		%
Peak Inductor Current	V_{IN}=3V, V_{FB}=0.5V Duty Cycle < 35%	0.75	1.00	1.25	A
Oscillator Frequency	V_{FBX} =0.6V	1.2	1.5	1.8	MHz
Synchronization Frequency			1.5		MHz
$R_{DS(ON)}$	Top Switch On-Resistance		0.35	0.45	**Ω**
	Bottom Switch On-Resistance		0.30	0.45	**Ω**
SW Leakage	V_{RUN} = 0V, V_{FBX}= 0V, V_{IN} = 5V		0.01	1	μA
RUN Threshold	-40°C ≦ T_A ≦ 85°C	0.3	1.0	1.50	V
RUN Leakage Current			±0.01	±1	μA

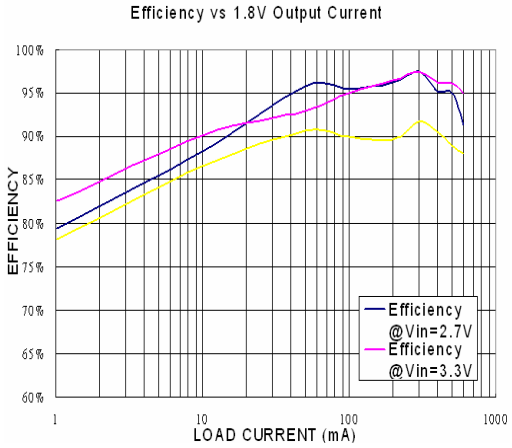
Note 2. 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

Typical Performance Characteristics (TBD)

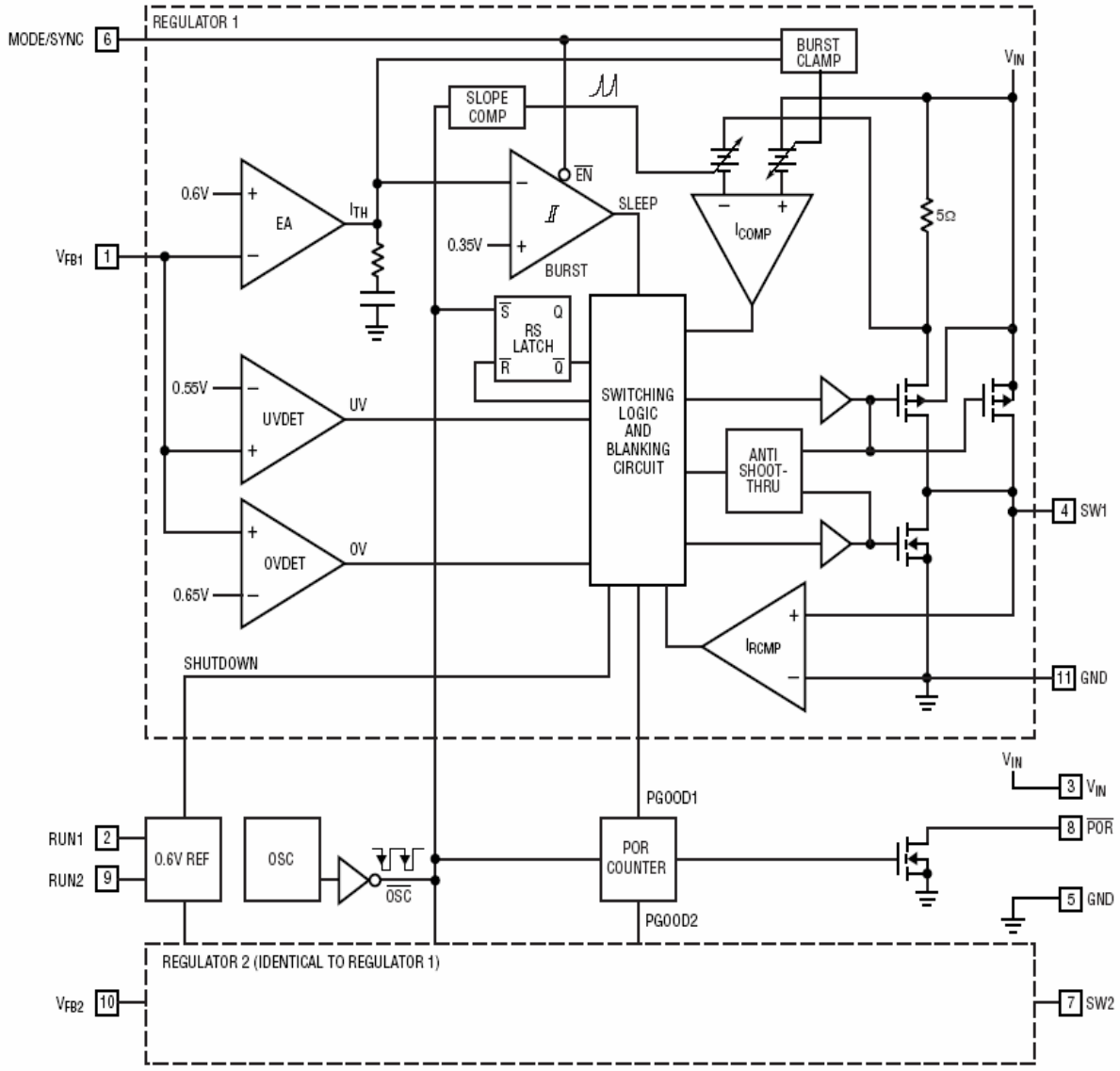








Functional Block Diagram



Pin Description

PIN	NAME	FUNCTION
1	V_{FB1}	Output Voltage Feedback Pin. An internal resistive divider divides the output voltage down for comparison to the internal reference voltage. Nominal voltage for this pin is 0.6V.
2	RUN1	Regulator 1 Enable control input. Forcing this pin to VIN enables regulator 1, while forcing it to GND causes regulator 1 to shut down. In shutdown, all functions are disabled drawing <1μA supply current. Do not leave RUN floating.
3	V_{IN}	Main Power Supply. Must be closely decoupled to GND with a ceramic capacitor.
4	SW1	Regulator 1 Power Switch Output. Switch Node Connection to the Inductor. This pin swings from VIN to GND.
5	GND	Ground
6	Mode/Sync	Combination of Mode Selection and Oscillator Synchronization. This pin controls the operation of the device. When tied to V_{IN} or GND, Burst Mode operation or pulse skipping mode is selected, respectively. Do not float this pin. The oscillation frequency can be synchronized to an external oscillator applied to this pin and pulse skipping mode is automatically selected.
7	SW2	Regulator 2 Power Switch Output. Switch Node Connection to the Inductor. This pin swings from V_{IN} to GND.
8	/POR	Power-On Reset. This common-drain logic output is pulled to GND when the output voltage is not within ±8.5% of regulation and goes high after 175ms when both channels are within regulation.
9	RUN2	Regulator 2 Enable control input. Forcing this pin to V_{IN} enables regulator 2, while forcing it to GND causes regulator 2 to shut down.
10	V_{FB2}	Output Voltage Feedback Pin for Regulator 2. See V_{FB1} section.
11	Power Ground	Connect to the (–) terminal of COUT, and (–) terminal of C_{IN}. Must be soldered to electrical ground on PCB.

OPERATION

The EP3003 uses current mode architecture with frequency set at 1.5MHz and can be synchronized to an external oscillator. Both channels share the same clock and run in-phase. To suit a variety of applications, the selectable Mode pin allows the user to trade-off noise for efficiency.

Output voltage is set by an external divider returned to the VFB pins. An error amplifier compares the divided output voltage with a reference voltage of 0.6V and adjusts the peak inductor current accordingly. Over voltage and under voltage comparators will pull the POR output low if the output voltage is not within ±8.5%. The POR output will go high after 270K clock cycles of achieving regulation. During normal operation, the top power switch (P-channel MOSFET) is turned on at the beginning of a clock cycle when the VFB voltage is below the reference voltage.

The current into the inductor and the load increases until the current limit is reached. The switch turns off and energy stored in the inductor flows through the bottom switch (N-channel MOSFET) into the load until the next clock cycle.

The peak inductor current is controlled by the internally compensated ITH voltage, which is the output of the error amplifier. This amplifier compares the VFB pin to the 0.6V reference. When the load current increases, the V_{FB} voltage decreases slightly below the reference. This decrease causes the error amplifier to increase the ITH voltage until the average inductor current matches the new load current. The main control loop is shut down by pulling the RUN pin to ground.

Low Current Control

Two modes are available to control the operation of the EP3003 at low currents. Both modes automatically switch from continuous operation to the selected mode when the load current is low.

To optimize efficiency, the Burst Mode operation can be selected. When the load is relatively light, the EP3003 automatically switches into Burst Mode operation in which the PMOS switch operates intermittently based on load demand with a fixed peak inductor current. By running cycles periodically, the switching losses which are dominated by the gate charge losses of the power MOSFETs are minimized. The main control loop is interrupted when the output voltage reaches the desired regulated value. A hysteretic voltage comparator trips when ITH is below 0.35V, shutting off the switch and reducing the power. The output capacitor and the inductor supply the power to the load until ITH exceeds 0.65V, turning on the switch and the main control loop which starts another cycle.

For lower ripple noise at low currents, the pulse skipping mode can be used. In this mode, the EP3003 continues to switch at a constant frequency down to very low currents, where it will begin skipping pulses.

Dropout Operation

The EP3003 allows the main switch to remain on for more than one switching cycle and increases the duty cycle until it reaches 100%. The output voltage then is the input voltage minus the voltage drop across the main switch and the inductor. At low input supply voltage, the $R_{DS(ON)}$ of the P Channel MOSFET increases, and the efficiency of the converter decreases. Caution must be exercised to ensure the heat dissipated not to exceed the maximum junction temperature of the IC.

Note 3. The duty cycle D of a step-down converter is defined as:

$D = T_{ON} \times f_{OSC} \times 100\% \approx V_{OUT}/V_{IN} \times 100\%$

where T_{ON} is the main switch on time, and f_{OSC} is the oscillator frequency (1.5MHz).

Maximum Load Current

The EP3003 will operate with input supply voltage as low as 2.5V, however, the maximum load current decreases at lower input due to large IR drop on the main switch and synchronous rectifier. The slope compensation signal reduces the peak inductor current as a function of the duty cycle to prevent sub-harmonic oscillations at duty cycles greater than 50%. Conversely the current limit increases as the duty cycle decreases.

APPLICATIONS INFORMATION

A general application circuit for EP3003 is shown in Figure 1, which is the baseline for some calculation mentioned below. All external component selection for EP3003 application design will be illustrated as the following.

Setting the Output Voltage

The external resistor sets the output voltage according to the following equation:

$$V_{out} = 0.6V\left(1 + \frac{R2}{R1}\right)$$

R1 = 150K**Ω**; R2 = 300K**Ω** for V_{OUT} = 1.8V;

R3 = 100K**Ω**; R4 = 330K**Ω** for V_{OUT} = 2.5V.

Inductor Selection

For most designs, the EP3003 operates with inductors of 1μH to 4.7μH. Low inductance values are physically smaller but require faster switching, which results in some efficiency loss. Large value inductors lower ripple current and small value inductors result in high ripple currents. The inductor value can be derived from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

where ΔI_L is inductor Ripple Current. Choose inductor ripple current approximately 35% of the maximum load current 600mA, or *2*10mA.

For output voltages above 2.0V, when light-load efficiency is important, the minimum recommended inductor is 2.2μH. For optimum voltage-positioning load transients, choose an inductor with DC series resistance in the 50m**Ω** to 150m**Ω** range. For higher efficiency at heavy loads (above 200mA), or minimal load regulation (but some transient overshoot), the resistance should be kept below 100m**Ω**. The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation (600mA+105mA). Table 1 lists some typical surface mount inductors that meet target applications for the EP3003.

Part #	L (μH)	Max DCR (m.)	Rated D.C. Current (A)	Size WxLxH (mm)
Sumida	1.4	56.2	2.52	4.5x4.0x3.5
CR43	2.2	71.2	1.75	
	3.3	86.2	1.44	
	4.7	108.7	1.15	
Sumida	1.5			4.7x4.7x2.0
CDRH4D18	2.2	75	1.32	
	3.3	110	1.04	
	4.7	162	0.84	
Toko	1.5	120	1.29	3.6x3.6x1.2
D312C	2.2	140	1.14	
	3.3	180	0.98	
	4.7	240	0.79	

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency shall be less than input source impedance to prevent high frequency switching current passing to the input. A low ESR input capacitor sized for maximum RMS current must be used. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 10μF ceramic capacitor for most applications is sufficient.

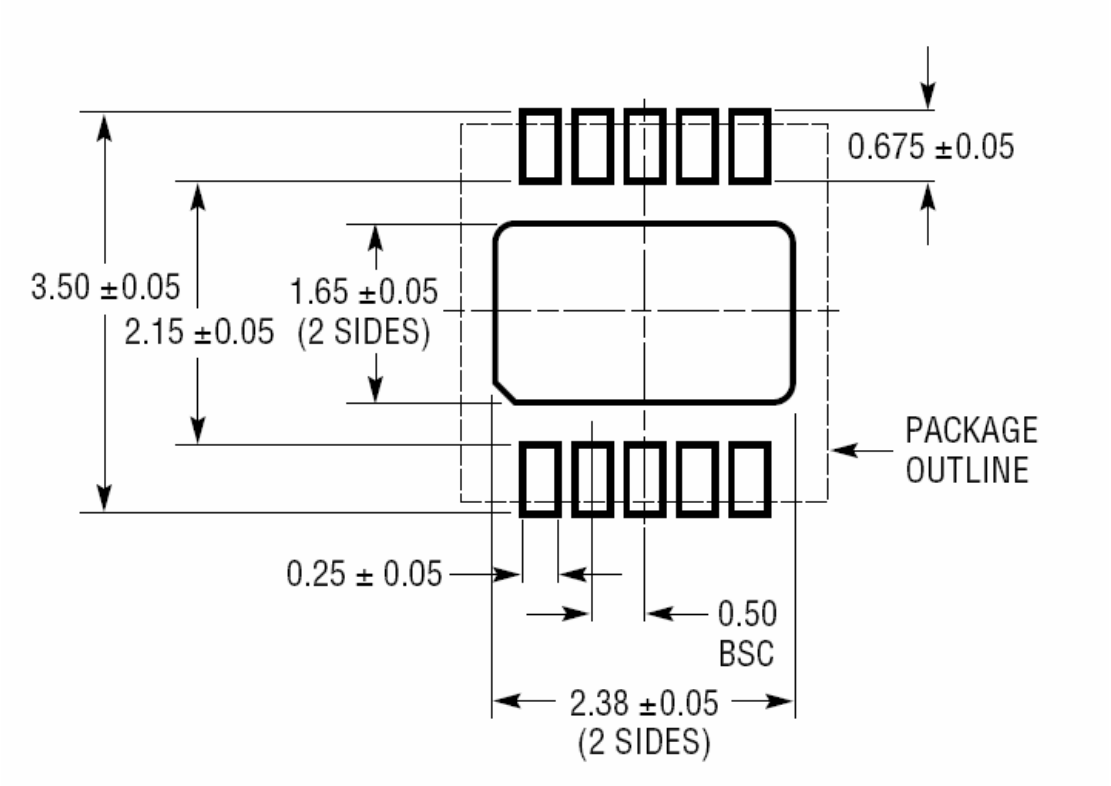
Output Capacitor Selection

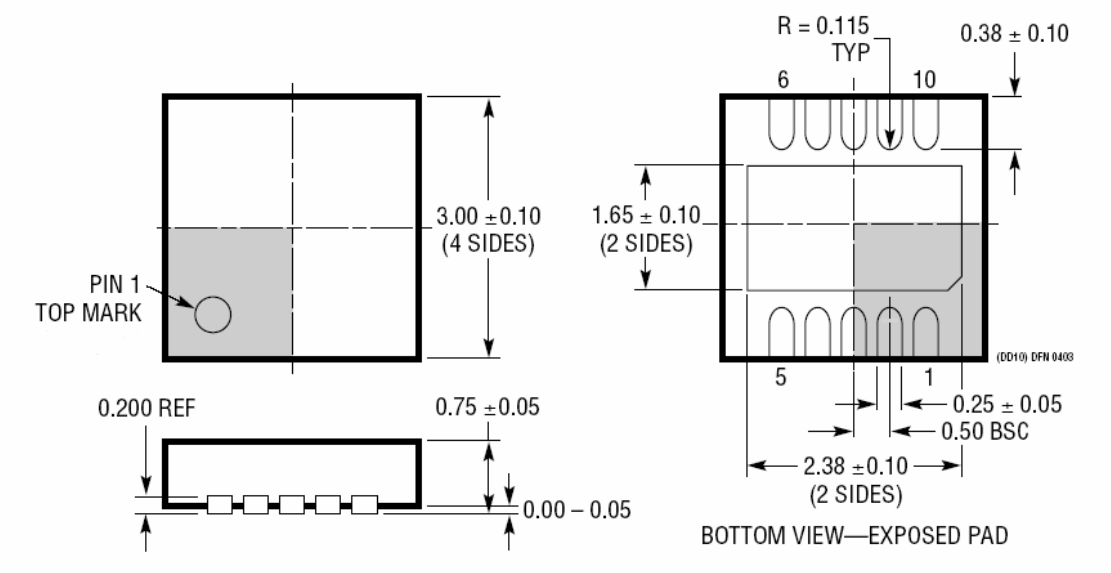
The output capacitor is required to keep the output voltage ripple small and to ensure regulation loop stability. The output capacitor must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and minimization of large temperature and voltage coefficients. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \le \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{OSC} \times L} \times \left(ESR + \frac{1}{8 \times f_{OSC} \times C3} \right)$$

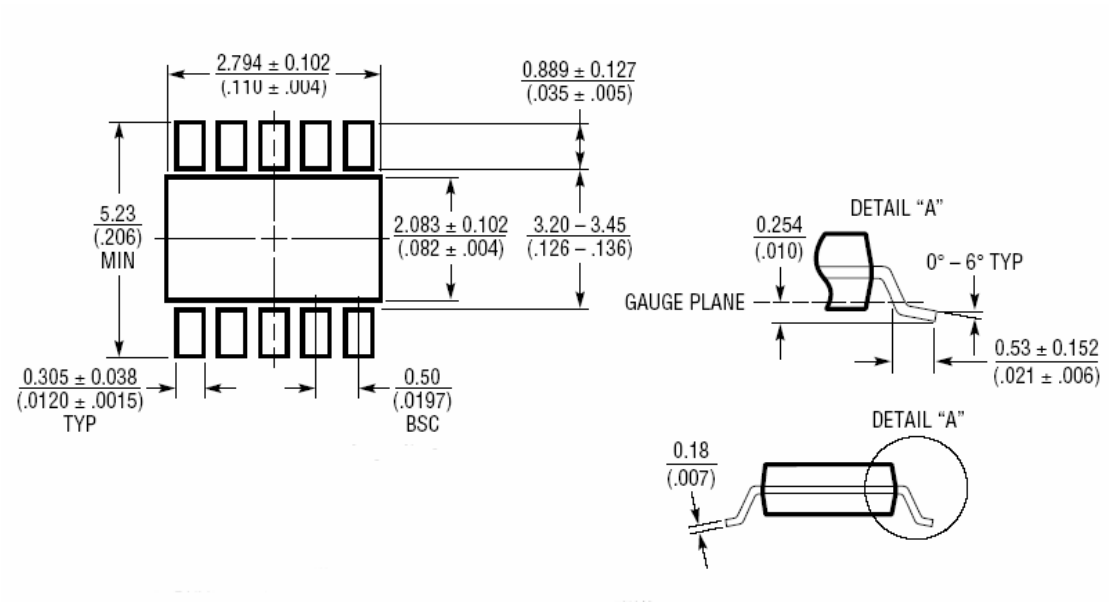
Package Description

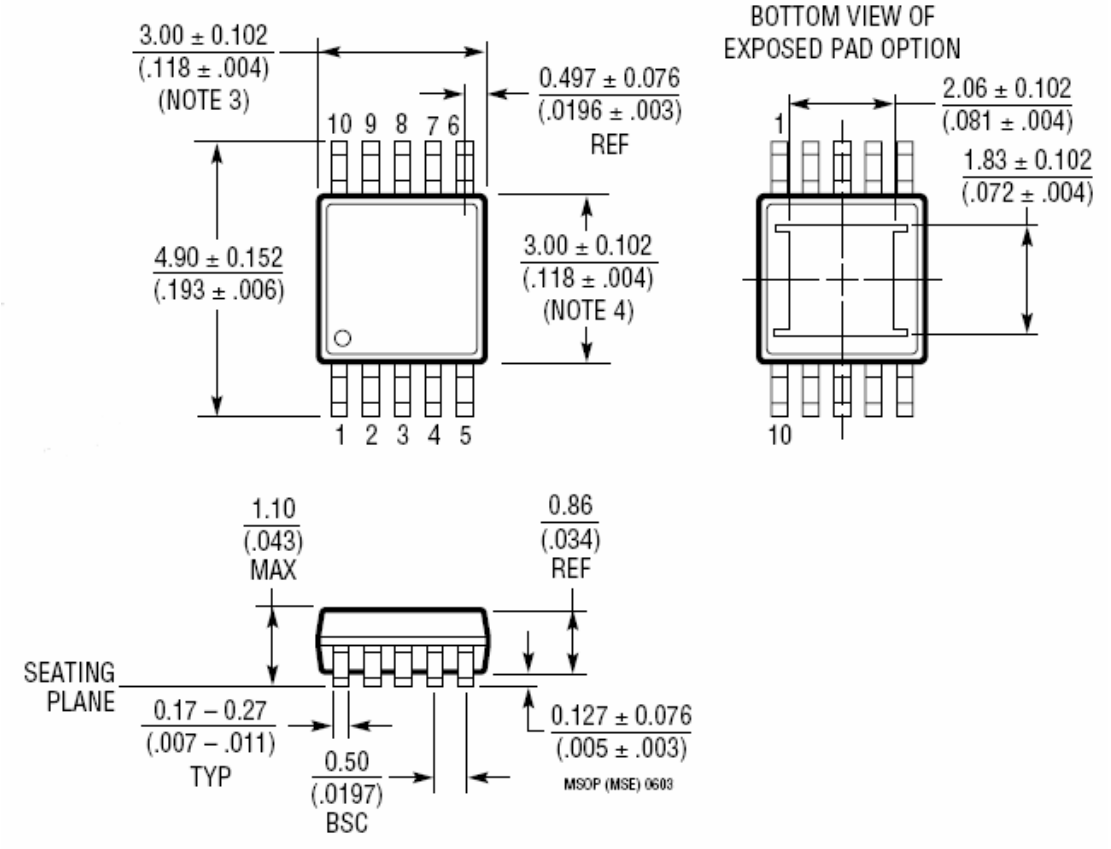
DFN:





MSOP:


2.794 ± 0.102
(.110 ± .004)
0.889 ± 0.127
(.035 ± .005)
5.23
(.206)
MIN
2.083 ± 0.102
(.082 ± .004)
3.20 – 3.45
(.126 – .136)
0.305 ± 0.038
(.0120 ± .0015)
TYP
0.50
(.0197)
BSC
DETAIL "A"
0.254
(.010)
0° – 6° TYP
GAUGE PLANE
0.53 ± 0.152
(.021 ± .006)
DETAIL "A"
0.18
(.007)


3.00 ± 0.102
(.118 ± .004)
(NOTE 3)
10 9 8 7 6
0.497 ± 0.076
(.0196 ± .003)
REF
4.90 ± 0.152
(.193 ± .006)
3.00 ± 0.102
(.118 ± .004)
(NOTE 4)
1 2 3 4 5
BOTTOM VIEW OF
EXPOSED PAD OPTION
1
2.06 ± 0.102
(.081 ± .004)
1.83 ± 0.102
(.072 ± .004)
10
1.10
(.043)
MAX
0.86
(.034)
REF
SEATING
PLANE
0.17 – 0.27
(.007 – .011)
TYP
0.50
(.0197)
BSC
0.127 ± 0.076
(.005 ± .003)
MSOP (MSE) 0603