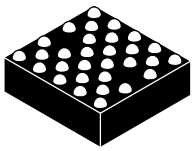
BelaSigna R261

Advance Information

Advanced Noise Reduction Solution for Voice Capture Devices

ON Semiconductor®

http://onsemi.com



WLCSP−30
W SUFFIX
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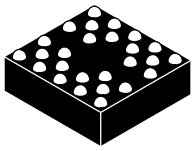

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Introduction

BelaSigna® R261 is a complete system−on−chip (SoC) solution that provides advanced dual−microphone noise reduction in voice capture applications such as laptops, mobile phones, webcams, tablet computers and other applications that will benefit from improved voice clarity.

Featuring a novel approach to removing mechanical, stationary and non−stationary noise, the chip preserves voice naturalness for greater speech intelligibility even when the talker is further away or not optimally aligned with microphones providing unmatched freedom of movement for end−users. Designed to be compatible with a wide range of codecs, baseband chips and microphones without the need for calibration, BelaSigna R261 is easy to integrate, improving manufacturers' speed to market.

Additional features include the ability to customize multiple voice capture modes and tune the algorithm to the unique needs of a manufacturer's device. The chip includes a highly optimized DSP−based application controller with industry−leading energy efficiency and is packaged in two highly compact 5.3 mm^2 WLCSPs to fit into even the most sized−constrained architectures and allow the use of the cheapest printed circuit board design technologies.

Key Features

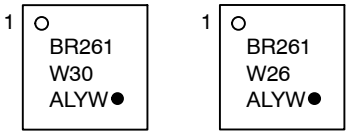
- Advanced Two−Microphone Noise Reduction Algorithm
- Preserves Voice Naturalness
- Supports Close−Talk and Far−Talk
- Conference Mode enables 360 Degrees Voice Pick−up
- Configurable Algorithm Performance
- Ultra Low Power Consumption
- Ultra Miniature Form Factor
- Complete System−on−Chip (SoC)
- Highly Flexible Clocking Architecture
- Hardware Configuration Interfaces
- Prototyping Tools
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Laptop Computers
- Mobile Phones
- Tablet PCs
- Webcams
- Any Portable Audio Application with Voice Pick−up

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MARKING DIAGRAMS



BR261	= BelaSigna R261
W30	= 30−ball version
W26	= 26−ball version
A	= Assembly Location
L	= Wafer Lot
YW	= Date Code Year & Week
●	= Pb−Free Package
○	= A1 Corner Indicator

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 28 of this data sheet.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Power Supply (Applies on VBAT, VBATRCVR and VDDO for “Max” and for VSSA, VSSRCVR and VSSD for “Min”) (Note 1)	−0.3	4.0	V
Digital input pin voltage	VSSA − 0.3 V	VDDO + 0.3 V	V
Operating temperature range	−40	85	°C
Storage temperature range	−40	85	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Time limit at maximum voltage must be less than 100 ms.

NOTE: Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

This device series incorporates ESD protection and is tested by the following methods:
- ESD Human Body Model (HBM) tested per AEC−Q100−002 (EIA/JESD22−A114)
- ESD Machine Model (MM) tested per AEC−Q100−003 (EIA/JESD22−A115)
- ESD Charge Discharge Model (CDM) tested per ESD−STM 5−3−1−1999.

This device series incorporates latch−up immunity and is tested in accordance with JESD78:

Electrical Performance Specifications

Table 2. ELECTRICAL CHARACTERISTICS (The typical parameters in Table 2 were measured at 20°C with a clean 3.3 V supply voltage (unless noted differently). Parameters marked as screened are tested on each chip. Other parameters are qualified for all process corners but not tested on every part.)

Parameter	Symbol	Test Conditions / Notes	Min	Typ	Max	Unit	Screened
OVERALL							
Supply voltage	VBAT		1.8	3.3	3.63	V	
Maximum risetime	VBAT_RISE	Between 0 V and 1.8 V			10	ms	
Current consumption	IBAT_ACTIVE	Active mode, VBAT = 3.3 V		15		mA	
	IBAT_BPASS	Bypass mode, VBAT = 3.3 V		2.5	3	mA	
	IBAT3_LOUT	Lineout mode, VBAT = 3.3 V		1.2	2	mA	
	IBAT4_SLEEP	Sleep mode, VBAT = 3.3 V		40		μA	
VREG (1 μF External Capacitor)							
Output voltage	VREG	Without load, or with micro-phone attached (0 to 200 μA)	0.95	1	1.05	V	
PSRR	VREG_PSRR	@ 1 kHz	54			dB	
Load regulation	VREG_LdReg	@ 2 mA			6	mV/mA	
Load current	VREG_ILoad				2	mA	
Line regulation	VREG_LnReg				0.065	mV/V	
VDDA (1 μF External Capacitor on VDDA + 100 nF External Capacitor on CAP0/CAP1)							
Output voltage	VDDA	Unloaded with VREG = 1 V	1.8	2	2.1	V	
PSRR	VDDA_PSRR	@ 1 kHz	45			dB	
Load regulation	VDDA_LdReg	@ 1 mA, MCLK = 1.28 MHz		110	140	mV/mA	
		@ 1 mA, MCLK = 2.56 MHz		70	100	mV/mA	
Load current	VDDA_ILoad				1	mA	
Line regulation	VDDA_LnReg				0.126	mV/V	
VDDD (1 μF External Capacitor)							
Output voltage	VDDD		1.62	1.8	1.98	V	
VMIC							
Output voltage	VMIC_VREG	VMIC = VREG	0.98	1.0	1.01	V	
	VMIC_VDDA	VMIC = VDDA	1.95	1.98	2.01	V	

Table 2. ELECTRICAL CHARACTERISTICS (continued) (The typical parameters in Table 2 were measured at 20°C with a clean 3.3 V supply voltage (unless noted differently). Parameters marked as screened are tested on each chip. Other parameters are qualified for all process corners but not tested on every part.)

Parameter	Symbol	Test Conditions / Notes	Min	Typ	Max	Unit	Screened
VMIC							
Load Regulation	VMIC_LdReg	VMIC = VREG			40	mV/mA	
	VMIC_LdReg	VMIC = VDDA			146	mV/mA	
Maximum Load Current	VMIC_ILoad	VMIC = VREG			2	mA	
		VMIC = VDDA			1	mA	
POWER ON RESET							
POR Threshold	POR_THR_UP	Active on VBAT	1.55	1.65	1.71	V	
	POR_THR_DN	Active on VBAT	1.55	1.6	1.65	V	
POR Duration	POR_TIME		3.9	5.8	11.6	ms	
INPUT STAGE							
Sampling frequency	SF	Defined by ROM−based application.		16		kHz	
Analog input voltage	Vin_AI1_3	No preamp gain on AI1 and AI3	0		2	Vpp	
	Vin_MIC0_2	30 dB preamp gain by default on MIC0 and MIC2	0		63.25	mVpp	
Preamplifier gain tolerance	Vin_Amp_Toll	1 kHz	−2		2	dB	
Input impedance	Vin_Rin	0 dB preamplifier gain, MCLK = 1.28 MHz	220		254	kΩ	
		All other gain settings	510		585	kΩ	
		Line−Out	5.2		5.35	kΩ	
Input offset voltage	Vin_Offset	0 dB preamp gain			7	mV	
	Vin_Offset	All other gains			0.6	mV	
Channel cross coupling	Vin_Coupling	Any 2 channels		−84	−60	dB	
Analog Filter cut−off frequency	AnaIF_FC1	LPF enabled	10	20	30	kHz	
	AnaIF_FC2	LPF disabled	50			kHz	
Analog Filter passband flatness	AnaIF_PB_F		−1		1	dB	
Analog filter stopband attenuation	AnaIF_SB_A		60			dB	
Digital Filter cut−off frequency	DigIF_FC			8		kHz	
Digital Filter cut−off stopband attenuation	DigIF_SB_A		80			dB	
Total Harmonic Distortion + Noise (Peak value)	AI_THDN	30 dB preamplifier gain VBAT = 3.3 V	−64	−68		dB	
Dynamic Range	AI_DR	30 dB preamplifier gain VBAT = 3.3 V	−77	−78		dB	
Equivalent Input Noise	EIN	30 dB preamplifier gain VBAT = 3.3 V			3.25	μV	
DIGITAL MICROPHONE OUTPUT							
DMIC input clock frequency	DMIC_CLK1	With presets 0 or 5 selected on CONFIG_SEL		2.048		MHz	
	DMIC_CLK2	With preset 1 selected on CONFIG_SEL		2.4		MHz	

Table 2. ELECTRICAL CHARACTERISTICS (continued) (The typical parameters in Table 2 were measured at 20°C with a clean 3.3 V supply voltage (unless noted differently). Parameters marked as screened are tested on each chip. Other parameters are qualified for all process corners but not tested on every part.)

Parameter	Symbol	Test Conditions / Notes	Min	Typ	Max	Unit	Screened
DIGITAL MICROPHONE OUTPUT							
DMIC input clock frequency	DMIC_CLK3	With preset 3 elected on CONFIG_SEL		2.8		MHz	
	DMIC_CLK4	With preset 2 selected on CONFIG_SEL		3.072		MHz	
Clock duty cycle	DMIC_DC	Any clock configuration	40	50	60	%	
Input clock jitter	DMIC_JITTER	Maximum allowed jitter on the DMIC_CLK			10	ns	
Setup time	DMIC_SETUP	DMIC_OUT setup time relative to DMIC_CLK edge	0.5		1.5	SYSCLK cycles	
Hold time	DMIC_HOLD	DMIC_OUT hold time relative to DMIC_CLK edge	10		100	ns	
ANALOG OUTPUT STAGE							
Signal Range	AO_Range	One single ended DAC used	0		2	Vpp	
		Two DACs used as one differential output	0		4	Vpp	
Attenuator gain tolerance	Vout_Att_Tol		−2		2	dB	
Output impedance	AO_Rout	@ 12 dB output attenuation			16	kΩ	
		@ 0 dB output attenuation			3	kΩ	
Channel cross coupling	AO_Coupling				−65	dB	
Analog Filter cut−off frequency	AnaOF_FC1	LPF Enabled	13		13.5	kHz	
		LPF Disabled	25		26	kHz	
Analog Filter passband flatness	AnaOF_PB_F		−1		1	dB	
Analog filter stopband attenuation	AnaOF_SB_A	> 60 kHz	90			dB	
Digital Filter cut−off frequency	DigOF_FC			8		kHz	
Digital Filter cut−off stopband attenuation	DigOF_SB_A		80			dB	
Total Harmonic Distortion + Noise (Peak value)	AO_THDN		−64	−68		dB	
Dynamic Range	AO_DR		−80	−82		dB	
NoiseFloor	AO_NF				100	μV	
DIRECT DIGITAL OUTPUT (available only through custom mode)							
Supply voltage	VBATRCVR		1.8	3.3	3.63	V	
Signal Range	RCVR_Range	One Differential Output Driver used @ 1 kHz	0		2*VBAT RCVR	Vpp	
		Single ended Output Driver used @ 1 kHz	0		VBATRC VR	Vpp	
Output Impedance	RCVR_Rout	Load between 1 mA and 30 mA		3	4	Ω	
Maximum Current	RCVR_IMax				90	mA	
Total Harmonic Distortion + Noise (Peak value)	RCVR_THDN		−70	−71		dB	
Dynamic Range	RCVR_DR		−85	−86		dB	
NoiseFloor	RCVR_NF				73	μV	

Table 2. ELECTRICAL CHARACTERISTICS (continued) (The typical parameters in Table 2 were measured at 20°C with a clean 3.3 V supply voltage (unless noted differently). Parameters marked as screened are tested on each chip. Other parameters are qualified for all process corners but not tested on every part.)

Parameter	Symbol	Test Conditions / Notes	Min	Typ	Max	Unit	Screened
LOW−SPEED A/D							
Input voltage	LSAD_Vin		0		1	V	
Sampling frequency	LSAD_SF	For each LSAD channel, MCLK = 1.28 MHz	0.5	1.6	4	kHz	
Input impedance	LSAD_RIN		100		108	kΩ	
Offset error	LSAD_O_Err	Input at VREG	−7		5	LSB	
Gain error	LSAD_G_Err	Input at VREG	−6		6	LSB	
INL	LSAD_INL		−4		4	LSB	
DNL	LSAD_DNL		−1		1.6	LSB	
DIGITAL PADS (VDDO = 1.8 V)							
Voltage level for Low input	VIL_1V8		−0.3		0.4	V	
Voltage level for High input	VIH_1V8		1.3		1.98	V	
Pull−up resistance	Rup_1V8		63	114	162	kΩ	
Pull−down resistance	Rdn_1V8		87	153	215	kΩ	
Rise and Fall Time	Trf_1V8	20 pF load	2	3	5	ns	
DIGITAL PADS (VDDO = 3.3 V)							
Voltage level for Low input	VIL_3V3		−0.3		0.8	V	
Voltage level for High input	VIH_3V3		1.8		3.6	V	
Pull−up resistance	Rup_3V3		33	46	61	kΩ	
Pull−down resistance	Rdn_3V3		87	153	215	kΩ	
Rise and Fall Time	Trf_3V3	20 pF load	1	1.5	2	ns	
DIGITAL PADS (Common parameters)							
Drive Strength	PAD_DR			12		mA	
ESD	PAD_HBM	Human Body Model	2			kV	
	PAD_MM	Machine Model	200			V	
	PAD_CDM	Charge Discharge Model	500			V	
Latch−up	PAD_LU	25°C, V < GNDO, V > VDDO	100			mA	
CLOCKING CIRCUITRY							
External clock frequency	EXT_CLK1	With presets 6 selected on CONFIG_SEL (Note 2)		19.2		MHz	
	EXT_CLK2	With presets 4 or 7 selected on CONFIG_SEL (Note 2)		26		MHz	
Reference clock duty cycle	EXT_CLK_DC		40	50	60	%	
External Input clock jitter	EXT_CLK_JT	Maximum allowed jitter on EXT_CLK			10	ns	
I^2C INTERFACE							
Maximum speed	I2C_SPEED	In Sleep mode			100	kbps	
		All other modes			400	kbps	

2. Many other clock frequencies are available through custom configuration of the internal PLL and clocking subsystem. See later in this document and in the BelaSigna R261 Configuration and Communications Guide for more information on custom mode usage.

Table 3. PIN CONNECTIONS

Pin Index	Pin Name	Description	A/D/P	I/O	Active	Pull
G1	MIC0	First microphone input	A	I		
E5*	AI1/LOUT1	Direct audio input / line−out preamp 1	A	I/O		
E1	MIC2	Second microphone input	A	I		
E3	AI3/VMIC/LOUT0	Direct audio input / microphone bias / line−out preamp 0	A	I/O		
D6*	A_OUT0	Audio output 0	A	O		
E7	A_OUT1	Audio output 1	A	O		
G7	CAP0	Charge pump capacitor connection	A	I/O		
F8	CAP1	Charge pump capacitor connection	A	I/O		
A1	DEBUG_RX	RS232 debug port serial input	D	I	L	U
B2	DEBUG_TX	RS232 debug port serial output	D	O	L	
F2	RESERVED	connect to VSSA				
A3	EXT_CLK	External clock input	D	I		U
A7	SPI_CLK/CONFIG_SEL	SPI clock / Configuration selection	D/A	O/I		
A9	SPI_CS/ATT_SEL	SPI chip select / Attenuation selection	D/A	O/I		
B8	SPI_SERO/ALGO_CTRL	SPI serial output / Algorithm control	D/D	O/I		−/U
C9	SPI_SERI/SLEEP_CTRL	SPI serial input / Sleep mode control	D	I/I		U/U
C7	DMIC_OUT	Digital microphone output	D	O		
C5*	BOOT_SEL	Boot selector	D	I		U
C3	I2C_SDA	I^2C data	D	I/O		U
C1	I2C_SCL	I^2C clock	D	I/O		U
D4*	NRESET	Reset	D	I	L	U
F6	VBAT	Power supply	P	I		
G9	VBATRCVR	Output driver power supply	P	I		
G5	VDDA	Analog supply voltage	P	O		
B6	VDDD	Digital power supply	P	O		
B4	VDDO	Digital I/O power supply	P	I		
G3	VREG	Analog supply voltage	P	O		
F4	VSSA	Analog ground	P	I		
A5	VSSD	Digital ground	P	I		
E9	VSSRCVR	Output driver ground	P	I		

* Pins C5, D4, D6 and E5 are not available on the WLCSP26 package.
All pins are available on the WLCSP30 package.

Application Diagrams

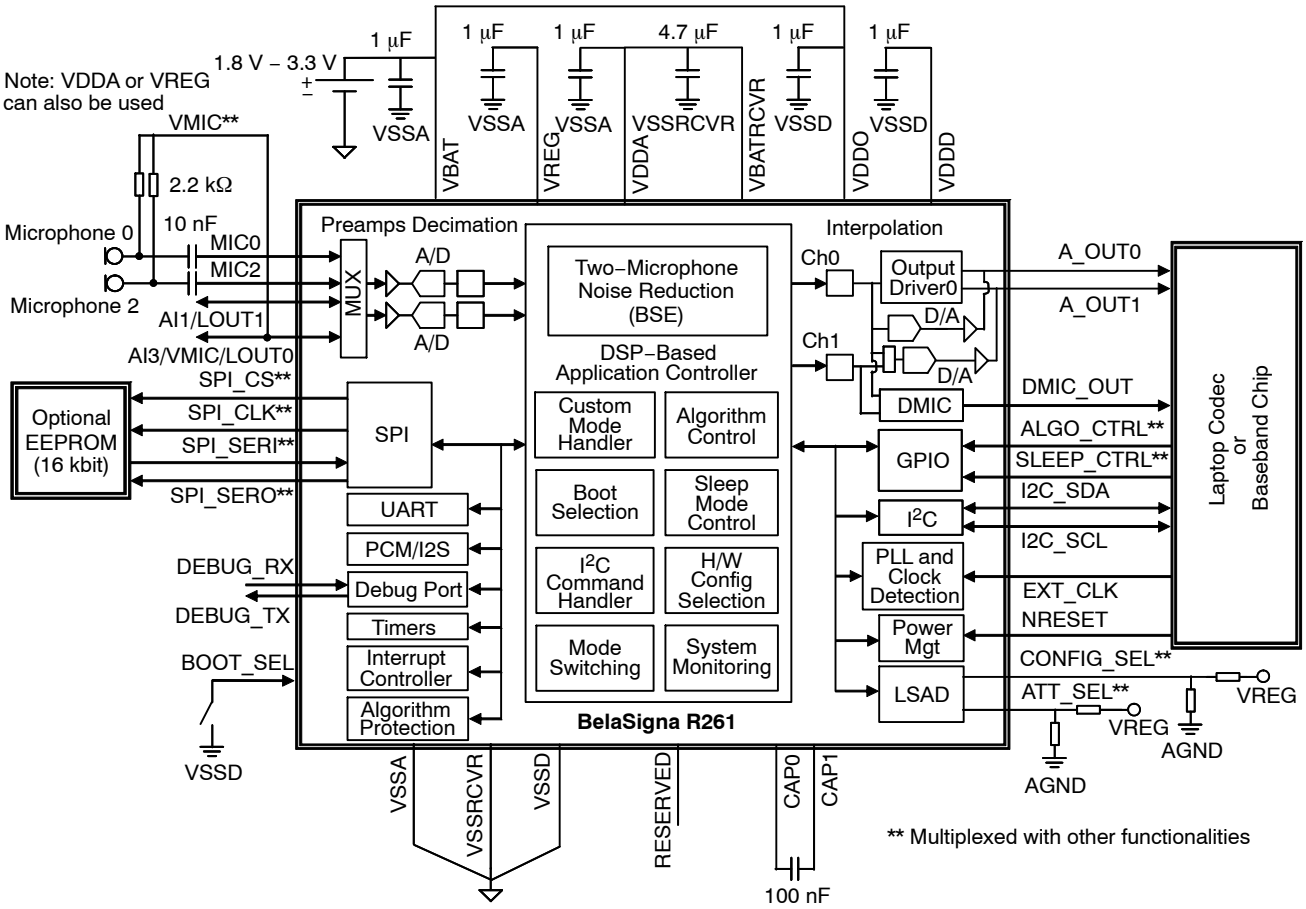


Figure 1. Typical Application Diagram for 30−ball WLCSP Package Option

Application Diagrams

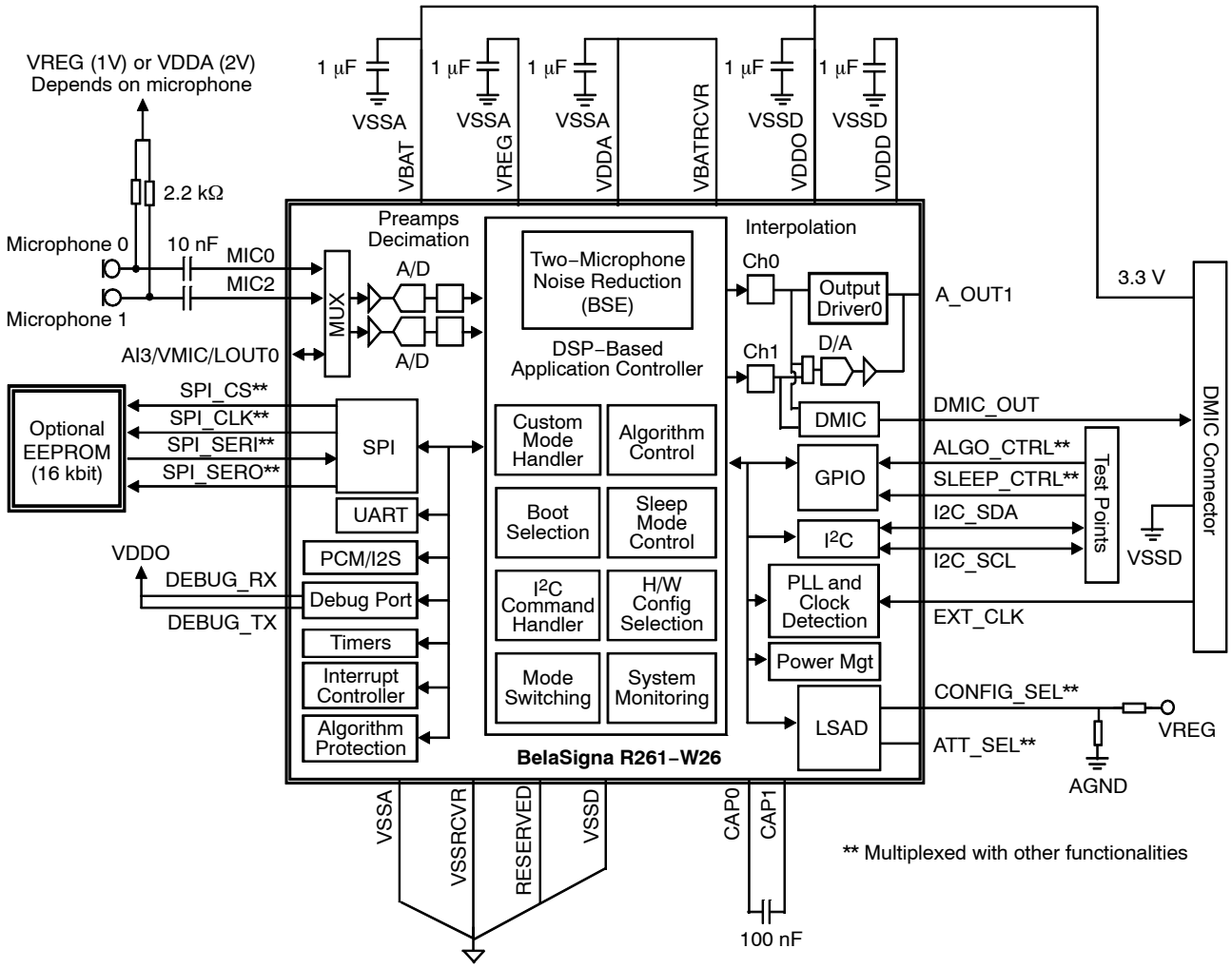


Figure 2. Typical Application Diagram for 26−ball WLCSP Package Option

Applications Information

Recommended Circuit Design Guidelines

BelaSigna R261 is designed to allow both digital and analog processing in a single system. Due to the mixed−signal nature of this system, careful design of the printed circuit board (PCB) layout is critical to maintain the high audio fidelity of BelaSigna R261. To avoid coupling noise into the audio signal path, keep the digital traces away from the analog traces. To avoid electrical feedback coupling, isolate the input traces from the output traces.

Recommended Ground Design Strategy

The ground plane should be partitioned into two parts: the analog ground plane (VSSA) and the digital ground plane (VSSD). These two planes should be connected together at a single point, known as the star point. The star point should be located at the ground terminal of a capacitor on the output of the power regulator as illustrated in Figure 3.

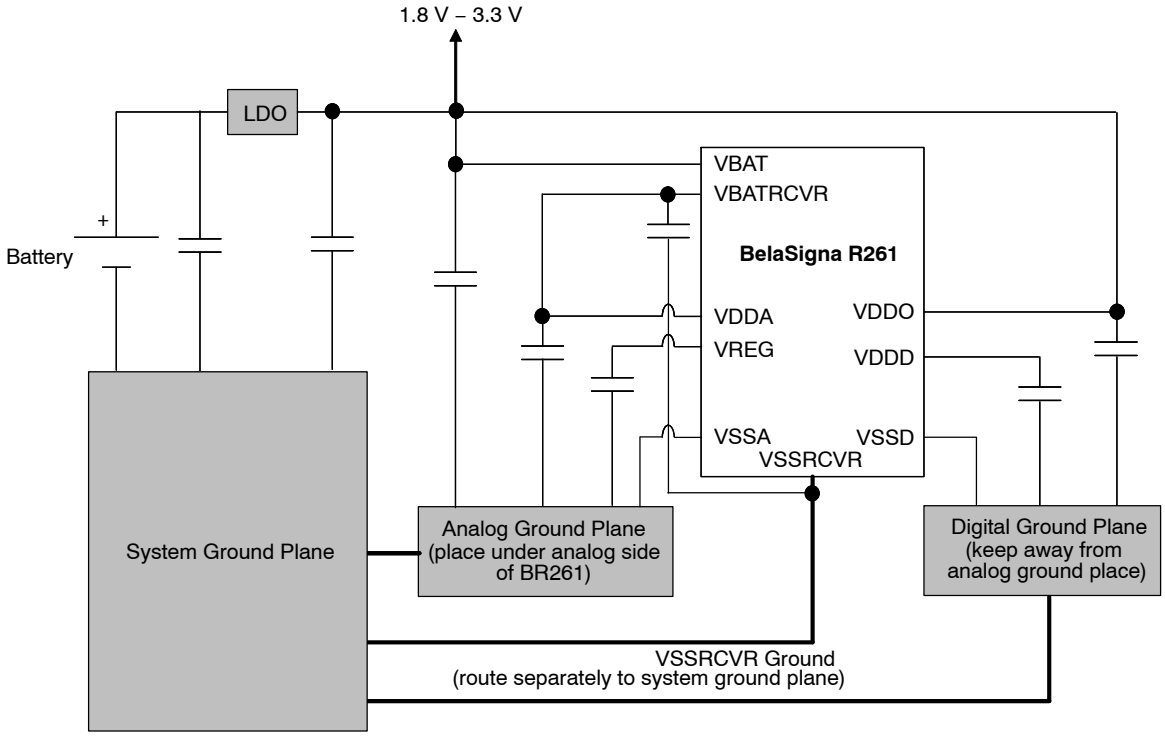


Figure 3. Schematic of Ground Scheme

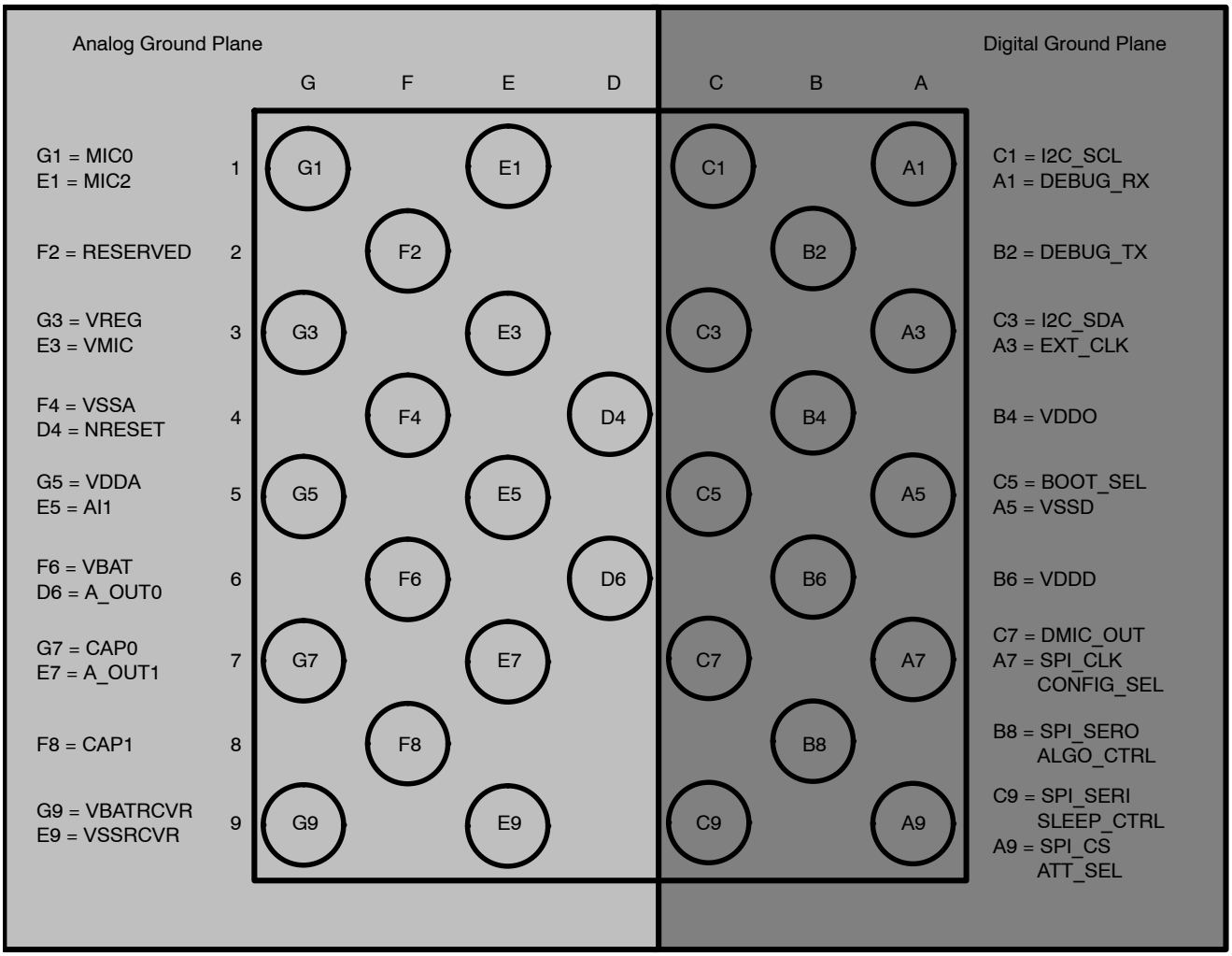


Figure 4. Analog Portion of BelaSigna R261 (Bumps facing up)

The VSSD plane is used as the ground return for digital circuits and should be placed under digital circuits. The VSSA plane should be kept as noise−free as possible. It is used as the ground return for analog circuits and it should surround analog components and pins. It should not be connected to or placed under any noisy circuits such as RF chips, switching supplies or digital pads of BelaSigna R261 itself. Analog ground returns associated with the audio output stage should connect back to the star point on separate individual traces.

For details on which signals require special design consideration, see Table 4 and Table 5.

In some designs, space constraints may make separate ground planes impractical. In this case a star configuration strategy should be used. Each analog ground return should connect to the star point with separate traces.

Internal Power Supplies

Power management circuitry in BelaSigna R261 generates separate digital (VDDD) and analog (VREG, VDDA) regulated supplies. Each supply requires an external decoupling capacitor, even if the supply is not used externally. Decoupling capacitors should be placed as close as possible to the power pads.

The digital I/O levels are defined by a separate power supply pin on BelaSigna R261 (VDDO). This pin must be externally connected by the application PCB, usually to VBAT. Note that the voltage on VDDO will influence the behavior of the LSAD dividers. The system is designed with the assumption that a 3.3 V power supply voltage is provided on VBAT, and that VDDO connects to VBAT on the application PCB.

Further details on these critical signals are provided in Table 4. Non−critical signals are outlined in Table 5. More information on the power supply architecture can be found in the Power Supply Unit section.

Table 4. CRITICAL SIGNALS

Pin Name	Description	Connection Guidelines
VBAT	Power supply	Place 1 μF (min) decoupling capacitor close to pin Connect negative terminal of capacitor to analog ground plane
VREG, VDDA	Internal regulator for analog blocks	Place separate 1 μF decoupling capacitors close to each pin Connect negative capacitor terminal to analog ground plane Keep away from digital traces and output traces VREG and VDDA may be used to generate microphone bias
VSSA	Analog ground return	Connect to analog ground plane
VDDD	Internal regulator for digital core	Place 1 μF decoupling capacitor close to pin Connect negative terminal of capacitor to VSSD
VSSD	Digital ground return	Connect to digital ground plane
VDDO	Digital I/O power	Place 1 μF decoupling capacitor close to pin Connect to VBAT, unless the pad ring must use different voltage levels
MIC0, MIC2, AI1/LOUT1, AI3/VMIC/LOUT0	Audio inputs / Microphone bias	Keep traces as short as possible Keep away from all digital traces and audio outputs Avoid routing in parallel with other traces
A_OUT0, A_OUT1	Audio outputs	Keep away from audio inputs Differential traces should be of approximately the same length Ideally, route lines parallel to each other
VSSRCVR	Output stage ground return	Connect to star ground point Keep away from all analog audio inputs
EXT_CLK	External clock input	Minimize trace length Keep away from analog signals If possible, surround with digital ground
DMIC_OUT	Digital Microphone Output	Minimize trace length Keep away from analog signals If possible, surround with digital ground

Table 5. NON−CRITICAL SIGNALS

Pin Name	Description	Connection Guidelines
CAP0, CAP1	Internal charge pump − capacitor connection	Place 100 nF capacitor very close to pins
I2C_SDA, I2C_SCL	I^2C port	Keep as short as possible. Place pull−up resistors (10 k) to VDDO
ALGO_CTRL, SLEEP_CTRL	Control GPIOs (Multiplexed with SPI port)	Not critical when used as GPIO
CONFIG_SEL, ATT_SEL	Low−speed A/D converters (Multiplexed with SPI port)	Not critical when used as LSAD
BOOT_SEL	Control GPIO	Not critical
SPI_CLK, SPI_CS, SPI_SERO, SPI_SERI	Serial peripheral interface port (Multiplexed with LSAD and GPIOs)	Keep away from analog input lines when used as SPI signals
NRESET	Reset	Not critical Leave unconnected if unused
DEBUG_RX, DEBUG_TX	Debug Port	Not critical If possible, connect to test points
RESERVED	Reserved pin	Leave unconnected
VBATRCVR	Output driver power supply	If the output driver is being used: − Place a separate 4.7 μF (min. 2.2 μF) decoupling capacitor close to pin − Connect positive terminal of capacitor to VBAT & VBATRCVR − Connect negative terminal of capacitor to VSSRCVR If the analog outputs or the DMIC output are being used: − Decoupling capacitor is not required − Connect VBATRCVR to VDDA

Audio Inputs

The audio input traces should be as short as possible. The input impedance of each audio input pad (e.g., MIC0, AI1, MIC2, AI3) is high (approximately 500 kΩ with PAs enabled); therefore a 10 nF capacitor is sufficient to decouple the DC bias. This capacitor and the internal resistance form a first−order analog high pass filter whose cut−off frequency can be calculated by f_{3dB} (Hz) = 1/(R x C x 2π), which results in ~30 Hz for a 10 nF capacitor. This 10 nF capacitor value applies when the preamplifier is being used, in other words, when a non−unity gain is applied to the signals; for MIC0 and MIC2, the preamplifier is enabled by the ROM−based application. When the preamplifier is by−passed, the impedance is reduced; hence, the cut−off frequency of the resulting high−pass filter could be too high. In such a case, the use of a 30−40 nF serial capacitor is recommended. In cases where line−level analog inputs without DC bias are used, the capacitor may be omitted for transparent bass response. ON Semiconductor recommends avoiding SMT capacitors with X7R dielectric, as it is known to be microphonic, sensitive to temperature and increase THD. NPO or COG dielectric capacitors have demonstrated good performance.

BelaSigna R261 provides a microphone power supply (VMIC) and ground (VSSA). In case VMIC cannot be used for PCB routing issues, the power supplies VREG (1.0 V) or VDDA (2.0 V) can alternatively be used. Keep audio input traces strictly away from output traces.

Audio outputs must be kept away from microphone inputs to avoid cross−coupling.

Audio Outputs

The audio output traces should be as short as possible. The trace length of the two signals should be approximately the same to provide matched impedances.

Recommendation for Unused Pins

Table 6 shows the connection details for each pin when they are not used.

Table 6. UNUSED PIN RECOMMENDATIONS

Signal Name	Connection Guidelines
A_OUT0	Do not connect
A_OUT1	Do not connect
AI3/VMIC/LOUT0	Do not connect when configured as VMIC (default) Connect to VSSA otherwise
AI1/LOUT1	Connect to VSSA
DMIC_OUT	Do not connect
SPI_SERO/ALGO_CTRL	Do not connect
SPI_SERI/SLEEP_CTRL	Do not connect
NRESET	Do not connect

Architecture Detailed Information

The architecture of BelaSigna R261 is shown in Figure 5.

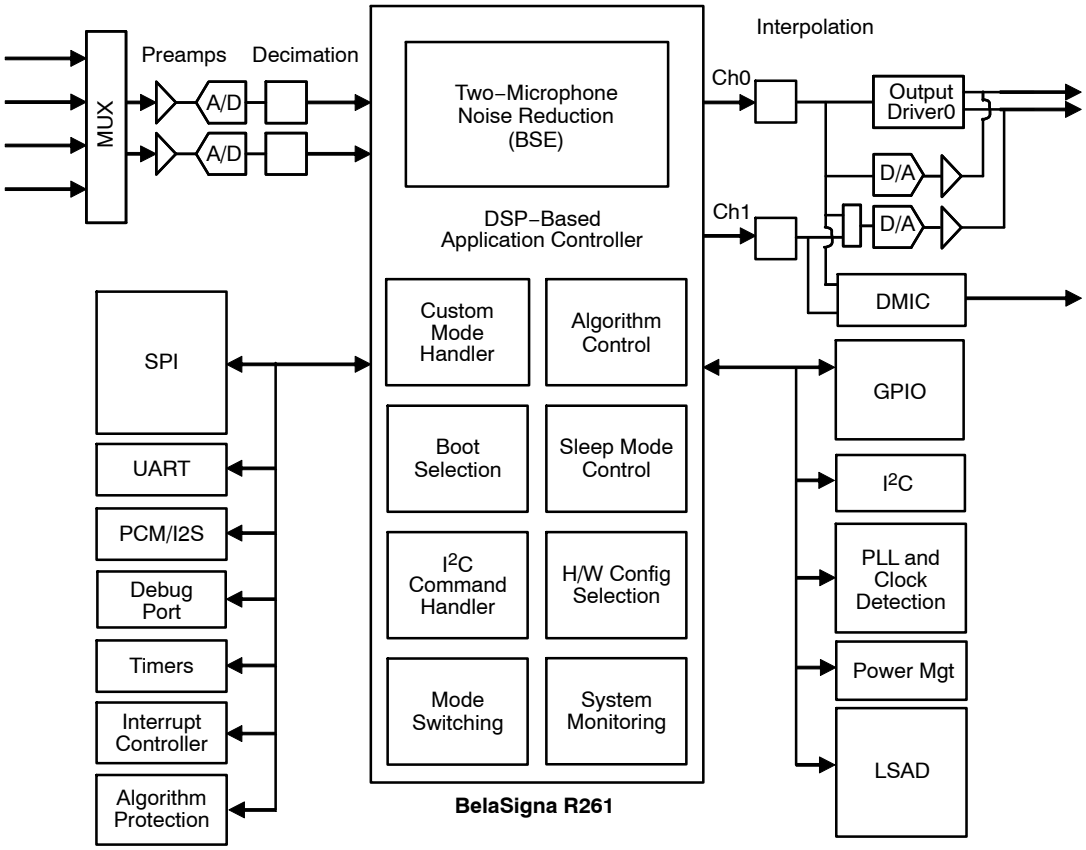


Figure 5. BelaSigna R261 Architecture: A Complete Audio Processing System

Two−Microphone Noise Reduction System

Blind Speech Extraction (BSE) from Exaudio AB

BelaSigna R261 contains the BSE algorithm inside its ROM memory. Exaudio offers a unique solution to the problem of blindly extracting wave propagating signals using one or more sensors without having any prior knowledge about source's or sensor's positions. The solution operates simultaneously in the frequency, temporal and the spatial domain using one global optimization criterion, with no constraints on the number of sources vs. the number of sensors. The solution is Signal−to−Noise Ratio (SNR) independent, meaning that it operates optimally in both low SNR as in high SNR environments and at the same time it performs de−reverberation of the received signals. The solution is ideal for electronic communication devices such as mobile phones and portable computers where it is desired to extract useful speech signals hidden in various noise fields. The flexibility offered by Exaudio's solution allows for flexible microphone positioning and arbitrary placement of the self adaptive device in the actual environment.

Algorithm Modes

The noise reduction algorithm built into BelaSigna R261 has two algorithm modes called Algorithm Mode 0 and Algorithm Mode 1. Algorithm Mode 0 is optimized for far−talk applications where the end user can be very far from the microphones (up to 6 meters) such as laptops or speakerphones (including cell phones in a speakerphone mode). This algorithm mode is also known as "Conference Mode". Algorithm Mode 1 is optimized for close−talk applications where the end user is close to the microphones (< 5 cm) such as telephony handset (including cell phones in a handset mode).

A Custom Algorithm Mode is also available in BelaSigna R261; it allows supporting special configurations and tuning by loading new algorithm parameters via an external EEPROM or the I^2C control interface. The algorithm performance can be optimized for specific applications, microphones types and positioning as well as other system parameters via this mechanism.

For additional details on the custom mode handler and algorithm performance tuning options, please refer to "BelaSigna R261 Configuration & Communications Guide."

Microphone Placement & Selection

The flexibility of the BelaSigna R261 ROM−based noise reduction algorithm offers a variety of possible microphone placements, but the default algorithm will operate optimally when the microphones are placed in the following configuration:

- The two microphones are facing the user's mouth
- The microphone centers are located within 10 to 25 mm from each other

As mentioned, other configurations that differ from the above guidelines can be supported through the use of the custom mode, as described earlier.

BelaSigna R261 does not require any acoustic microphone calibration procedure.

The selection of the microphones should be made in cooperation with ON Semiconductor, such as the built−in algorithm can operate seamlessly. The following guidelines can be used for a pre−selection:

- Two omni−directional microphones with similar characteristics should be used
- The microphone sensitivity should be −42 dB (where 0 dB = 1 V/Pa, at 1 kHz)
- The microphones are two terminal microphones
- The microphone power supply is either 1 V, or 2 V if it has to be provided by BelaSigna R261
- The dynamic range of BelaSigna R261 on its analog input channels is 2.0 V peak−to−peak, after amplification by the default gain value of 30 dB using BelaSigna R261's input preamplifiers
- When higher sensitivity microphones have to be used, the preamp gain will be adjustable to match the 2.0 Vpp input voltage swing on BelaSigna R261, but this will require a custom tuning operation, as described later.

Operating Modes

The default application in ROM on BelaSigna R261 has five Operating Modes. The Operating Modes are summarized in Table 7.

Table 7. OPERATING MODES SUMMARY

Operating Mode	Switching	Description
Active	Active mode is the default operating mode. The chip normally enters Active mode upon boot−up and when exiting Sleep mode. Active mode can also be entered via I^2C from another mode.	In Active mode, the two−microphone noise reduction algorithm is executed on the audio inputs and both the processed and unprocessed signals are sent to the audio outputs.
Bypass	Bypass mode can only be entered via an I^2C command.	In Bypass mode, no signal processing is done on the audio inputs. The inputs are passed directly to the audio outputs. While in Bypass mode, BelaSigna R261 collects statistics on the input signals that can be retrieved via I^2C. These signal statistics can be used for level calibration and other debugging. For more information using Bypass mode for calibration and debugging see the "BelaSigna R261 Configuration and Communications Guide"
Line−Out	Line−Out mode can only be entered via an I^2C command.	In Line−Out mode, no signal processing or digital processing of the audio inputs is done. The analog signals from the input stage preamplifiers are routed back via the lineout pins (LOUT0 and LOUT1). When in this mode, BelaSigna R261 runs off an internal clock source, thereby allowing the external clock to be disabled. Note that LOUT1 is not available on the 26−ball WLCSP package.
Sleep	Sleep mode can be entered via I^2C commands or by using the SLEEP_CTRL pin. When Sleep mode is entered via I^2C, the chip will exit Sleep mode only based on activity on the I2C_SCL pin. When put to Sleep mode via the SLEEP_CTRL pin, the chip will exit Sleep mode only when the SLEEP_CTRL pin is toggled again. Sleep mode will be automatically entered if BelaSigna R261 detects that a required external clock is no longer present. For more information, see the Sleep Control section below.	In Sleep mode no signal processing is done. All analog blocks of the chip are disabled and the digital core continues to run off an internal low−speed oscillator, thereby allowing the external clock to be disabled when the chip is asleep. This is BelaSigna R261's lowest power operating mode.
Stand−By	Stand−By mode is an intermediate mode that is only used when exiting sleep mode by an I^2C command.	When I^2C is used to exit Sleep mode, the application will transition to Stand−By mode, and will wait until the master I^2C device issues a *Switch_Mode* command to enter another processing mode like Active, Bypass or Line−Out.

Digital Control, Hardware Configuration and Interfaces

Boot Control

At power−on−reset, BelaSigna R261 will normally execute the application stored in ROM with the default hardware and algorithm configuration. Additional built−in hardware and algorithm configuration options are available as described later in this section by using the CONFIG_SEL and ATT_SEL pins. These settings are selected at boot−time based on the pin voltage levels.

The BOOT_SEL pin controls the booting method of BelaSigna R261. There are in fact two alternate methods to boot a custom application or hardware/algorithm configuration. These methods, along with the default boot method, are described in Table 9. Note that the BOOT_SEL pin is not available on the WLCSP−26 package option, consequently, this signal is left floating and the automatic boot selection described below applies for all applications using this reduced ball package variant.

Table 8. BOOT CONTROL OPTIONS

Boot Method	Condition	Description
EEPROM Boot (Automatic boot selection)	BOOT_SEL high (or floating/not available on package)	Enables SPI interface and attempts to boot from external EEPROM. EEPROM may contain a custom application or configuration. If no EEPROM, or bad content, loads the default application in ROM with hardware and algorithm configuration determined by CONFIG_SEL and ATT_SEL pins. See the “BelaSigna R261 Configuration and Communications Guide” for more information.
LSAD Boot	BOOT_SEL low	Loads default application in ROM. Hardware and algorithm configuration determined by CONFIG_SEL and ATT_SEL pins.
I^2C Boot	Connect to BelaSigna R261 via I^2C after default boot−up	The I^2C control interface can be used to download a custom application, or to re−configure the default application. See the “BelaSigna R261 Configuration and Communications Guide” for more information.

When the automatic boot selection process is being used, either when selecting the 26−ball package version, or simply when leaving the BOOT_SEL pin unconnected on the application PCB, it is very important to ensure that the SPI pins will not be driven by any external hardware component. Typically, a custom application may want to use the PCM interface, which is also multiplexed with the SPI port. Extreme care must be taken in such use cases, to ensure that the SPI ports remain at high impedance during the boot process. Contact your local technical support for more information on this particular use case.

Reset

BelaSigna R261 can be forced to execute a power−on−reset by pulling the NRESET pin to ground for at least 100 ns. Note: NRESET is not available on the 26−ball WLCSP package.

Algorithm Control

BelaSigna R261 has provisions to control whether the noise reduction algorithm processed signal is output, or an unprocessed signal is output. This effectively enables or disables the algorithm. The algorithm can be controlled via the I^2C interface or by use of the ALGO_CTRL pin. When using the ALGO_CTRL pin, the algorithm state is toggled whenever the digital signal transitions to low and stays low for at least 10 ms, as shown in Figure 6. The actual transition between algorithm enable/disable states can occur at any time during the 10 ms low period of the signal.

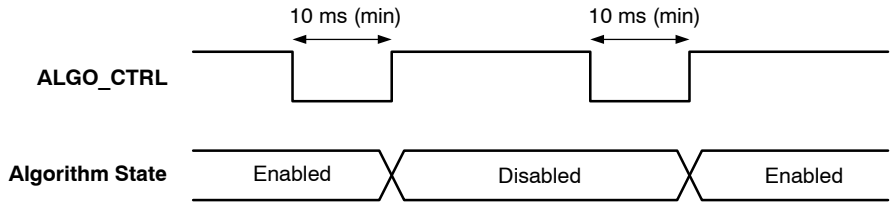


Figure 6. ALGO_CTRL Timing Diagram

BelaSigna R261 has two processing channels (Channel 0 and Channel 1), when the noise reduction algorithm is enabled, Channel 0 contains the processed signal and Channel 1 contains the unprocessed signal. The effect of toggling the algorithm state is to swap Channel 0 and Channel 1, i.e. disabling the algorithm causes Channel 0 to contain the unprocessed signal and Channel 1 to contain the processed signal. These two output channels represent the internal DSP output signals with BelaSigna R261. The DMIC and analog audio outputs can each be configured to use either channel. See the Output stage section to see how Channel 0 and Channel 1 are used by the various configuration options of BelaSigna R261’s output stage.

Sleep Control

As described in the modes of operation, there are multiple methods to enter and exit from Sleep mode. Each of these methods is meant to be used independently, i.e. methods of

putting the system into Sleep mode and waking it up from Sleep mode cannot be mixed in the same system design.

The first Sleep mode control mechanism is the SLEEP_CTRL pin. When using SLEEP_CTRL, the application will transition into or out of Sleep mode whenever the digital signal transitions to low and stays low for at least 20 ms, as shown in Figure 7. The actual transition between modes can occur at any time during the 20 ms low period of the signal. When SLEEP_CTRL is used to put the chip into Sleep mode, only another high−to−low transition on SLEEP_CTRL or a reset will take the system out of Sleep mode.

The operating mode after exiting Sleep mode using the SLEEP_CTRL mechanism is always the same as it was before entering Sleep mode (Active mode in the case of Figure 7).

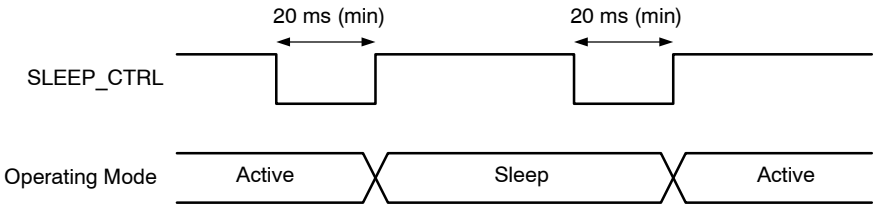


Figure 7. SLEEP_CTRL Timing Example

The second method for Sleep mode control is via the I^2C interface. The *Switch_Mode* command can be used directly to switch the system into and out of Sleep mode. If the *Switch_Mode* command is used to put the chip into Sleep mode, only another *Switch_Mode* command or a reset will take the system out of Sleep mode. When waking−up by I^2C commands, the following I^2C operations have to be performed by the master I^2C to ensure proper wake−up:

1. Send a *NOP* command to wake up the I^2C interface. This command will not be interpreted by BelaSigna R261, so the master will have to deal with any I^2C errors that result.
2. Send the *Get_Status* command in a while−type loop, until a response from BelaSigna R261 is sent, and that confirms that the application is in Standby Mode.
3. Send a *Switch_Mode* command to enter the desired mode (Active, Bypass or Line−Out).

When the *NOP* command is sent and the chip wakes up, the master has about one second to complete the above procedure before the chip goes back to Sleep mode. This mechanism was put in place to deal with I^2C bus traffic that would wake the chip up unintentionally (i.e. communications between the master and another slave on the I^2C bus).

The final mechanisms for entering Sleep mode are considered fail safes to maintain a graceful system shutdown in the case of invalid operating conditions which could be that the clock source suddenly stopped. Under this circumstance, the chip will enter sleep mode to ensure proper shutdown. More information on this can be found in the system monitoring section.

The SLEEP_CTRL pin must not be used when the automatic boot selection method is being used, as described in Table 9, as BelaSigna R261 will start by searching for an SPI EEPROM on the multiplexed pins. Consequently, the SLEEP_CTRL pin must stay unconnected in this mode. Other mechanisms for controlling sleep mode have to be used in such cases. This limitation is always there with the 26−ball WLCSP package of BelaSigna R261, since the BOOT_SEL pin is not available, and hence is always floating.

Clocking, Output Stage & Algorithm Configuration

As mentioned in the Boot Control section, BelaSigna R261 can be controlled by hardware configuration when no EEPROM is present on the application, or when the BOOT_SEL signal was tied low. The CONFIG_SEL signal is sampled by BelaSigna R261 during its booting process using a low−speed A/D converter (LSAD). Based on the actual voltage that the chip will read on this pin, it will automatically select a particular clock, output stage and algorithm configuration, as described in Table 9:

Table 9. CLOCKING, OUTPUT STAGE AND ALGORITHM CONFIGURATION OPTIONS

Clock, Output Stage & Algorithm Configuration		Voltage Range (V)							
		0 (High)	**1**	**2**	**3**	**4**	**5**	**6**	**7 (Low)**
		0.93–1.00	**0.79–0.91**	**0.65–0.77**	**0.50–0.63**	**0.36–0.49**	**0.22–0.35**	**0.08–0.21**	**0 – 0.07**
External Clock Frequency (MHz)	2.048	X					X		
	2.4		X						
	3.072			X					
	2.8				X				
	19.2							X	
	26					X			X
Output Stage Configuration	DMIC Stereo	X	X	X	X		X		
	Analog Mono	X	X	X	X	X	X	X	X
Algorithm Mode		Mode0	Mode0	Mode0	Mode0	Mode0	Mode1	Mode1	Mode1
		Far−Talk					Close−Talk		

The use of a resistive divider, as shown in Figure 8, allows the application schematic to select the appropriate combination of clock, output stage and algorithm mode. The LSAD is using a voltage range between 0 and 1 V. The actual voltage levels that need to be guaranteed by the application schematic are also mentioned in Figure 8. The figure proposes actual resistor values to reach the eight different presets.

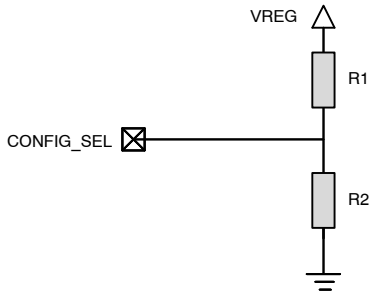


Figure 8. Resistive Dividers for LSAD Preset Selection

Preset	R1	R2	Voltage Range
0	10 kΩ	–	0.93 – 1.00 V
1	16 kΩ	100 kΩ	0.79 – 0.91 V
2	39 kΩ	100 kΩ	0.65 – 0.77 V
3	75 kΩ	100 kΩ	0.50 – 0.63 V
4	100 kΩ	75 kΩ	0.36 – 0.49 V
5	100 kΩ	39 kΩ	0.22 – 0.35 V
6	100 kΩ	16 kΩ	0.08 – 0.21 V
7	–	10 kΩ	0 – 0.07 V

It is important to note that the configuration is only read by the chip at boot time, and consequently, it will not be dynamically updated. So if the voltage on the CONFIG_SEL is changing during operation, it will only have an impact at the next reboot operation.

Analog Output Attenuation Control

The hardware configuration method described above, using an LSAD and a resistive divider is also being used on another signal called ATT_SEL, such that the application schematic can select an analog output attenuation to be applied on the analog output signals. Typically, when interfacing BelaSigna R261 with a baseband chipset in a cell phone application, it is very often required to match the amplitude of the output signals to the input range requirements of the baseband processor. Table 10 describes the available values, and their corresponding preset. The resistive dividers described in Figure 8 can also be used to configure the ATT_SEL pin.

Table 10. OUTPUT ATTENUATION CONTROL OPTIONS

ATT_SEL: Analog Output Attenuation Select	Voltage Range							
	0 (High)	1	2	3	4	5	6	7 (Low)
	0.93–1.00	0.79–0.91	0.65–0.77	0.50–0.63	0.36–0.49	0.22–0.35	0.08–0.21	0 – 0.07
Output Attenuation (Ch0 & Ch1)	0 dB	12 dB	15 dB	18 dB	21 dB	24 dB	27 dB	30 dB

I²C Command Handler

The BelaSigna R261 ROM application contains an I²C based command and control interface, allowing many aspects of the chip's operation and hardware configuration to be controlled via I²C. This I²C interface is the recommended way to control the chip and to configure the application at run−time. The default I²C address of BelaSigna R261 is 0x61. The I²C interface protocol is fully supported by the SignaKlara Device Utility (SKDU).

For more information on the I²C interface, please refer to the I²C interface section of this document, and to the "BelaSigna R261 Configuration and Communications Guide."

System Monitoring

The application software within BelaSigna R261 is equipped with a few blocks that monitor system sanity. A watchdog timer is used to ensure proper execution of the signal processing application. It is always active and is periodically acknowledged as a check that the application is still running. Once the watchdog times out, a hardware system reset will occur. System sanity is also monitored by the clock detection mechanism; the chip will automatically enter Sleep mode if it is in Active or Bypass mode and detects that the external clock source (the signal on EXT_CLK) is stopped. In this case, the system will only exit Sleep mode when it detects that the external clock source has been restored or a reset occurs.

The power supply blocks of the system also monitor for minimum supply voltages as part of the power supervision strategy, as described in the Power Management section.

Analog Blocks

Input Stage

The BelaSigna R261 analog audio input stage is shown in Figure 9. The input stage is comprised of two individual channels. There are four configurable aspects of each channel – input multiplexing, preamplifier gain, filtering and lineout. The input multiplexing allows one input to be selected from any of the four possible input and then routed to the inputs of the preamplifier. Each preamplifier can be

configured for bypass or gain values of 12 to 30 dB in 3 dB steps. The filters can be configured as well; the DC removal high−pass filter can be bypassed, or set to a cut−off frequency of 5 Hz, 10 Hz or 20 Hz (default). The low−pass filter can be either enabled with a 20 kHz cut−off frequency (default), or bypassed. The lineout selection allows the preamplifier outputs to be routed back out via the auxiliary audio input pins. Note that the AI1/LOUT1 pin is not available on the WLCSP−26 package option.

Two oversampled 16−bit sigma−delta analog−to−digital converters then convert the analog signals into the digital domain. The ADCs are running at a sampling rate of 16 kHz in both Bypass and Active mode. The sampling rate can potentially be changed using the I^2C interface. Changing the sampling rate in Active mode will cause the noise cancellation algorithm to stop operating properly, so this should not be done; however, the sampling rate in Bypass mode could potentially be changed to other values. Contact your local technical support for more information.

Input signal amplitudes can also be adjusted in the digital domain; digital gain for both converted signals can be adjusted by using I^2C commands.

The ROM−based application pre−configures all these parameters in the input stage such that the algorithm operates properly. These parameters can be changed using the I^2C interface, but extreme care should be taken when doing so, as this could alter the performance of the algorithm.

The AI3 pin is multiplexed with the microphone power supply. The default mode for the microphone bias is to be used as a 2 V power supply. Consequently, any application that plans to use the AI3 input pin or the LOUT0 functionality has to change the VMIC settings to high-impedance mode, such as the pin can be properly used as an analog input or a line-out.

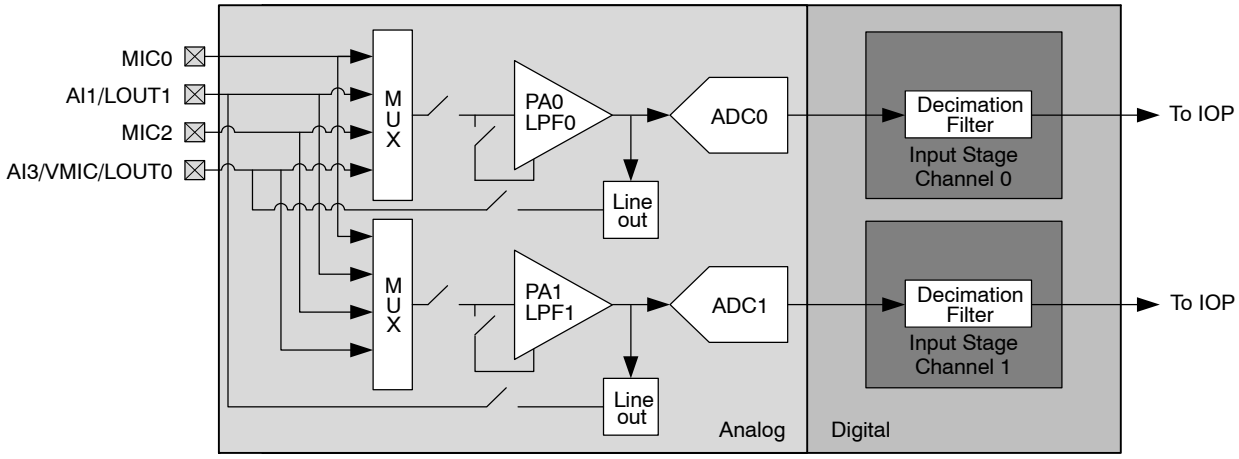


Figure 9. Input Stage

Output Stage

At all times, the application will produce two output channels. The content of each channel is determined by the state of the algorithm enable/disable bit, as explained in the Algorithm Control section. When the algorithm is enabled, Channel 0 will contain the processed signal and Channel 1 will contain the un−processed signal. Toggling the algorithm bit will swap these two channels. These two output channels will then be transmitted to the output stage hardware block.

Independently from the actual output stage that was selected, the amplitude of both the processed and the non−processed channels can be controlled by I^2C commands. A first parameter determines the number of output shifts (6 dB attenuation or amplification, depending on the sign) that will be applied to the channels. A second parameter is a finer mechanism that allows applying a fractional, broadband gain on the channels. With these two mechanisms, applied in the digital domain by the application processor, a great level of flexibility is provided to match the output level requirements of the target application, independently for the two output channels. The ROM−based application has initialized these parameters for proper operation of the algorithm and correct output levels, so extreme care should be taken when modifying these parameters.

The BelaSigna R261 output stage is shown in Figure 10. The output stage processes the two channels although, depending on the configuration, one or both of the output signals are available on the output pins. There are four options for audio outputs from BelaSigna R261 – a digital microphone (DMIC) interface, a low−impedance output driver, a stereo single−ended analog output or a mono differential analog output. All outputs are generated from a sigma−delta modulator which produces a pulse density modulated (PDM) output signal and then provides it to the appropriate output system, based on the system configuration.

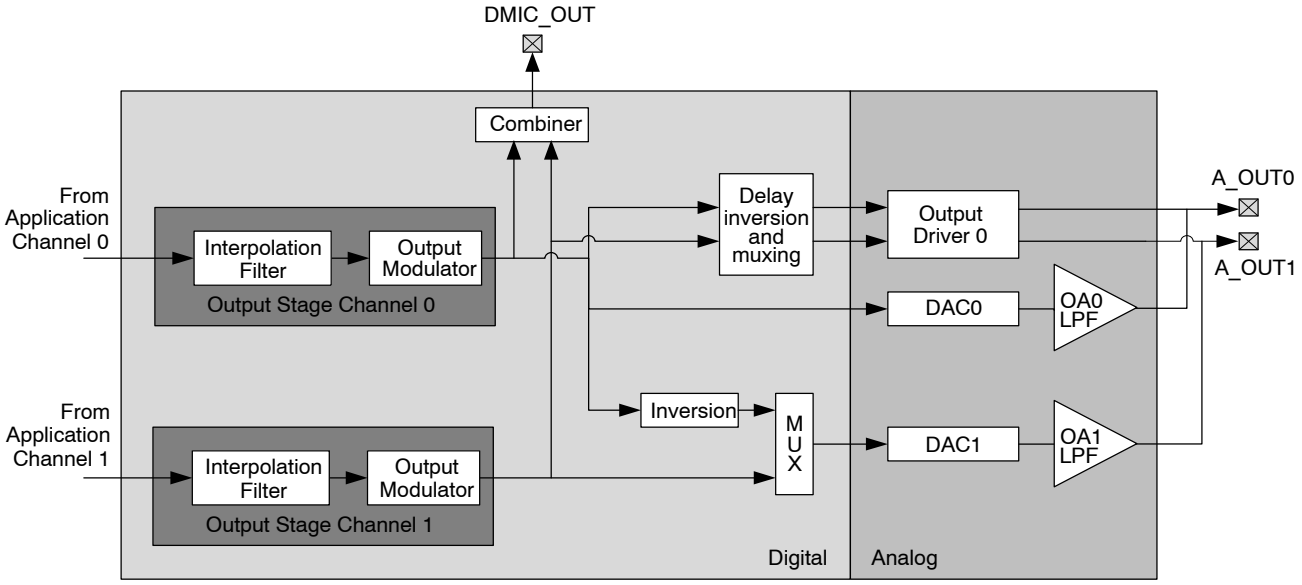


Figure 10. Output Stage

The digital microphone interface provides the PDM signals directly on a pin (DMIC_OUT), for interfacing with the DMIC input of external systems. When using this interface, the EXT_CLK input to BelaSigna R261 must be given a DMIC_CLK signal and the system's clocking must be set up properly, such as proper synchronization can happen between the incoming DMIC_CLK and the output data produced by BelaSigna R261 on its DMIC_OUT pin. Various DMIC_CLK frequencies are supported through hardware configuration on the CONFIG_SEL pin, as discussed earlier. Other frequencies could also be supported under certain conditions, see the clocking section of this document for more information on the supported DMIC clock frequencies.

The DMIC output can be configured to carry a mono or stereo signal. In fact both left and right signals can be configured to either contain output stage channel 0 or output stage channel 1. Also, both left and right can be configured to be muted independently (driving a '0' all the time).

Figure 11 shows the timing of the DMIC output data relative to the incoming DMIC_CLK signal. See Table 2 for electrical specifications of the timing parameters.

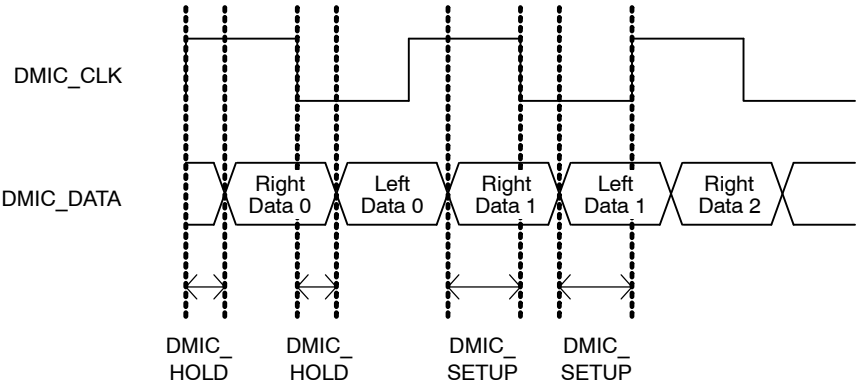


Figure 11. DMIC Timing Diagram

The ROM−based application pre−configures the DMIC interface, such as it always outputs a stereo signal with Channel 0 as the right signal, and Channel 1 as the left signal. Table 11 shows the actual signals on the right and left channels of the DMIC interface, depending on the algorithm enable/disable bit.

Table 11. DMIC OUTPUT SIGNALS

	Algorithm Enabled	Algorithm Disabled
Right	BSE processed signal	Un−processed signal
Left	Un−processed signal	BSE Processed signal

The DMIC host can consequently ignore the algorithm enable/disable functionality, as both processed and un−processed signals are always output for all pre−defined DMIC configurations. This functionality can still be used with custom DMIC configurations, such as mono. These custom configurations can be made over the I^2C interface.

When the DMIC interface is not required or needed, the analog outputs can be used for interfacing at line−levels or other signal levels, e.g. microphone levels for an external system which expects low level signals (e.g. an analog baseband chipset).

There are three configurable aspects of the analog output stage – the selection of stereo (two single ended outputs) or mono (one differential output), the output attenuation and the reconstruction filter. When a stereo single−ended option is selected, each channel is filtered to generate an analog signal which is then scaled by a configurable output attenuator (OA in Figure 10). In mono differential mode, channel 1 is replaced by an inverted version of channel 0 such that the two output pins contain a differential signal for channel 0. In this latter case, both output attenuators are used, so it is mandatory to ensure that they have the same attenuation settings. This can be configured using I^2C commands.

As defined with the CONFIG_SEL pin, some pre−defined configurations have been designed specifically for use with analog output instead of DMIC interface. For these configurations, a differential mono analog output is pre−configured by the ROM−based application. Consequently, the host processor will have to use the algorithm enable/disable pin (ALGO_CTRL) or the I^2C interface, to swap between the processed and the non−processed signal, as shown on Table 12:

Table 12.
ANALOG MONO DIFFERENTIAL OUTPUT SIGNAL

	Algorithm Enabled	Algorithm Disabled
A_OUT0 – A_OUT1	BSE processed signal	Un−processed signal

Alternatively, when stereo analog outputs have been configured through the I^2C interface, the signals on the two output pins will be as shown on Table 13:

Table 13. ANALOG STEREO OUTPUT SIGNALS

	Algorithm Enabled	Algorithm Disabled
A_OUT0	BSE processed signal	Un−processed signal
A_OUT1	Un−processed signal	BSE Processed signal

The attenuation of these analog signals can be done by using the ATT_SEL mechanism described earlier, but alternatively, the I^2C interface can also be used for this purpose.

The reconstruction filters can also be altered by I^2C commands; typically, the cut−off frequency can be switched between 13 kHz (default) and 26 kHz.

The WLCSP-26 package option doesn't provide access to the A_OUT0 pin. Consequently, only A_OUT1 is available as an analog output. For the predefined configurations (using CONFIG_SEL), the analog output stage is configured to provide a mono differential output signal, as described on Table 12. The A_OUT1 signal will thus be an inverted version of the processed output channel. Access to the un-processed signal will have to be done with an I^2C command, or potentially with the ALGO_CTRL signal, with the precautions discussed earlier concerning the automatic booting process (See the Boot Control section for additional details).

A third output method is available on BelaSigna R261, using the Class−D output driver which can drive an output transducer without the need for a separate power amplifier. The output driver can also be configured for single ended stereo or differential mono, through the same I^2C commands as described for the analog outputs.

For optimal audio performance it is important to note that the VBATRCVR power supply must be connected differently, depending on whether the output driver or the analog outputs are being used:

- When using the analog outputs, VBATRCVR must be connected to VDDA on the application PCB
- When using the output driver, VBATRCVR must be connected to VBAT on the application PCB and must be decoupled with an external capacitor

When interfacing BelaSigna R261 with other processors like codecs or baseband chipsets, it is not recommended to use the output driver, but rather the analog outputs.

Clock Generation Circuitry

BelaSigna R261 is equipped with a fully configurable and flexible clocking system, which allows for a large number of clocking configurations for various different use cases. Computing applications would typically require the use of a DMIC interface, which imposes constraints on the BelaSigna R261 clocking system, such as it provides full synchronization between an incoming DMIC clock and the DMIC data that the chip will produce. The input frequencies that these systems usually operate with are in the range of 2.048 to 3.072 MHz. Mobile phone applications would typically use much higher clock frequencies; historically, baseband systems have been using 13 MHz or 26 MHz, or even 19.2 MHz or 38.4 MHz.

The variety of clocking use cases that BelaSigna R261 must support forced the integration of a phase locked loop as one of the components of BelaSigna R261's clock generation circuitry. This highly configurable PLL is shown in Figure 12, in the context of the BelaSigna R261 clocking architecture.

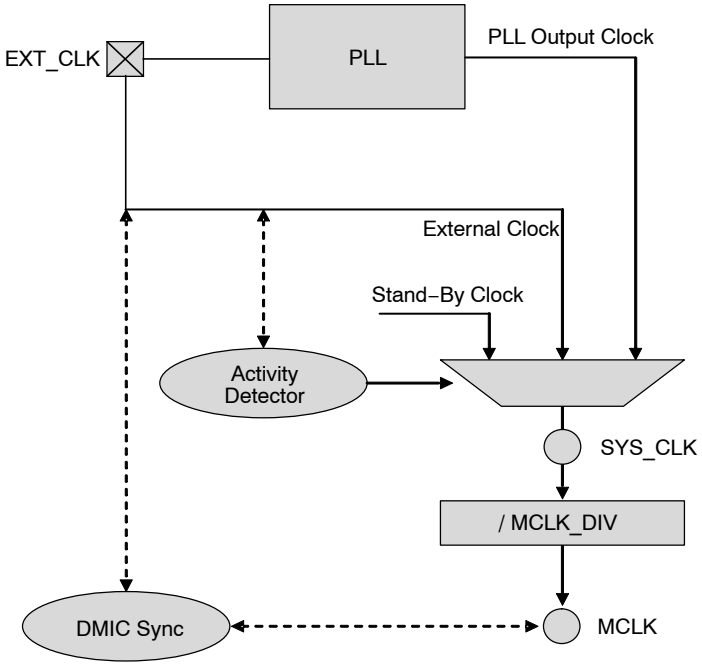


Figure 12. Clocking Circuitry

The ROM−based application has pre−configured the clocking system in the various hardware presets that are available, as described in Table 9, but for extended flexibility, the use of the I^2C interface allows changing the clocking configuration to accommodate specific application needs. See BelaSigna R261 Configuration and Communications Guide for more information.

SYS_CLK is the clock signal that will be used by the digital signal processing engine inside BelaSigna R261. It can be either the output of the PLL, as described above or it can also be driven by the stand−by clock, which is a very low frequency signal used to minimize power consumption in Sleep mode. Alternatively, the EXT_CLK signal could also be used directly by the system, bypassing the internal PLL.

MCLK is the clock signal that is used by the input and output stages of BelaSigna R261. MCLK must be configured to stay within the 1.92 MHz – 3.84 MHz range, to guarantee correct system operation. Among other parameters, an important impact of the MCLK signal is the sampling rate.

When the DMIC interface has to be used, BelaSigna R261 automatically synchronizes the EXT_CLK signal and the MCLK signal, as shown on Figure 12. Since MCLK is used to generate the DMIC data output, it must be fully synchronized with the EXT_CLK signal which is the DMIC clock, such as the DMIC host can properly sample the DMIC data. Consequently, the range of supported DMIC clock frequencies is the same as the MCLK range, i.e. 1.92 MHz to 3.84 MHz.

As discussed in the System Monitoring section, BelaSigna R261 is equipped with a clock detection mechanism that will permanently monitor activity on the EXT_CLK signal. This will ensure that whenever this clock source disappears, BelaSigna R261 will properly enter a known state, using an internal clocking signal, until the external clock comes back.

It has to be noted that the internal PLL of BelaSigna R261 has a free−running mode, whereby it is capable to operate without an external clock reference to be provided. This mode requires special configuration, but can be used when it is not necessary to guarantee an exact clock frequency or when the sampling rate accuracy isn't important.

For more information on the configuration of this clocking architecture, refer to BelaSigna R261 Configuration and Communications Guide.

Power Supply Unit

BelaSigna R261 uses multiple power supplies as can be seen on the simplified representation of the power supply unit in Figure 13.

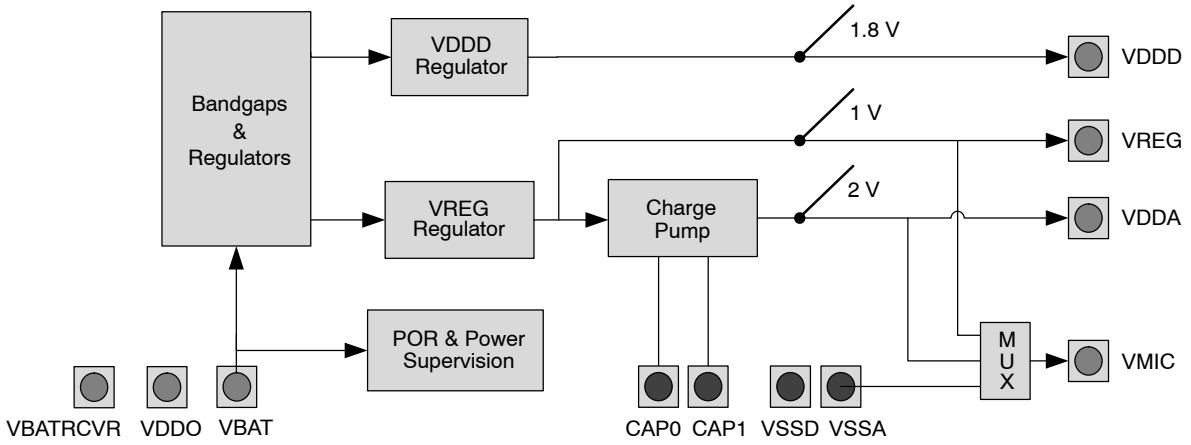


Figure 13. Power Supply Structure

Digital and analog sections of the chip have their own power supplies to allow exceptional audio quality. Several band gap reference circuits and voltage regulators are used to separate the power supplies to the various blocks that compose the BelaSigna R261 architecture.

Table 14 provides a short description of all the power supply pins of BelaSigna R261.

Table 14. POWER SUPPLY VOLTAGES

Voltage	Abbreviation	Description
Battery Supply Voltage	VBAT	The primary voltage supplied to BelaSigna R261 is VBAT. It is typically in the range 1.8 V – 3.3 V. BelaSigna R261 has internal voltage regulator, which allows the application PCB to avoid the use of voltage regulators.
Output Driver Supply Voltage	VBATRCVR	If powered independently and the output driver is to be used, VBATRCVR must be connected to VBAT on the application PCB. Alternatively, if the analog outputs are used, VBATRCVR should be connected to VDDA.
Internal Digital Supply Voltage	VDDD	The internal digital supply voltage is used as the supply voltage for all internal digital components, including being used as the interface voltage at the internal side of the level translation circuitry attached to all of the digital pins. VDDD is provided as an output pad, where a decoupling capacitor to ground has to be placed to filter power supply noise.
External I/O Supply Voltage	VDDO	VDDO is an externally provided power source. It is used by BelaSigna R261 as the external side of the level translation circuitry attached to all of the digital pins. Communication with external devices on digital pins will happen at the level defined on this pin.
Regulated Supply Voltage	VREG	VREG is a 1 V reference to the analog circuitry. It is available externally to allow for additional noise filtering of the regulated voltages within the system. VREG can also be used as a microphone power supply, when the VMIC pin cannot be used.
Analog Supply Voltage	VDDA	VDDA is a 2 V reference voltage generated from the internal charge pump. It is a reference to the analog circuitry. It is available externally to allow for additional noise filtering of the regulated voltages within the system. The internal charge pump uses an external capacitor that is periodically refreshed to maintain the 2 V supply. VDDA can also be used as a microphone power supply, when the VMIC pin cannot be used.
Microphone Bias Voltage	VMIC	VMIC is a configurable microphone bias voltage. VMIC can be configured by the application to provide 1 V or 2 V power supply to the microphones. It can also be grounded or put to High−Z mode to save power when the microphones don't have to be used. The ROM−based application configures VMIC to provide 2 V to the microphones when they are in use, and High−Z when the system is in Sleep mode.

Power Management Strategy & Battery Monitoring

BelaSigna R261 has a built−in power management unit that guarantees valid system operation under any voltage supply condition to prevent any unexpected audio output as the result of any supply irregularity. The unit constantly monitors the power supply and shuts down all functional units (including all units in the audio path) when the power supply voltage goes below a level at which point valid operation can no longer be guaranteed.

The power management unit on BelaSigna R261 includes power−on−reset (POR) functionality as well as power supervisory circuitry, as shown in Figure 13. These two components work together to ensure proper device operation under all battery conditions.

The POR sequence is designed to ensure proper system behavior during start−up and proper system configuration after start−up. At the start of the POR sequence, the audio output is disabled and all configuration and control registers are asynchronously reset to their default values.

The power supervisory circuitry monitors the battery supply voltage (VBAT). This circuit is used to start the system when VBAT reaches a safe startup voltage, and to reset the system when it drops below a relevant voltage threshold. The relevant parameters are shown in Table 15.

Table 15. POWER MANAGEMENT PARAMETERS

Parameters	Voltage Level
VBAT startup (POR_THR_UP)	1.65 V ± 80 mV
VBAT shutdown (POR_THR_DN)	1.6 V ± 50 mV
POR duration (POR_TIME)	5.6 ms

The POR sequence consists of two phases: voltage supply stabilization and boot ROM initialization. During the voltage supply stabilization phase, the following steps are performed:

1. The internal regulators are enabled and allowed to stabilize
2. The internal charge pump is enabled and allowed to stabilize
3. SYSCLK is connected to all of the system components (Free−running PLL output)
4. The system runs the ROM application

At step 1, once the supply voltage rises above the startup voltage (POR_THR) and remains there for a certain time (POR_TIME), a signal will enable the charge pump.

At step 2, another POR_TIME delay is implemented to allow the charge pump to stabilize before toggling the POR signal, and thus enabling the digital core.

If the supply is consistent, the internal system voltage will then remain at a fixed nominal voltage. If a spike occurs that causes the voltage to drop below the shutdown internal system voltage (POR_THR), the system will shut down. If the voltage rises again above the startup voltage and remains there for the required time (POR_TIME), a POR sequence will occur again.

See the electrical characteristics on Table 2 for details on POR_THR and POR_TIME.

Once the ROM application is running, more system monitoring is performed by the application; typically, the software will permanently monitor the presence of an external clock, and take the appropriate actions whenever it disappears. See the system monitoring section for more information.

Digital Communication Interfaces

Debug Port (UART)

BelaSigna R261 has an RS232−based UART that can be used to interface the chip from ON Semiconductor's communication tools. The debug port cannot be used for customer applications. BelaSigna R261 can only be configured using the I^2C interface. See the I^2C interface section for information on how communication tools can interface with BelaSigna R261.

General−Purpose Input Output (GPIO) Ports

BelaSigna R261 has five GPIO ports which are all used with specific functionalities. The five signals are SPI_CLK/CONFIG_SEL, SPI_CS/ATT_SEL, SPI_SERO/ALGO_CTRL, SPI_SERI/SLEEP_CTRL and BOOT_SEL.

The BOOT_SEL pin controls the behavior of the four other GPIOs, as defined in the Booting Control section. When not used as an SPI port, these four other pins will act as GPIOs (ALGO_CTRL and SLEEP_CTRL) or as LSADs (ATT_SEL and CONFIG_SEL).

When used as GPIOs, all pins have pull−up resistors (BOOT_SEL, SLEEP_CTRL and ALGO_CTRL). When used as LSADs (ATT_SEL and CONFIG_SEL), the pull−ups are disabled. If left floating in LSAD mode, the pins have a weak pull−down to ground.

See the Booting Control, Sleep Mode Control and Algorithm Control sections earlier in this document for details on the behavior of these GPIO ports.

I^2C Interface

The I^2C interface is an industry−standard interface that can be used for high−speed transmission of data between BelaSigna R261 and an external device. The interface operates at speeds up to 400 kbit/sec. In product development mode, the I^2C interface is used for application debugging purposes, communicating with the BelaSigna R261 development tools, also known as SignaKlara Development Utility (SKDU). The interface always operates in slave mode and the slave address is 0x61.

A comprehensive command interface can be used with SKDU. It will offer a variety of support functions grouped in different categories like general system control (system reset, status information), application control (switching between operating modes, enabling or disabling the algorithm), hardware setup (for custom configuration of the various hardware units like clocking, input/output stages), algorithm setup (amplitude management, custom algorithm mode loading) and finally the low−level I^2C protocol is also supported. More details on this command interface can be found in the "BelaSigna R261 Configuration and Communications Guide".

Serial Peripheral Interface (SPI) Port

An SPI port is available on BelaSigna R261 for applications such as communication with a non−volatile memory (EEPROM). The I/O levels on this port are defined by the voltage on the VDDO pin. The SPI port operates in master mode only, which supports communications with slave SPI devices. The four signals needed by the SPI port are multiplexed with other functions on BelaSigna R261 (GPIOs, LSADs). The use of the SPI port is excluding the use of these other functions.

Interfaces Unused by the ROM−based Application

BelaSigna R261 also contains hardware provisions for a high speed PCM interface, as well as a high speed UART. These two interfaces are not used by the ROM−based application, hence cannot be used by default. Custom applications developed by ON Semiconductor could enable the use of these interfaces, should this be required.

Long Term Storage Conditions

ON Semiconductor specifies a 24−month maximum storage time for WLCSP devices in pocket tapes and conditioned in dry bags, as stated in Table 16 below and defined in ON Semiconductor's "Finished Goods Packing and Long Term Storage Procedures". (Document # 12MRB17500B)

Table 16. LONG TERM STORAGE CONDITIONS

Storage Condition	Maximum Storage Time	Remarks
temperature 18−28°C, humidity 30−65%RH	24 months after die singulation/sawing date	Maximum 12 months storage at condition 18−28°C, 30−65%RH. Afterwards storage in vacuum moisture bag with desiccant and humidity card. Storage in nitrogen cabinet allowed.

Re−Flow Information

The re−flow profile depends on the equipment that is used for the re−flow and the assembly that is being re−flowed. Care must be taken not to expose the packages to temperatures above the rated features. The WLCSP package is tested to perform reliably up to 3x reflow passes at the maximum reflow peak temperature of 260°C. Use Table 17 from the JEDEC Standard 22−A113D and J−STD−020D as a guideline but note that actual profiles should be developed by customers based on specific process needs and board designs.

Table 17. RE−FLOW INFORMATION

Profile Feature	Pb−free Assembly
Preheat & Soak Temperature minimum (TSMIN) Temperature maximum (TSMAX) Time (TSMIN to TSMAC) (TS)	 150°C 200°C 60−120 seconds
Average Ramp−Up Rate (TSMAX to TP)	3°C/second maximum
Liquidous temperature and time Temperature (TL) Time (tL)	 217°C 60−150 seconds
Peak Temperature (TP)	260 +0/−5°C
Time within 5°C of Actual Peak Temperature	20−40 seconds
Ramp−Down Rate (TP to TSMAX)	6°C/second maximum
Time 25°C to Peak Temperature	8 minutes maximum

Miscellaneous

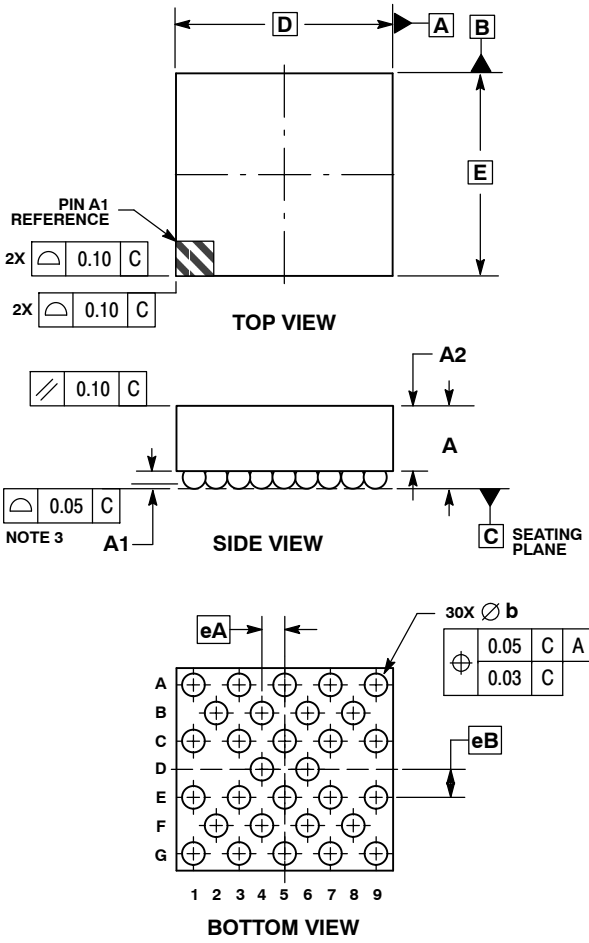
Chip Identification

Chip identification information can be retrieved by using the Communications Accelerator Adaptor (CAA) tool along with the protocol software provided by ON Semiconductor. For BelaSigna R261, the key identifier components and values are as follows:

Chip Family	Chip Version
0x02 (SK2)	0x3010

PACKAGE DIMENSIONS

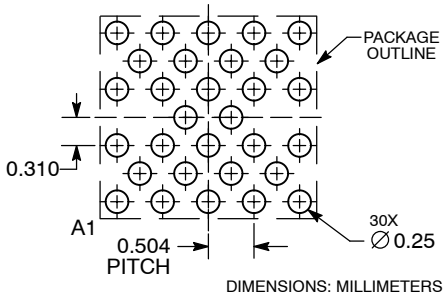
WLCSP30, 2.233x2.388
CASE 567CT−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.84	1.00
A1	0.17	0.23
A2	0.72 REF	
b	0.24	0.29
D	2.388 BSC	
E	2.233 BSC	
eA	0.252 BSC	
eB	0.310 BSC	

RECOMMENDED SOLDERING FOOTPRINT*

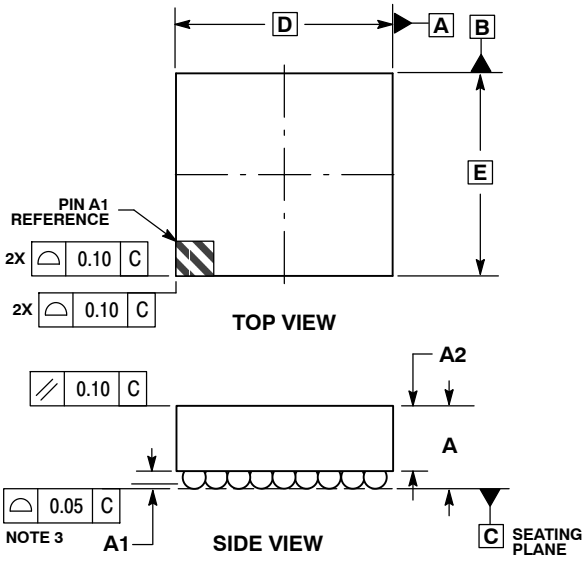


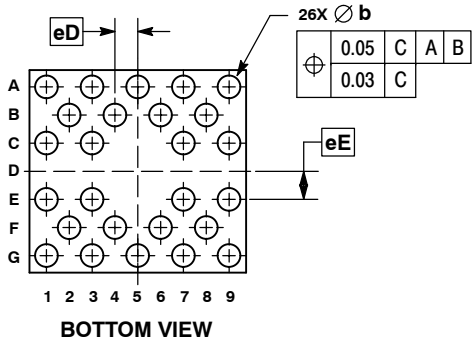
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

WLCSP26, 2.388x2.233
CASE 567CY−01
ISSUE O

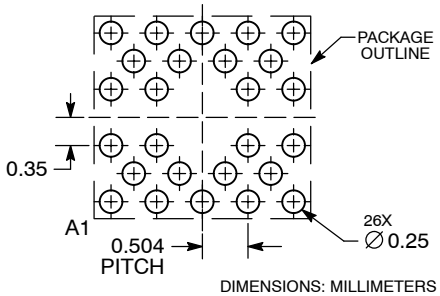




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.84	1.00
A1	0.17	0.23
A2	0.72 REF	
b	0.24	0.29
D	2.388 BSC	
E	2.233 BSC	
eD	0.252 BSC	
eE	0.310 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Assembly / Design Notes

For PCB manufacture with BelaSigna R261, ON Semiconductor recommends solder−on−pad (SoP) surface finish. With SoP, the solder mask opening should be non−solder mask−defined (NSMD) and copper pad geometry will be dictated by the PCB vendor's design requirements.

Alternative surface finishes are ENiG and OSP; volume of screened solder paste (#5) should be less than 0.0008 mm^3. If no pre−screening of solder paste is used, then the following conditions must be met:

1. the solder mask opening should be >0.3 mm in diameter,
2. the copper pad will have 0.25 mm diameter, and
3. solder mask thickness should be less than 1 mil thick above the copper surface.

ON Semiconductor can provide BelaSigna R261 mounting foot print guidelines to assist your PCB design upon request.

Table 18. ORDERING INFORMATION

Device	Marking	Package	Shipping †
BR261W30A101E1G	BR261W30	WLCSP30	2500 / Tape & Reel
BR261W26A101E1G	BR261W26	WLCSP26	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative