MAXIM

CMOS 8-Bit Buffered Multiplying DACs

T-51-09-08

General Description

The AD7524 and MAX7624 are CMOS 8-bit digital-to-analog converters (DAC) which will interface directly with most microprocessors. On-chip input latches make the DAC interface similar to a RAM write cycle where CS and WR are the only control inputs required.

Linearity up to ±⅛ LSB is available (AD7524L/C/U grades) and power consumption is less than 10mW. Monotonicity is guaranteed over the full temperature range.

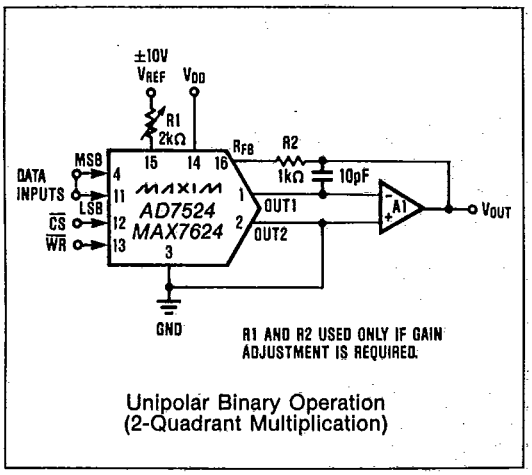
For the AD7524, +5V TTL and CMOS logic compatibility is guaranteed when using +5V power. Over the supply range of +5V to +15V, all logic inputs are high voltage CMOS compatible.

The MAX7624 has +5V TTL/CMOS compatible inputs for a +12V to +15V supply range.

Applications

μP Controlled Gain
Function Generators
Bus Structured Instruments
Automatic Test Equipment
Digital Control Systems

Typical Operating Circuit



Unipolar Binary Operation
(2-Quadrant Multiplication)

Features

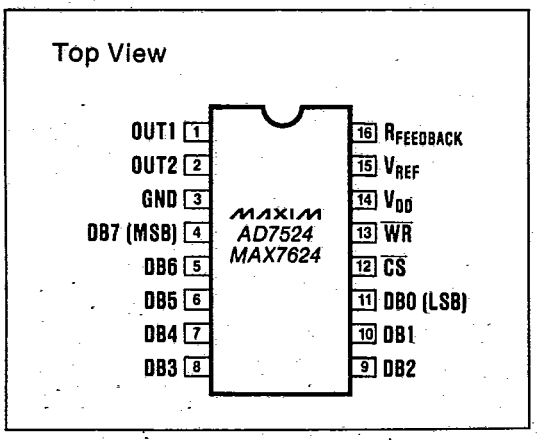
- Microprocessor Compatible
- On-Chip Data Latches
- Guaranteed Monotonic Over Temp.
- Low Power Consumption
- 8, 9, and 10-Bit Linearity
- AD7524 TTL/CMOS Compatible at +5V
- MAX7624 TTL/CMOS Compatible at +12V to +15V

Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7524JN	0°C to +70°C	Plastic DIP	±½ LSB
AD7524KN	0°C to +70°C	Plastic DIP	±¼ LSB
AD7524LN	0°C to +70°C	Plastic DIP	±⅛ LSB
AD7524JCSE	0°C to +70°C	Small Outline	±½ LSB
AD7524KCSE	0°C to +70°C	Small Outline	±¼ LSB
AD7524LCSE	0°C to +70°C	Small Outline	±⅛ LSB
AD7524JC/D	0°C to +70°C	Dice	±½ LSB
AD7524AD	-25°C to +85°C	Ceramic	±½ LSB
AD7524BD	-25°C to +85°C	Ceramic	±¼ LSB
AD7524CD	-25°C to +85°C	Ceramic	±⅛ LSB

* *All devices — 16 lead packages*
** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages*
(Ordering Information continued on last page)

Pin Configuration



CMOS 8-Bit Buffered Multiplying DACs

ABSOLUTE MAXIMUM RATINGS—AD7524, MAX7624

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
V_{RFB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V to V_{DD} + 0.3V
OUT1, OUT2 to GND ..... -0.3V, V_{DD}
Operating Temperature Ranges
AD7524JN, KN, LN, JCSE, KCSE, LCSE
MAX7624CPE, CSE ..... 0°C to +70°C
Operating Temperature Ranges (continued)
AD7524AD, AQ, BD, BQ, CD, CQ .... -25°C to +85°C
MAX7624EPE ..... -40°C to +85°C
AD7524SD, SQ, TD, TQ, UD, UQ
MAX7624MJE ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Power Dissipation (any Package) to +75°C 450mW
Derate Above +75°C by ..... 6 mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—AD7524, +5V Operation

(V_{DD} = +5V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY							
Resolution				8			Bits
Relative Accuracy	INL	J,A,S K,B,T L,C,U				±1/2 ±1/2 ±1/2	LSB
Differential Non-Linearity	DNL	All Grades Guaranteed Monotonic Over Temp.				±1	LSB
Gain Error (Note 1)		T_A = 25°C T_A = T_{MIN} to T_{MAX}				±2½ ±3½	LSB
Gain Temp. Coefficient (Note 2, 3)					±2	±40	ppm/°C
Supply Rejection (Note 2)	PSR	ΔV_{DD} = ±10%	T_A = 25°C T_A = T_{MIN} to T_{MAX}		0.002 0.01	0.08 0.16	%FSR/%
Output Leakage Current (I_{OUT1})		V_{REF} = ±10V DAC is 00000000	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±400	nA
Output Leakage Current (I_{OUT2})		V_{REF} = ±10V DAC is 11111111	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±400	nA
REFERENCE INPUT							
R_{IN} (pin 15 to GND)				5	10	20	kΩ
DYNAMIC PERFORMANCE							
Output Current Settling-Time to 1/2 LSB (Note 2)		DB0-DB7 = 0V to V_{DD} to 0V $\overline{WR}$ = $\overline{CS}$ = 0V OUT1 Load = 100Ω, C_{EXT} = 13pF;	T_A = 25°C T_A = T_{MIN} to T_{MAX}			400 500	ns
AC Feedthrough (OUT1 or OUT2) (Note 2)		V_{REF} = ±10V 100kHz Sinewave DB0-DB7 = $\overline{WR}$ = $\overline{CS}$ = 0V	T_A = 25°C T_A = T_{MIN} to T_{MAX}			0.25 0.5	%FSR
ANALOG OUTPUTS							
OUT1 Capacitance (Note 2)	C_{OUT1}	DB0-DB7 = V_{DD}; $\overline{WR}$ = $\overline{CS}$ = 0V DB0-DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V				120 30	pF
OUT2 Capacitance (Note 2)	C_{OUT2}	DB0-DB7 = V_{DD}; $\overline{WR}$ = $\overline{CS}$ = 0V DB0-DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V				30 120	pF

Note 1: Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}.
Note 2: Guaranteed, but not tested.
Note 3: Gain error measured from 25°C to T_{MAX} or from 25°C to T_{MIN}.
Note 4: Sample tested at 25°C to ensure compliance.

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ELECTRICAL CHARACTERISTICS—AD7524, +5V Operation (Continued)

(V_{DD} = +5V, V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	T_A = 25°C; V_{IN} = 0V or V_{DD} T_A = T_{MIN} to T_{MAX}			±1 ±10	μA
Input Capacitance (Note 2)	C_{IN}	DB0-DB7 $\overline{WR}$, $\overline{CS}$			8 20	pF
POWER REQUIREMENTS						
Supply Current	I_{DD}	Digital inputs V_{IL} or V_{IH} T_A = 25°C T_A = T_{MIN} to T_{MAX}			1 2	mA
		Digital inputs 0V or V_{DD} T_A = 25°C T_A = T_{MIN} to T_{MAX}			100 500	μA
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram)						
Chip Select to Write Setup Time	t_{CS}	T_A = 25°C T_A = T_{MIN} to T_{MAX} J,K,L,A,B,C T_A = T_{MIN} to T_{MAX} S,T,U	170 220 240			ns
Chip Select to Write Hold Time	t_{CH}		0			ns
Write Pulse Width	t_{WR}	T_A = 25°C T_A = T_{MIN} to T_{MAX} J,K,L,A,B,C T_A = T_{MIN} to T_{MAX} S,T,U	170 220 240			ns
Data Setup Time	t_{DS}	T_A = 25°C T_A = T_{MIN} to T_{MAX} J,K,L,A,B,C T_A = T_{MIN} to T_{MAX} S,T,U	135 170 170			ns
Data Hold Time	t_{DH}		10			ns

ELECTRICAL CHARACTERISTICS—AD7524, +15V Operation

(V_{DD} = +15V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			8			Bits
Relative Accuracy	INL	J,A,S K,B,T L,C,U			±1/2 ±1/4 ±1/8	LSB
Differential Non-Linearity	DNL	All Grades Guaranteed Monotonic Over Temp.			±1	LSB
Gain Error (Note 1)		T_A = 25°C T_A = T_{MIN} to T_{MAX}			±1¼ ±1½	LSB
Gain Temp. Coefficient (Note 2, 3)				±1	±10	ppm/°C
Supply Rejection (Note 2)	PSR	ΔV_{DD} = ±10% T_A = 25°C T_A = T_{MIN} to T_{MAX}		0.001 0.005	0.02 0.04	%FSR/%
Output Leakage Current (I_{OUT1})		V_{REF} = ±10V T_A = 25°C DAC is 00000000 T_A = T_{MIN} to T_{MAX}			±50 ±200	nA
Output Leakage Current (I_{OUT2})		V_{REF} = ±10V T_A = 25°C DAC is 11111111 T_A = T_{MIN} to T_{MAX}			±50 ±200	nA

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ELECTRICAL CHARACTERISTICS—AD7524, +15V Operation (Continued)

(V_{DD} = +15V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE INPUT						
R_{IN} (pin 15 to GND)			5	10	20	kΩ
DYNAMIC PERFORMANCE						
Output Current Settling-Time to 1/2 LSB (Note 2)		$\overline{DB0}$-$\overline{DB7}$ = 0V to V_{DD} to 0V $\overline{WR}$ = $\overline{CS}$ = 0V T_A = 25°C OUT1 Load = 100Ω, T_A = T_{MIN} to T_{MAX} C_{EXT} = 13pF;			250 350	ns
AC Feedthrough (OUT1 or OUT2) (Note 2)		V_{REF} = ±10V 100kHz Sinewave T_A = 25°C $\overline{DB0}$-$\overline{DB7}$ = $\overline{WR}$ = T_A = T_{MIN} to T_{MAX} $\overline{CS}$ = 0V			0.25 0.5	%FSR
ANALOG OUTPUTS						
OUT1 Capacitance (Note 2)	C_{OUT1}	DB0-DB7 = V_{DD}; $\overline{WR}$ = $\overline{CS}$ = 0V DB0-DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V			120 30	pF
OUT2 Capacitance (Note 2)	C_{OUT2}	DB0-DB7 = V_{DD}; $\overline{WR}$ = $\overline{CS}$ = 0V DB0-DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V			30 120	pF
DIGITAL INPUTS						
Input High Voltage	V_{IH}		13.5			V
Input Low Voltage	V_{IL}				1.5	V
Input Current	I_{IN}	T_A = 25°C; V_{IN} = 0V or V_{DD} T_A = T_{MIN} to T_{MAX}			±1 ±10	μA
Input Capacitance (Note 2)	C_{IN}	$\overline{DB0}$-$\overline{DB7}$ $\overline{WR}$, $\overline{CS}$			8 20	pF
POWER REQUIREMENTS						
Supply Current	I_{DD}	Digital inputs V_{IL} or V_{IH}			2	mA
		Digital inputs 0V or V_{DD} T_A = 25°C T_A = T_{MIN} to T_{MAX}			100 500	μA
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram)						
Chip Select to Write Setup Time	t_{CS}	T_A = 25°C T_A = T_{MIN} to T_{MAX} J,K,L,A,B,C T_A = T_{MIN} to T_{MAX} S,T,U	100 130 150			ns
Chip Select to Write Hold Time	t_{CH}		0			ns
Write Pulse Width	t_{WR}	T_A = 25°C T_A = T_{MIN} to T_{MAX} J,K,L,A,B,C T_A = T_{MIN} to T_{MAX} S,T,U	100 130 150			ns
Data Setup Time	t_{DS}	T_A = 25°C T_A = T_{MIN} to T_{MAX} J,K,L,A,B,C T_A = T_{MIN} to T_{MAX} S,T,U	60 80 100			ns
Data Hold Time	t_{DH}		10			ns

Note 1: Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}.
Note 2: Guaranteed, but not tested.
Note 3: Gain error measured from 25°C to T_{MAX} or from 25°C to T_{MIN}.
Note 4: Sample tested at 25°C to ensure compliance.

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ELECTRICAL CHARACTERISTICS—MAX7624, +12V to +15V Operation

(V_{DD} = +10.8V to +15.75V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			8			Bits
Relative Accuracy	INL				±1/2	LSB
Differential Non-Linearity	DNL	All Grades Guaranteed Monotonic Over Temp.			±1	LSB
Gain Error (Note 1)					±2	LSB
Gain Temp. Coefficient (Note 2, 3)				±1	±10	ppm/°C
Supply Rejection (Note 2)	PSR	V_{DD} = +10.8V to +15.75V; T_A = 25°C T_A = T_{MIN} to T_{MAX}		0.001 0.005	0.02 0.04	%FSR/%
Output Leakage Current (I_{OUT1})		V_{REF} = ±10V, DAC is 00000000; T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±200	nA
Output Leakage Current (I_{OUT2})		V_{REF} = ±10V, DAC is 11111111; T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±200	nA
REFERENCE INPUT						
R_{IN} (pin 15 to GND)			5	10	20	kΩ
DYNAMIC PERFORMANCE						
Output Current Settling-Time to 1/2 LSB (Note 2)		DB0-DB7 = 0V to +5V to 0V; $\overline{WR}$ = $\overline{CS}$ = 0V; T_A = 25°C OUT1 Load = 100Ω, T_A = T_{MIN} to T_{MAX} C_{EXT} = 13pF;			250 350	ns
AC Feedthrough (OUT1 or OUT2) (Note 2)		V_{REF} = ±10V, 100kHz Sinewave; T_A = 25°C DB0-DB7 = $\overline{WR}$ = T_A = T_{MIN} to T_{MAX} $\overline{CS}$ = 0V			0.25 0.5	%FSR
ANALOG OUTPUTS						
OUT1 Capacitance (Note 2)	C_{OUT1}	DB0-DB7 = +5V; $\overline{WR}$ = $\overline{CS}$ = 0V DB0-DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V			60 25	pF
OUT2 Capacitance (Note 2)	C_{OUT2}	DB0-DB7 = +5V; $\overline{WR}$ = $\overline{CS}$ = 0V DB0-DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V			25 60	pF
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	T_A = 25°C; V_{IN} = 0V or V_{DD} T_A = T_{MIN} to T_{MAX}			±1 ±10	µA
Input Capacitance (Note 2)	C_{IN}	DB0-DB7, $\overline{WR}$, $\overline{CS}$			8	pF
POWER REQUIREMENTS						
Supply Current	I_{DD}	Digital inputs V_{IL} or V_{IH}			2.5	mA
		Digital inputs 0V or V_{DD}; T_A = 25°C T_A = T_{MIN} to T_{MAX}			100 500	µA

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ELECTRICAL CHARACTERISTICS—MAX7624, +12V to +15V Operation (Continued)

(V_{DD} = +10.8V to +15.75V, V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram)						
Chip Select to Write Setup Time	t_{CS}	T_A = 25°C T_A = T_{MIN} to T_{MAX} C,E T_A = T_{MIN} to T_{MAX} M	160 160 210			ns
Chip Select to Write Hold Time	t_{CH}		10			ns
Write Pulse Width	t_{WR}	T_A = 25°C T_A = T_{MIN} to T_{MAX} C,E T_A = T_{MIN} to T_{MAX} M	150 170 210			ns
Data Setup Time	t_{DS}	T_A = 25°C T_A = T_{MIN} to T_{MAX} C,E T_A = T_{MIN} to T_{MAX} M	160 160 210			ns
Data Hold Time	t_{DH}		10			ns

Detailed Description

The AD7524/MAX7624 is an 8-bit multiplying digital-to-analog converter (DAC) that consists of a thin-film R-2R resistor array with CMOS current steering switches. In applications requiring a voltage output, an output operational amplifier and reference will be needed. Figure 1 shows a simplified schematic of the DAC. The inverted R-2R ladder divides the voltage or current reference in a binary manner among the eight steering switches. The magnitude of the current appearing at either OUT terminal depends on the number of switches selected, and therefore the output is an analog representation of the digital input. The two OUT terminals must be held at the same potential so a constant current is maintained in each ladder leg. This makes the V_{REF} input current independent of switch state and also ensures that the AD7524/MAX7624 maintains its excellent linearity performance.

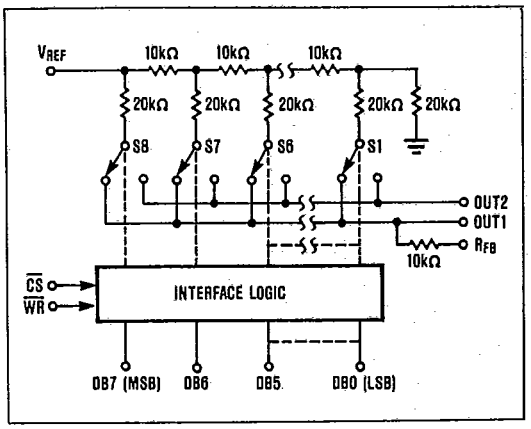

Figure 1. AD7524/MAX7624 Functional Diagram

Equivalent-Circuit Analysis

The equivalent circuit for all digital inputs LOW is shown in figure 2. In this state the reference current is switched to OUT2. The current source, $I_{LEAKAGE}$, is composed of small surface and junction leakages to the substrate which double every 10°C. The R-2R ladder termination resistor generates a constant 1/256 current which represents 1 LSB of the reference current, I_{REF}. The value of output capacitance at the OUT1 and OUT2 terminals is input code dependent and lies in the range 20pF to 30pF.

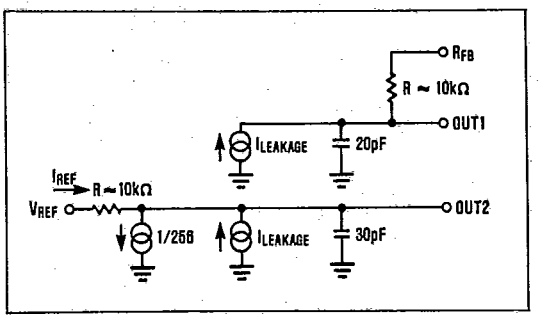

Figure 2. AD7524/MAX7624 DAC Equivalent Circuit—All Digital Inputs LOW

The AD7524's digital inputs are TTL compatible when operated with a V_{DD} of +5V (V_{IH} = 2.4V, V_{IL} = 0.8V). Internal level shifters convert from TTL to CMOS logic levels. When V_{IN} is in the region 1.5 to 3.5 volts, the input buffers operate in their linear region and the quiescent current increases as indicated by the graph in figure 3. Therefore to minimize supply current it is recommended that the digital inputs be as close to the supply rails as possible (V_{DD} and DGND).

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The AD7524 may be operated with any supply voltage in the range $5V < V_{DD} < 15V$. With V_{DD} = +15V the input logic levels are CMOS compatible only, i.e. 1.5V and 13.5V.

The MAX7624's digital inputs are TTL/CMOS compatible for a +12V to +15V supply range. However, when V_{IN} is in the range of 1.5V to V_{DD} - 1.5V the input buffers operate in their linear region and the quiescent current increases (see figure 3).

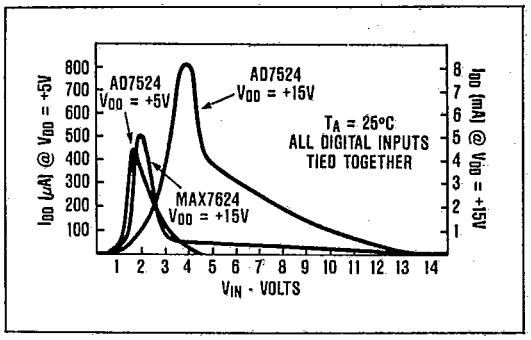


Figure 3. Typical Supply Current, I_{DD} vs. Logic Input Voltage V_{IN}, for V_{DD} = +5V and +15V

Interface Logic Information

Mode Selection

The inputs $\overline{CS}$ and $\overline{WR}$ control the operating mode of the AD7524/MAX7624. See Mode Selection Table.

Mode Selection Table

$\overline{CS}$	$\overline{WR}$	MODE	DAC RESPONSE
L	L	WRITE	DAC responds to data bus (DB0-DB7) inputs
H X	X H	HOLD HOLD	Data bus (DB0-DB7) is locked out; DAC holds last data present when $\overline{CS}$ or $\overline{WR}$ assumed HIGH state

L = Low State, H = High State, X = Don't Care

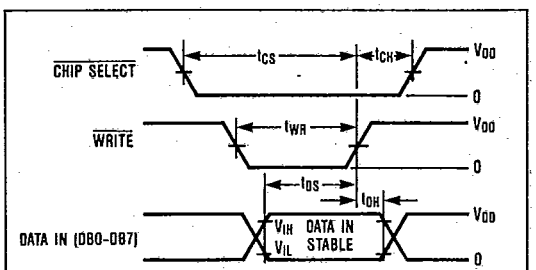
Write Mode

When $\overline{CS}$ and $\overline{WR}$ are both LOW, the AD7524/MAX7624 is in the write mode, and the AD7524/MAX7624 analog output responds to data activity at the DB0-DB7 data bus inputs. In this mode, the data latches are transparent.

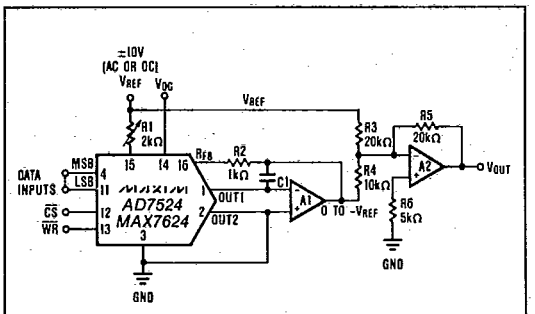
Hold Mode

The AD7524/MAX7624 retains the data that was present on DB0-DB7 just prior to $\overline{CS}$ or $\overline{WR}$ assuming a high state. The analog output remains at the value corresponding to the digital code locked in the data latch.

Write Cycle Timing Diagram



NOTES:
1. FOR THE AD7524 ALL INPUT SIGNAL RISE AND FALL TIMES ARE MEASURED FROM 10% TO 90% OF V_{DD}. V_{DD} = +5V, $t_r = t_f$ = 20ns; V_{DD} = +15V, $t_r = t_f$ = 40ns.
2. FOR THE MAX7624 ALL INPUT SIGNAL RISE AND FALL TIMES ARE MEASURED FROM 10% TO 90% OF +5V.
3. TIMING MEASUREMENT REFERENCE LEVEL IS $(V_{IH} + V_{IL})/2$.



NOTES:
1. ADJUST R1 FOR V_{OUT} = 0V AT CODE 10000000.
2. C1 PHASE COMPENSATION (10-15pF) MAY BE REQUIRED IF A1 IS A HIGH SPEED AMPLIFIER

Figure 4. Bipolar (4-Quadrant) Operation

CMOS 8-Bit Buffered Multiplying DACs

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7524AQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7524BQ	-25°C to +85°C	CERDIP**	±¼ LSB
AD7524CQ	-25°C to +85°C	CERDIP**	±⅛ LSB
AD7524SD	-55°C to +125°C	Ceramic	±½ LSB
AD7524TD	-55°C to +125°C	Ceramic	±¼ LSB
AD7524UD	-55°C to +125°C	Ceramic	±⅛ LSB
AD7524SQ	-55°C to +125°C	CERDIP**	±½ LSB
AD7524TQ	-55°C to +125°C	CERDIP**	±¼ LSB
AD7524UQ	-55°C to +125°C	CERDIP**	±⅛ LSB
MAX7624CPE	0°C to +70°C	Plastic DIP	±½ LSB
MAX7624CSE	0°C to +70°C	Small Outline	±½ LSB
MAX7624C/D	0°C to +70°C	Dice	±½ LSB
MAX7624EPE	-40°C to +85°C	Plastic DIP	±½ LSB
MAX7624MJE	-55°C to +125°C	CERDIP	±½ LSB

* *All devices—16 lead packages*
** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Chip Topography

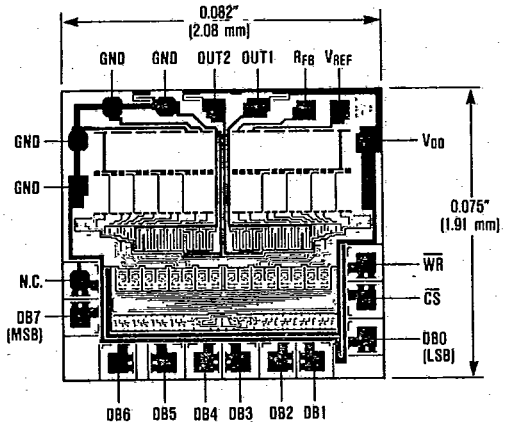


Table 1. Unipolar Binary Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{255}{256}\right)$
1 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{129}{256}\right)$
1 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{127}{126}\right)$
0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{256}\right)$
0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{0}{256}\right) = 0$

Note: 1LSB = $(2^{-8})(V_{REF}) = \frac{1}{256}(V_{REF})$

Table 2. Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{127}{128}\right)$
1 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{128}\right)$
1 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{128}\right)$
0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{127}{128}\right)$
0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{128}{128}\right)$

Note: 1LSB = $(2^{-7})(V_{REF}) = \frac{1}{128}(V_{REF})$