CY26580

PacketClock™ Network Applications Clock

Features

- Integrated phase-locked loop (PLL)
- Low-jitter, high-accuracy outputs
- 3.3V operation

Benefits

- Internal PLL with precision operation
- Meets critical timing requirements in complex system designs
- Enables application compatibility

Table 1. Frequency Table

Part Number	Outputs	Input Frequency	Output Frequencies
CY26580-1	2	125MHz or 25-MHz driven	100 MHz, 133.33 MHz

Logic Block Diagram

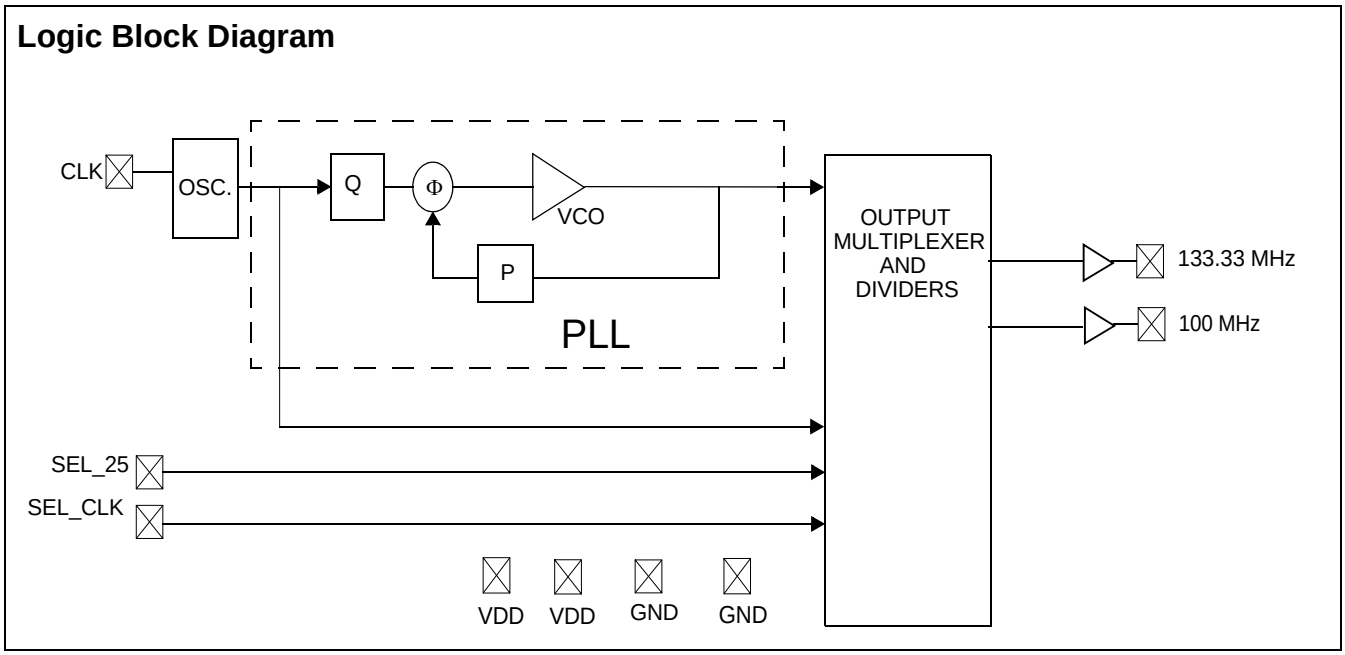


Table 2. Input Select Options

SEL_25	SEL_CLK	Input Type	Input Frequency	CLK1	CLK2	Unit
X	0	Do not use				
0	1	Driven	125	133.33	100	MHz
1	1	Driven	25	133.33	100	MHz

Pin Configuration

Figure 1. CY26580 20-pin SSOP (QSOP)

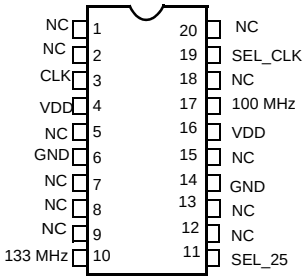


Table 3. Pin Definition

Pin Name	Pin Number	Pin Description
NC	1	No Connect
NC	2	No Connect
CLK	3	Reference Input
V_{DD}	4	Voltage Supply
NC	5	No Connect
GND	6	Ground
NC	7	No Connect
NC	8	No Connect
NC	9	No Connect
133 MHz	10	133.33-MHz Clock Output
SEL_25	11	Reference Frequency Select Input; 0 = 125 MHz, 1 = 25 MHz, weak internal pull up
NC	12	No Connect
NC	13	No Connect
GND	14	Ground
NC	15	No Connect
V_{DD}	16	Voltage Supply
100 MHz	17	100-MHz Clock Output
NC	18	No Connect
SEL_CLK	19	Reference Select Input; Set to 1 = Driven, weak internal pull up
NC	20	No Connect

Absolute Maximum Conditions[1]

Supply Voltage (V_{DD}) ..... –0.5 to +7.0V
DC Input Voltage ..... –0.5V to V_{DD}+0.5
Storage Temperature (Non-condensing) .... –55°C to +125°C
Junction Temperature ..... –40°C to +125°C
Data Retention at Tj = 125°C .....> 10 years
Package Power Dissipation..... 350 mW
ESD (Human Body Model) MIL-STD-883..... 2000V

Recommended Operating Conditions

Parameter	Description	Min	Typ.	Max	Unit
V_{DD}	Supply Voltage	3.14	3.3	3.47	V
T_A, I-grade	Ambient Temperature, Industrial	–40	–	85	°C
C_{LOAD}	Max. Load Capacitance	–	–	15	pF
f_{REF}	Reference Frequency	–	125, 25	–	MHz

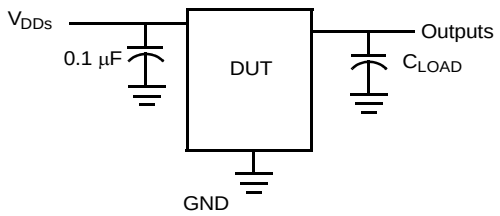
DC Electrical Specifications

Parameter[2]	Description	Conditions	Min	Typ.	Max	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3V$	12	24	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD} = 3.3V$	12	24	–	mA
I_{IH}	Input High Current	$V_{IH} = V_{DD}$	–	5	10	µA
I_{IL}	Input Low Current	$V_{IL} = 0V$	–	–	50	µA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7	–	–	V_{DD}
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}	–	–	0.3	V_{DD}
I_{DD}	Supply Current	V_{DD} Current, no load	–	35	50	mA
R_{UP}	Pull up resistor on Inputs	V_{DD} = 3.14 to 3.47V, measured $V_{IN} = 0V$	–	100	150	kΩ

AC Electrical Specifications

Parameter[2]	Description	Conditions	Min	Typ.	Max	Unit
F_{error}	Frequency Error	All clocks			0	ppm
DC	Output Duty Cycle	Duty Cycle is defined in Figure 3, 50% of V_{DD}	45	50	55	%
ER	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD}, C_{LOAD} = 15 pF. See Figure 4.	0.8	1.4	2	V/ns
EF	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of V_{DD}, C_{LOAD} = 15 pF. See Figure 4.	0.8	1.4	2	V/ns
t_9	Clock Jitter	CLK1, CLK2 Peak-Peak period jitter	–	100	–	ps
t_{10}	PLL Lock Time		–	–	3	ms

Figure 2. Test and Measurement Setup



Notes
1. Above which the useful life may be impaired. For user guidelines, not tested.
2. Guaranteed by characterization, not 100% tested.

Voltage and Timing Definitions

Figure 3. Duty Cycle Definition

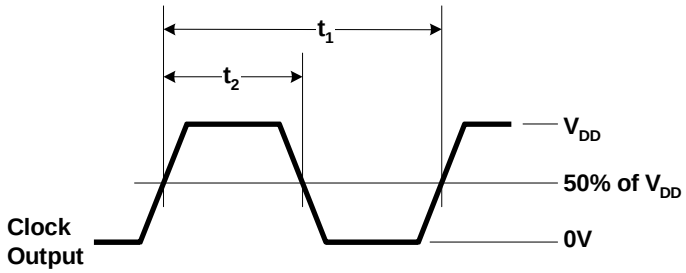
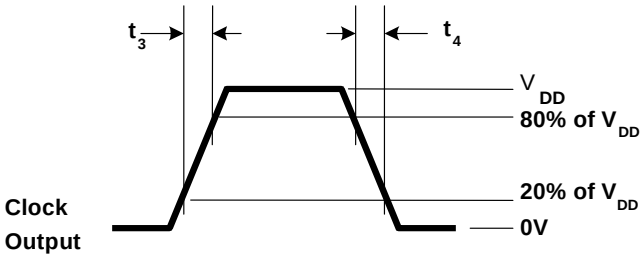


Figure 4. ER = (0.6 x V_{DD}) /t3, EF = (0.6 x V_{DD}) /t4



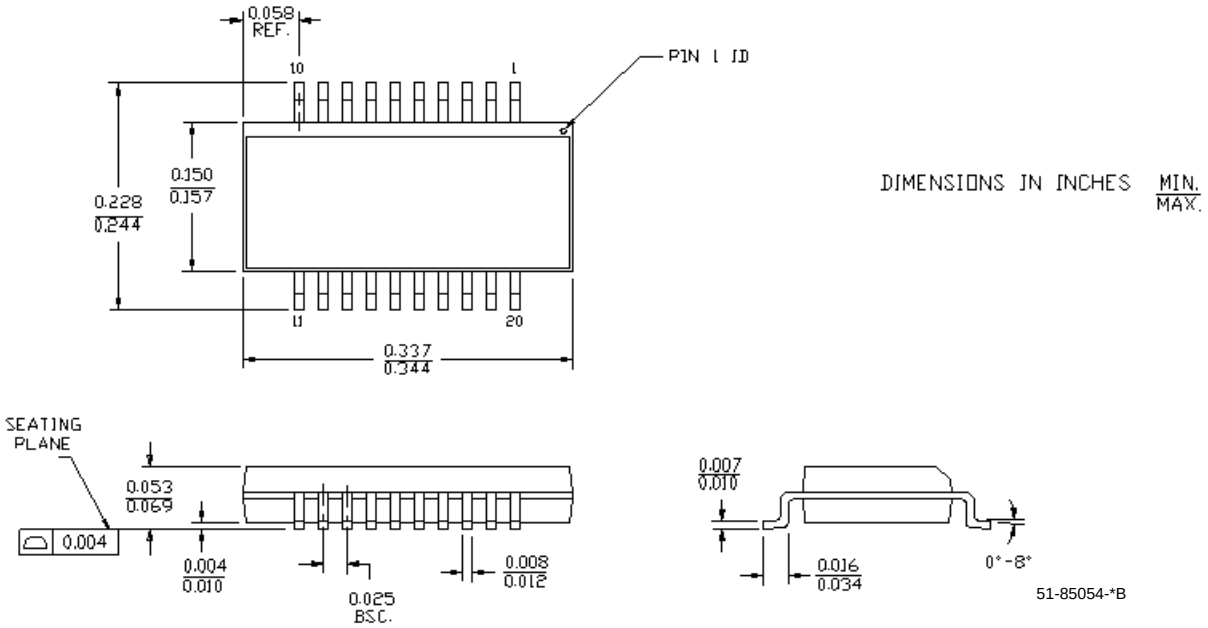
Ordering Information

Ordering Code[3]	Package Type	Temperature Range	Operating Voltage
CY26580OI–2[4]	20-pin SSOP (QSOP)	Industrial	3.3V
CY26580OI–2T[4]	20-pin SSOP (QSOP) – Tape and Reel	Industrial	3.3V
CY26580KOI–2	20-pin SSOP (QSOP)	Industrial	3.3V
CY26580KOI–2T	20-pin SSOP (QSOP) – Tape and Reel	Industrial	3.3V
Pb-Free			
CY26580KQXI–2	20-pin SSOP (QSOP)	Industrial	3.3V
CY26580KQXI–2T	20-pin SSOP (QSOP) – Tape and Reel	Industrial	3.3V

Notes
3. Part numbers ending in -1 and -1T have been replaced by part numbers ending in -2 and -2T. Specifications for -1, -1T, -2 and -2T part numbers are identical.
4. Not recommended for new designs.

Package Drawing and Dimensions

Figure 5. 20-lead QSOP O201 and SQ201



Document History Page

Document Title: CY26580 PacketClock™ Network Applications Clock Document #: 38-07536 Rev. *C				
REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	127357	06/17/03	RGL	New Data Sheet
*A	128564	09/12/03	IJA	Change pin 1 to NC and pin 3 to CLK
*B	216828	See ECN	RGL	Removed Preliminary
*C	2442066	See ECN	KVM/AESA	Updated template. Added Note “Not recommended for new designs.” Added Note explaining “-1” and “-2” part numbers. Removed part numbers CY26580OI-1 and CY26580OI-1T. Added part number CY26580OI–2T, CY26580KOI–2, CY26580KOI–2T, CY26580KQXI–2, and CY26580KQXI–2T in ordering information table. Updated figure caption for package drawing.

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