AK8857VQ
Dual Channel Digital Video Decoder

Overview

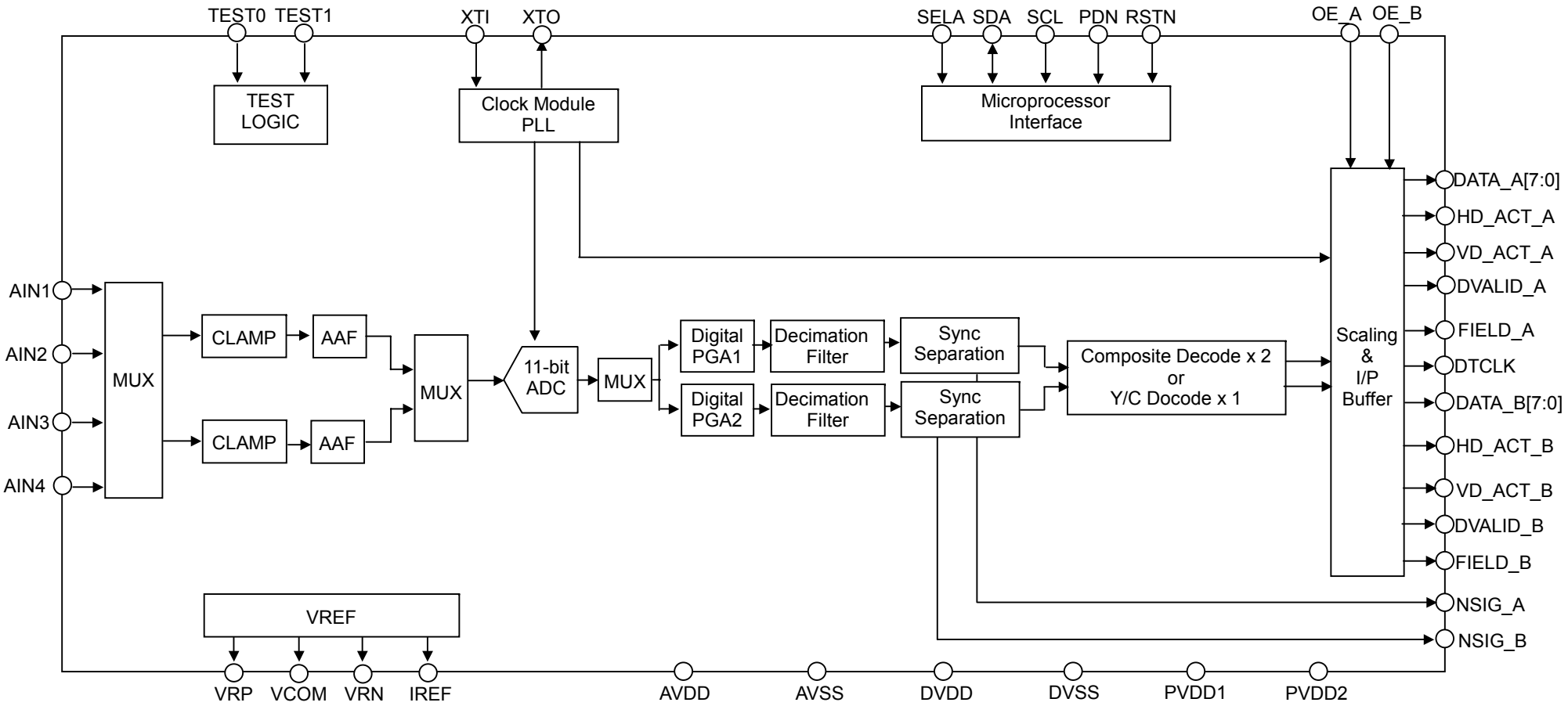
The AK8857VQ is a single-chip digital video decoder for composite and s-video video signals. In case of composite video signal, it can decode two inputs at the same time. Its output data is in YCbCr format, compliant with ITU-R BT.601. Its output interface is ITU-R BT.656 compliant. A simple IP conversion function is built internally and the output pixel size also can easily be changed using this function. The operating temperature range is −40°C to 85°C. The package is 64-terminal LQFP.

Features

- Decodes two inputs of composite video signals NTSC (J, M, 4.43), PAL (B, D, G, H, I, M, N, Nc, 60), SECAM at the same time.
- Decodes S-video video signals NTSC (J, M, 4.43), PAL (B, D, G, H, I, M, N, Nc, 60), SECAM.
- Four input channels, with internal video switch.
- 11-bit 54Mhz ADC 1 channel.
- Digital PGA.
- Adaptive automatic gain control (AGC).
- Auto Color Control (ACC)
- Simple IP conversion function (Line repeating process).
- Image adjustment (contrast, saturation, brightness, hue, sharpness).
- Automatic input signal detection.
- Adaptive 2-D Y/C separation.
- ITU-R BT.656 and ITU-R BT.601 format output (with 4:2:2_8 bit parallel_EAV/SAV).
- Supported output pixel size : 720x487, 720x576, WVGA, VGA, WQVGA, QVGA
- SYNC signal timing for external output : HSYNC/HACT, VSYNC/VACT, FIELD, DVALID
- Closed-caption signal decoding (output via register).
- VBID(CGMS-A) signal decoding (CRCC decode) (output via register).
- WSS signal decoding (output via register).
- Power down function.
- I^2C control.
- 1.70~2.00 V core power supply.
- 1.70~3.60 V interface power supply.
- Operating temperature range: −40°C to 85°C.
- 64-pin LQFP package.

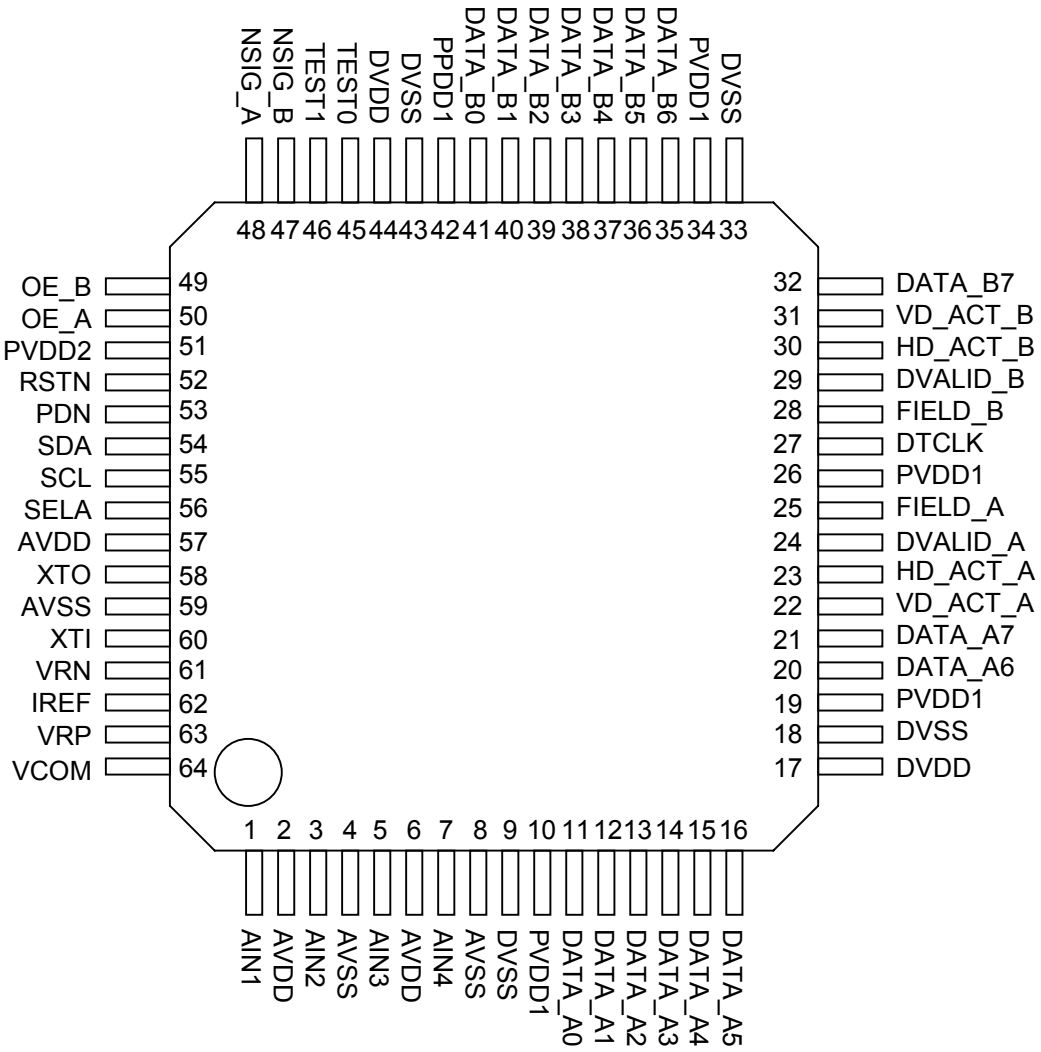
*Because the data is sampling to a fixed clock, it may not fullfilled the ITU-R BT.656 standard interface.

1.Functional Block Diagram



In this specification, the output pins above the DTCLK pin on the right side of this block diagram is called [A BLOCK] and the output pins below the DTCLK pin is called [B BLOCK].

2.Pin assignment – 64 pins LQFP



3.Pin Functions

Pin No.	Symbol	P/S[1]	I/O[2]	Functional Description
1	AIN1	A	I	Analog video signal input pin. Connect via 0.033 μF capacitor and voltage-splitting resistors as shown in page 121. If it is not used, connect to NC.
2	AVDD	A	P	Analog ground pin.
3	AIN2	A	I	Analog video signal input pin. Connect via 0.033 μF capacitor and voltage-splitting resistors as shown in page 121. If it is not used, connect to NC.
4	AVSS	A	G	Analog ground pin.
5	AIN3	A	I	Analog video signal input pin. Connect via 0.033 μF capacitor and voltage-splitting resistors as shown in page 121. If it is not used, connect to NC.
6	AVDD	A	P	Analog ground pin.
7	AIN4	A	I	Analog video signal input pin. Connect via 0.033 μF capacitor and voltage-splitting resistors as shown in page 121. If it is not used, connect to NC.
8	AVSS	A	G	Analog ground pin.
9	DVSS	D	G	Digital ground pin.
10	PVDD1	P1	P	I/O power supply pin.
11	DATA_A0	P1	O (I)	A block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
12	DATA_A1	P1	O (I)	A block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
13	DATA_A2	P1	O (I)	A block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
14	DATA_A3	P1	O (I)	A block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
15	DATA_A4	P1	O (I)	A block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
16	DATA_A5	P1	O (I)	A block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
17	DVDD	D	P	Digital power supply pin.
18	DVSS	D	G	Digital ground pin.
19	PVDD1	P1	P	I/O power supply pin.
20	DATA_A6	P1	O (I)	A block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.

Pin No.	Symbol	P/S[1]	I/O[2]	Functional Description
21	DATA_A7	P1	O (I)	A block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
22	VD_ACT_A	P1	O (I)	A block VD(Vertical Drive) / VACT(Vertical Active) signal output pin. VD signal output / VACT signal output can be selected by register setting. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
23	HD_ACT_A	P1	O (I)	A block HD(Horizontal Drive) / HACT(Horizontal Active) signal output pin. HD signal output / HACT signal output can be selected by register setting. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
24	DVALID_A	P1	O (I)	A block DVALID signal output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
25	FIELD_A	P1	O (I)	A block FIELD signal output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
26	PVDD1	P1	P	I/O power supply pin.
27	DTCLK	P1	O	Data clock output pin. Approx. 27 MHz clock output. See Table below for relation of output to OE_A, OE_B, PDN and RSTN pin status.
28	FIELD_B	P1	O (I)	B block FIELD signal output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
29	DVALID_B	P1	O (I)	B block DVALID signal output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
30	HD_ACT_B	P1	O (I)	B block HD(Horizontal Drive) / HACT(Horizontal Active) signal output pin. HD signal output / HACT signal output can be selected by register setting. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
31	VD_ACT_B	P1	O (I)	B block VD(Vertical Drive) / VACT(Vertical Active) signal output pin. VD signal output / VACT signal output can be selected by register setting. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.

Pin No.	Symbol	P/S[1]	I/O[2]	Functional Description
32	DATA_B7	P1	O (I)	B block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
33	DVSS	D	G	Digital ground pin.
34	PVDD1	P1	P	I/O power supply pin.
35	DATA_B6	P1	O (I)	B block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
36	DATA_B5	P1	O (I)	B block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
37	DATA_B4	P1	O (I)	B block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
38	DATA_B3	P1	O (I)	B block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
39	DATA_B2	P1	O (I)	B block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
40	DATA_B1	P1	O (I)	B block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
41	DATA_B0	P1	O (I)	B block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
42	PVDD1	P1	P	I/O power supply pin.
43	DVSS	D	G	Digital ground pin.
44	DVDD	D	P	Digital power supply pin.
45	TEST0	P2	I	Pin for test mode setting. Connect to DVSS.
46	TEST1	P2	I	Pin for test mode setting. Connect to DVSS.
47	NSIG_B	P2	O (I)	Shows status of synchronization with input signal of B block. Low: Signal present (synchronized). High: Signal not present or not synchronized. See Table below for relation of output to OE_B, PDN, RSTN pin status.
48	NSIG_A	P2	O (I)	Shows status of synchronization with input signal of A block. Low: Signal present (synchronized). High: Signal not present or not synchronized. See Table below for relation of output to OE_A, PDN, RSTN pin status.

Pin No.	Symbol	P/S[1]	I/O[2]	Functional Description
49	OE_B	P2	I	B block Output Enable pin. L: Digital output pin in Hi-z output mode. H: Data output mode. Hi-z input to OE_B pin is prohibited.
50	OE_A	P2	I	A block Output Enable pin. L: Digital output pin in Hi-z output mode. H: Data output mode. Hi-z input to OE_A pin is prohibited.
51	PVDD2	P2	P	Microprocessor I/F power supply pin.
52	RSTN	P2	I	Reset signal input pin. Hi-z input is prohibited. L: Reset. H: Normal operation.
53	PDN	P2	I	Power-down control pin. Hi-z input is prohibited. L: Power-down. H: Normal operation.
54	SDA	P2	I/O	I^2C data pin. Connect to PVDD2 via a pull-up register. Hi-z input possible when RSTN=L. Will not accept SDA input during reset sequence.
55	SCL	P2	I	I^2C clock input pin. Use PVDD2 or lower for input. Hi-z input possible when PDN=L. Will not accept SCL input during reset sequence.
56	SELA	P2	I (O)	I^2C bus address selector pin. PVDD2 connection: Slave address [0x8A] DVSS connection: Slave address [0x88]
57	AVDD	A	P	Analog power supply pin.
58	XTO	A	O	Crystal connection pin. Connect to digital ground via 22 pF capacitor as shown in Sec. 10. Use 24.576 MHz crystal. When PDN=L, output level is DVSS. If crystal is not used, connect to NC or DVSS.
59	AVSS	A	G	Analog ground pin.
60	XTI	A	I	Crystal connection pin. Connect to digital ground via 22 pF capacitor as shown in Sec. 10. Use 24.576 MHz crystal resonator. For input from 24.576 MHz crystal oscillator, use this pin.
61	VRN	A	O	Internal reference negative voltage pin for AD converter. Connect to AVSS via ≥0.1 μF ceramic capacitor.
62	IREF	A	O	Reference current setting pin. Connect to ground via 6.8 kΩ (≤1% accuracy) resistor.

Pin No.	Symbol	P/S[1]	I/O[2]	Functional Description
63	VRP	A	O	Internal reference positive voltage pin for AD converter. Connect to AVSS via ≥0.1 μF ceramic capacitor.
64	VCOM	A	O	Common internal voltage for AD convertor. Connect to AVSS via ≥0.1 μF ceramic capacitor.

[1]Power supply A: AVDD, D: DVDD, P1: PVDD1, P2: PVDD2

[2]Input/Output O: output pin, I: intput pin, I/O:input/output pin, P: power supply pin,G:ground connection pin.

Output pin status as determined by OE_A, OE_B, PDN, and RSTN pin status.

OE_A, OE_B (*2)	PDN	RSTN	Output1 (*2)	Output2 (*2)
L	x	x	Hi-Z output	L output
H	L	x	L output	L output
H	H	L	L output	L output
		H	Default Data Out (*3)	Default Data Out (*3)

[2]Output1:

(A Block) DATA_A[7:0], HD_ACT_A, VD_ACT_A, DVALID_A, FIELD_A

(B Block) DATA_B[7:0], HD_ACT_B, VD_ACT_B, DVALID_B, FIELD_B

DTCLK.

If OE_A and OE_B both are in Low condition, the DTCLK pin output is Hi-Z.

Output2: NSIG_A, NSIG_B

If (OE_A=H or OE_B=H) and PDN=H just after power is turned on, output pin status will be indefinite until internal state is determined by reset sequence.

[3]In the absence of AIN signal input, output will be black data ((Y=0x10, Cb/Cr=0x80).
(Blueback output can be obtained by register setting.)

4.Electrical specifications

(1) Absolute maximum ratings

Parameter	Min	Max	Units	Notes
Supply voltage AVDD, DVDD, PVDD1, PCDD2	 −0.3 −0.3	 2.2 4.2	 V V	
Analog input pin voltage A (VinA)	−0.3	AVDD + 0.3 (≤2.2)	V	
Digital output pin voltage P1 (VioP1)	−0.3	PVDD1 + 0.3 (≤4.2)	V	(*1)
Digital output pin voltage P2 (VioP2)	−0.3	PVDD2 + 0.3 (≤4.2)	V	(*2)
Input pin current (Iin) (except for power supply pin)	−10	10	mA	
Storage temperature	−40	125	ºC	

*The above supply voltages are referenced to ground pins (DVSS=AVSS) at 0 V (the Reference Voltage).

All power supply grounds (AVSS, DVSS) should be at the same electric potential.

If digital output pins are connected to data bus, the data bus operating voltage should be in the same range as shown above for the digital output pin.

(*1) DATA_A[7:0], HD_ACT_A, VD_ACT_A, DVALID_A, FIELD_A,
DATA_B[7:0], HD_ACT_B, VD_ACT_B, DVALID_B, FIELD_B, DTCLK.

(*2) OE_A, OE_B, SELA, PDN, RSTN, SDA, SCL, NSIG_A, NSIG_B, TEST0, TEST1.

(2) Recommended operating conditions

Parameter	Min	Typ	Max	Units	Condition
Analog supply voltage (AVDD) Digital supply voltage (DVDD)	1.70	1.80	2.00	V	AVDD=DVDD
I/O supply voltage (PVDD1) MPU I/F supply voltage (PVDD2)	1.70	1.80	3.60	V	PVDD1≥DVDD PVDD2≥DVDD
Operating temp. (Ta)	−40		85	ºC	

The above supply voltages are referenced to ground pins (DVSS=AVSS) at 0 V (the Reference Voltage).

All power supply grounds (AVSS, DVSS) should be at the same electric potential.

(3) DC characteristics

Where no specific condition is indicated in the following table, the supply voltage range is the same as that shown for the recommended operating conditions in 4-2 above.

Parameter	Symbol	Min	Typ	Max	Units	Condition
Digital P2 input high voltage	VPIH	0.8PVDD2			V	Case *1
		0.7PVDD2			V	Case *2
Digital P2 input low voltage	VPIL			0.2PVDD2	V	Case *1
				0.3PVDD2	V	Case *2
Digital input leak current	IL			±10	uA	
Digital P1 output high voltage	VP1OH	0.8PVDD1			V	IOH = -600uA
Digital P1 output low voltage	VP1OL			0.2PVDD1	V	IOL = 1mA
Digital P2 output high voltage	VP2OH	0.8PVDD2			V	IOH = -600uA
Digital P2 output low voltage	VP2OL			0.2PVDD2	V	IOL = 1mA
I^2C (SDA)L output	VOLC			0.4 0.2 PVDD2	V	IOLC = 3mA PVDD2≥2.0V PVDD2<2.0V

*1: < DVDD = 1.70V~2.00V, DVDD≤PVDD1<2.70V, DVDD≤PVDD2<2.70V, Ta: -40~85˚C >

*2: < DVDD = 1.70V~2.00V, 2.70V≤PVDD1≤3.60V, 2.70V≤PVDD2≤3.60V, Ta: -40~85˚C >

Definition of above input/output terms

Digital P2 input : Collective term for SDA, SCL, SELA, OE_A, OE_B, PDN, RSTN, TEST0, TEST1 pin inputs.

Digital P1 output : Collective term for DATA_A[7:0], HD_ACT_A, VD_ACT_A, DVALID_A, FIELD_A, DATA_B[7:0], HD_ACT_B, VD_ACT_B, DVALID_B, FIELD_B, DTCLK pin outputs.

Digital P2 output : Collective term for NSIG_A, NSIG_B pin outputs.

SDA pin output: Not termed digital pin output unless otherwise specifically stated.

(4) Analog characteristics (AVDD=1.8V, Temp.25˚C)

Selector clamp

Parameter	Symbol	Min	Typ	Max	Units	Condition
Maximum input range	VIMX	0	0.50	0.60	V_{PP}	ADC output data is fullcode when input range is 0.6Vpp input.

AD converter

Parameter	Symbol	Min	Typ	Max	Units	Condition
Resolution	RES		11		bit	
Operating clock frequency	FS		27		MHz	ADC:54MHz
Integral nonlinearity	INL		±2.0	+4.0 -4.0	LSB	FS=27MHz, Input range = 0.5Vpp
Differential nonlinearity	DNL		±0.5	+1.5 -1.0	LSB	FS=27MHz, Input range = 0.5Vpp
S/N	SN		54		dB	Fin=1MHz*, FS=27MHz, Input range = 0.5Vpp
S/(N+D)	SND		52		dB	
ADC internal common voltage	VCOM		0.96		V	
ADC internal positive VREF	VRP		1.28		V	
ADC internal negative VREF	VRN		0.64		V	

*Fin = AIN input signal frequency

AAF (Anti-Aliasing Filter)

Parameter	Symbol	Min	Typ	Max	Units	Condition
Pass band ripple	Gp	-1		+1	dB	6MHz
Stop band blocking	Gs	20	35		dB	27MHz

(5) Current consumption (at DVDD = AVDD = PVDD1 = PVDD2 = 1.8V, Ta = −40 ~ 85˚C) (*1)

Parameter	Symbol	Min	Typ	Max	Units	Condition
(Active mode)						
Total	IDD1		86	130	mA	CVBS : 2ch
	IDD2		63		mA	CVBS : 1ch (*2)
	IDD3		75	112	mA	S-Video (*2)
Analog block	AIDD		39		mA	CVBS : 2ch With Xtal crystal connected.
Digital block	DIDD		34		mA	CVBS : 2ch
I/O block	PIDD		13		mA	Load condition: CL=12pF, 24pF* (*DTCLK pin)
(Power down mode)						PDN=L(DVSS) (*3)
Total	SIDD		≤ 1	20	uA	
Analog block	ASIDD		≤ 1		uA	
Digital block	DSIDD		≤ 1		uA	
I/O block	PSIDD		≤ 1		uA	

(*1) With NTSC-J 100% color bar input.

(*2) Reference Value. During A Block is set to output, B Block is set to [No Decode].

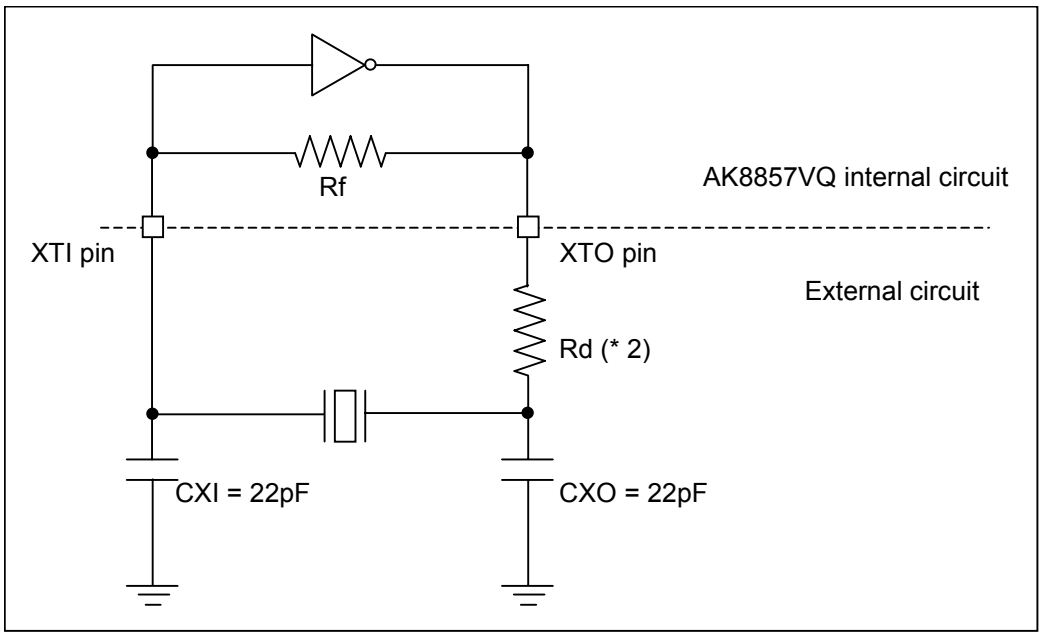
(*3)To perform power-down, OE_A, OE_B and RSTN pins must always be brought to the voltage polarity to be used or to ground level.

(6) **Crystal circuit block** (Ta : -40~85˚C)

Parameter	Symbol	Min	Typ	Max	Units	Condition
Frequency	f_0		27		MHz	
Frequency tolerance	Δf / f			±100	ppm	
Load capacitance	CL		15		pF	
Effective equivalent resistance	Re			100	Ω	(*1)
Crystal parallel capacitance	CO		0.9		pF	
XTI terminal external connection load capacitance	CXI		22		pF	CL=15pF
XTO terminal external connection load capacitance	CXO		22		pF	CL=15pF

(*1) Effective equivalent resistance generally may be taken as $Re = R1 \times (1+CO/CL)^2$, where R1 is the crystal series equivalent resistance.

Example connection



(*2) Determine need for and appropriate value of limiting resistance (Rd) in accordance with the crystal specifications.

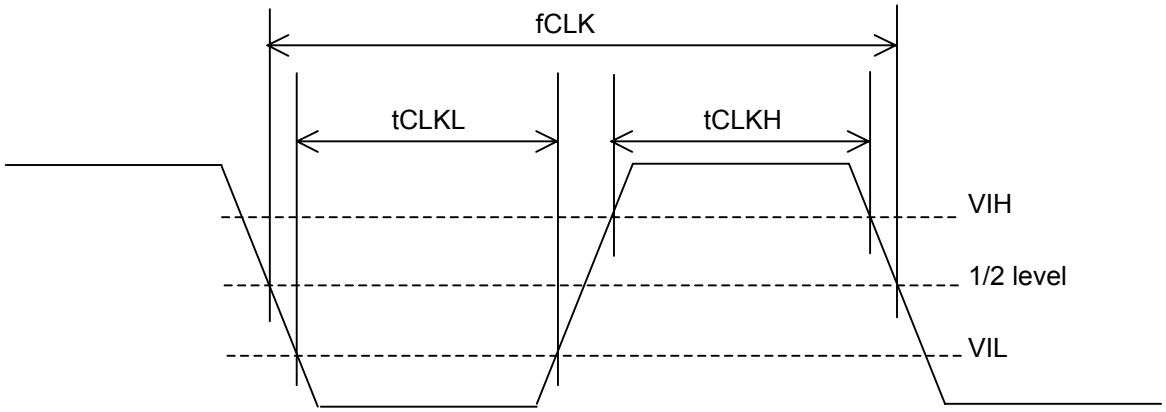
AK8857VQ is hereafter the “AK8857”.

5. **AC Timing**

(DVDD=1.70V~2.00V, PVDD1=DVDD~3.60V, PVDD2=DVDD~3.60V, -40~85˚C)
Load condition: CL=12pF, 24pF(DTCLK pin)

(1) Clock Input

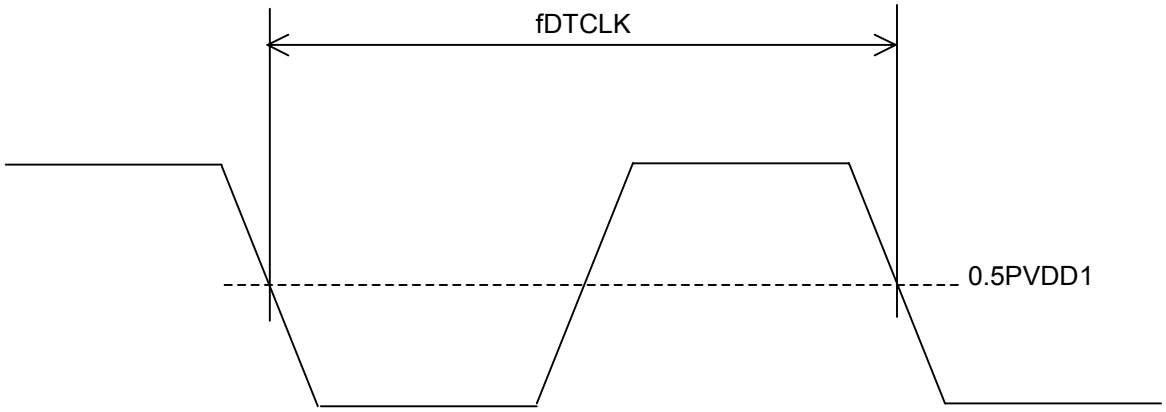
Set AK8857 clock input as follows.



Parameter	Symbol	Min	Typ	Max	Units
Input CLK	fCLK		27		MHz
CLK pulse width H	tCLKH	15			nsec
CLK pulse width L	tCLKL	15			nsec
Frequency tolerance				±100	ppm

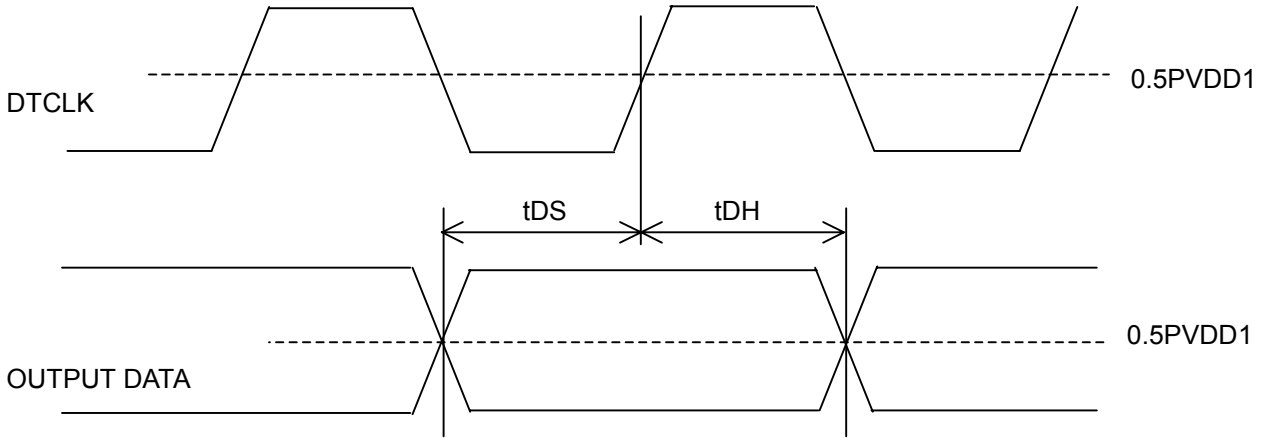
(2) Clock Output (DTCLK output)

Parameter	Symbol	Min	Typ	Max	Units	Output Data Format
DTCLK	fDTCLK		54		MHz	601,VGA, WVGA progressive output.
			27			601,VGA, WVGA other than progressive output.



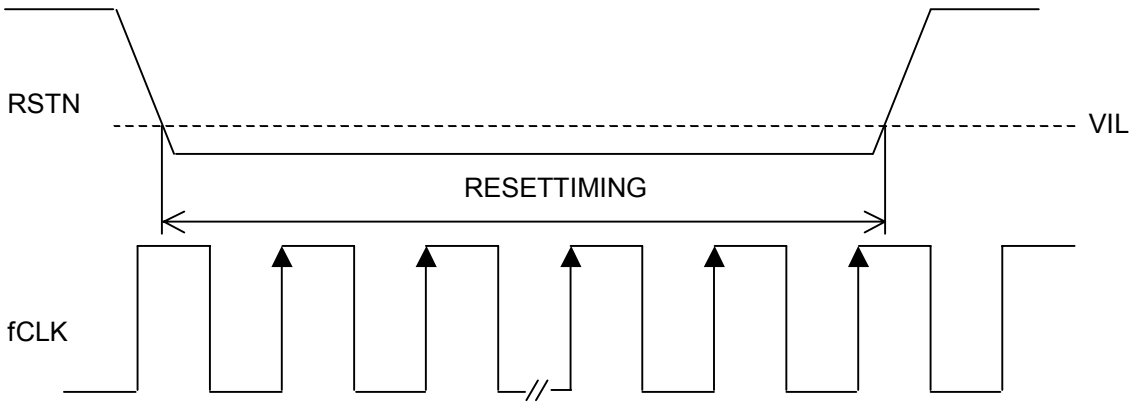
(3) Output Data Timing

DATA_A[7:0], HD_ACT_A, VD_ACT_A, FIELD_A, DVALID_A, DATA_A[7:0], HD_ACT_A, VD_ACT_A, FIELD_A, DVALID_A



Parameter	Symbol	Min	Typ	Max	Units	DTCLK
Output Data Setup Time	tDS	10			nsec	27MHz
		5			nsec	54MHz
Output Data Hold Time	tDH	10			nsec	27MHz
		5			nsec	54MHz

(4) Register reset timing

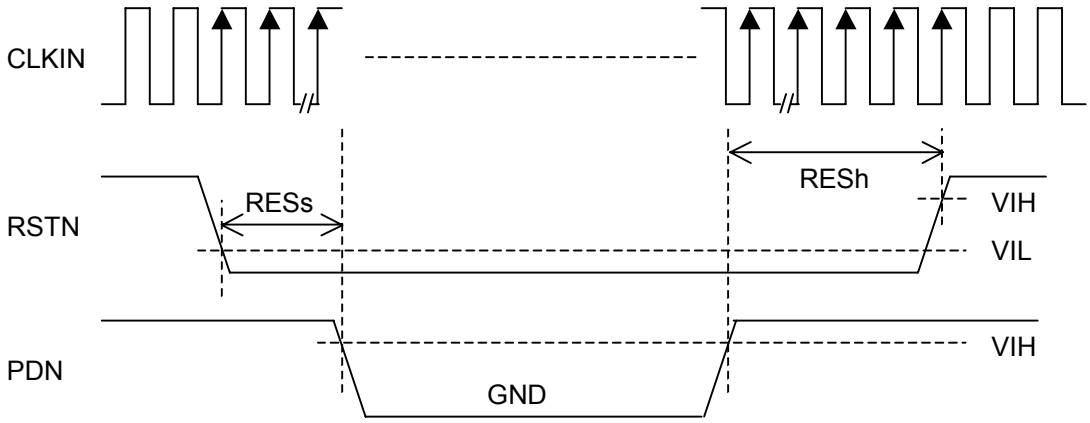


Parameter	Symbol	Min	Typ	Max	Units	Notes
RSTN pulse width	RESETTIMING	100 (3.7)			CLK (usec)	Based on clock leading edge

Note. Clock input is necessary for reset operation.
RSTN pin must be pulled low following clock application.

(5) **Power-down sequence and Reset sequence after power-down**

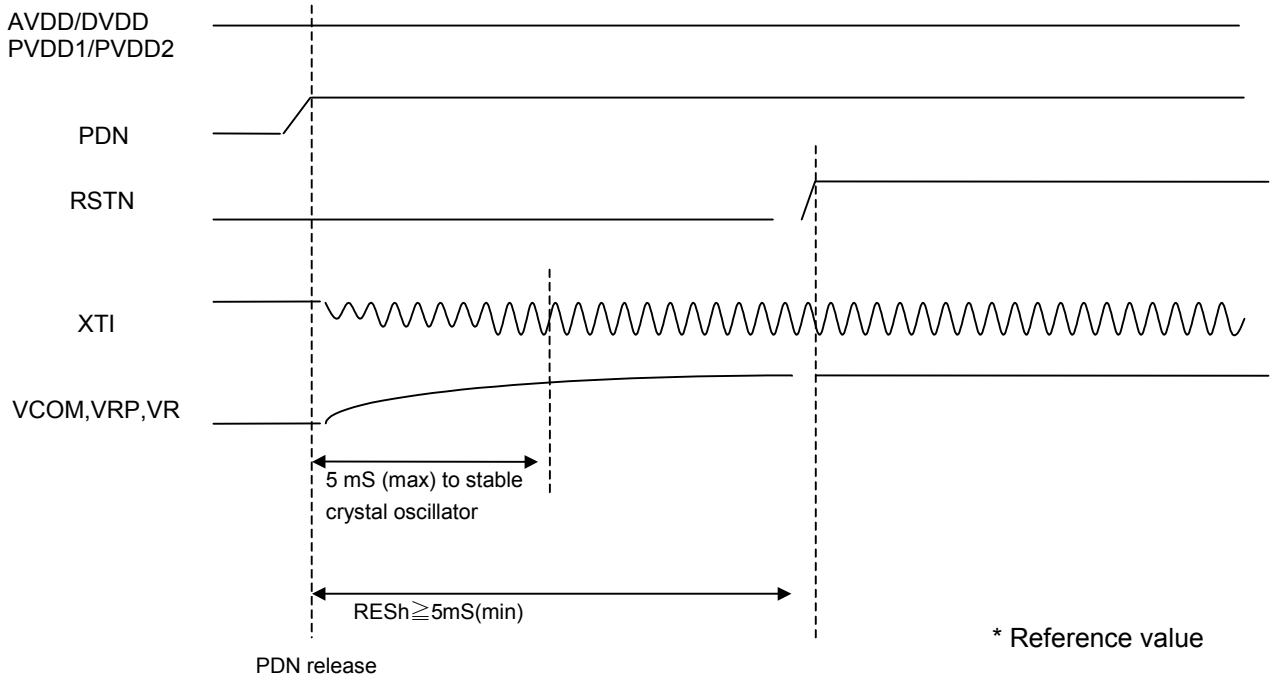
Reset must be applied for at least 2048 clock cycles (or 83.33 μs) before setting PDN (PDN=Low).
Reset must be applied for at least 5 ms after PDN release (PDN=Hi).



Parameter	Symbol	Min	Typ	Max	Units
Reset width before setting PDN	RESs	2048 (75.85)			CLK (usec)
Reset width after PDN release	RESh	5			msec

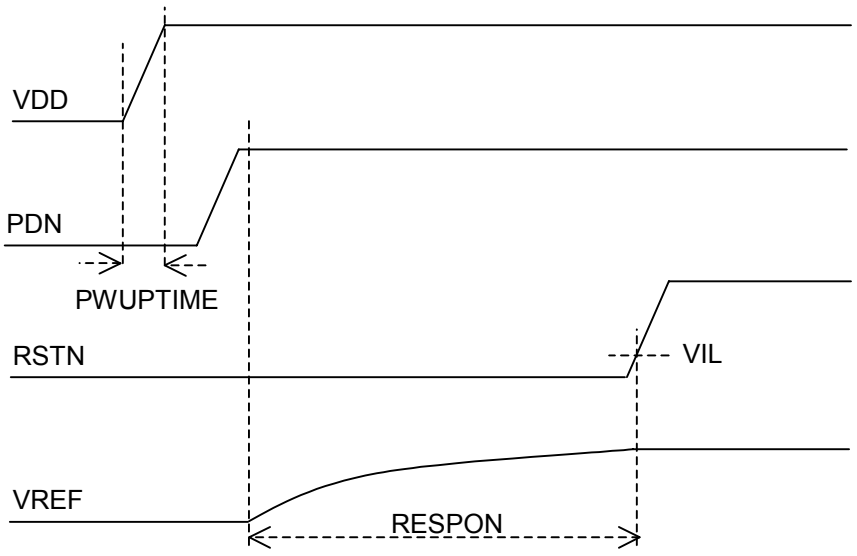
To perform power-down, all control signals must always be brought to the voltage polarity to be used or to ground level.
For any power supply removal, all power supplies must be removed.
Clock input is necessary for resetting.

The power-down sequence for connection of the crystal is as follows.



(6) Power-on reset

At power-on, reset must be applied until the analog reference voltage and current have stabilized.[1] (*1) The order of each power supply to be start up is not required. All the power supply must be on within 100msec during PDN pin status is low.



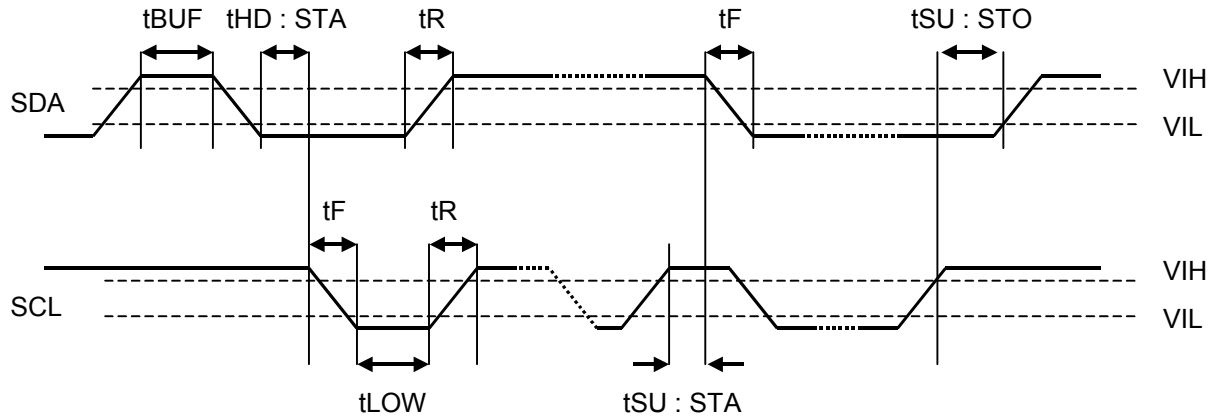
Parameter	Symbol	Min	Typ	Max	Units
POWERUP TIME	PWUPTIME			100	msec
RSTN pulse width	RESPON	5			msec

[1]Clock input is necessary for resetting.

(7) I²C bus input timing

(DVDD=1.70V~2.00V, PVDD1=DVDD~3.60V, PVDD2=DVDD~3.60V, -40~85˚C)

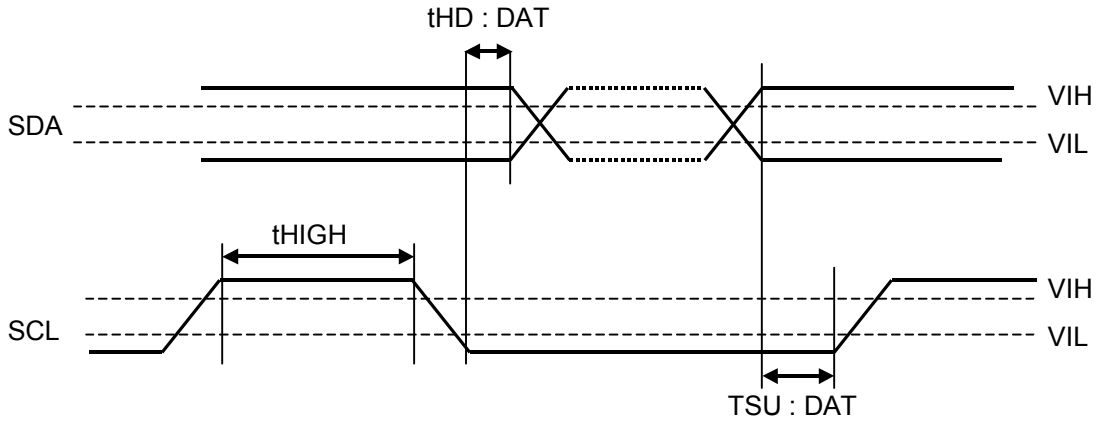
(7-1) Timing 1



Parameter	Symbol	Min	Max	Units
Bus Free Time	tBUF	1.3		Usec
Hold Time (Start Condition)	tHD:STA	0.6		Usec
Clock Pulse Low Time	tLOW	1.3		Usec
Input Signal Rise Time	tR		300	Nsec
Input Signal Fall Time	tF		300	Nsec
Setup Time(Start Condition)	tSU:STA	0.6		Usec
Setup Time(Stop Condition)	tSU:STO	0.6		Usec

Note. The timing relating to the I²C bus is as stipulated by the I²C bus specification, and not determined by the device itself. For details, see I²C bus specification.

(7-2) Timing 2



Parameter	Symbol	Min	Max	Units
Data Setup Time	tSU:DAT	100[1]		nsec
Data Hold Time	tHD:DAT	0.0	0.9[2]	usec
Clock Pulse High Time	tHIGH	0.6		usec

[1] If I²C is used in standard mode, tSU: DAT ≥ 250 ns is required.

[2] This condition must be met if the AK8854 is used with a bus that does not extend tLOW (to use tLOW at minimum specification).

6. Functional description

Analog interface

The AK8857 accepts composite video signal (CVBS), S-video input with 4 input pins available for this purpose.

The decode signal is selected via the register (AINSEL[4:0]).

The AK8857 can decode 2ch of anolog video signal at the same time during composite video signal input. The digital output data is output to A block and B block output block. It is possible to switch the digital output data between A block and B block output block. It also possible to select one of digital output data to be output at A block and B block output at the same time.

	Definition
Analog Input Select	A block and B block output video signal selection : [AINSEL4: AINSEL0] [00000]: [A]: AIN1 (CVBS), [B]: AIN4(CVBS) [00001]: [A]: AIN1 (CVBS), [B]: AIN3(CVBS) [00010]: [A]: AIN1 (CVBS), [B]: AIN2(CVBS) [00011]: [A]: AIN1 (CVBS), [B]: AIN1(CVBS) [00100]: [A]: AIN1 (CVBS), [B]: Non-decode [00101]: [A]: AIN2 (CVBS), [B]: AIN4(CVBS) [00110]: [A]: AIN2 (CVBS), [B]: AIN3(CVBS) [00111]: [A]: AIN2 (CVBS), [B]: AIN2(CVBS) [01000]: [A]: AIN2 (CVBS), [B]: AIN1(CVBS) [01001]: [A]: AIN2 (CVBS), [B]: Non-decode [01010]: [A]: AIN3 (CVBS), [B]: AIN4(CVBS) [01011]: [A]: AIN3 (CVBS), [B]: AIN3(CVBS) [01100]: [A]: AIN3 (CVBS), [B]: AIN2(CVBS) [01101]: [A]: AIN3 (CVBS), [B]: AIN1(CVBS) [01110]: [A]: AIN3 (CVBS), [B]: Non-decode [01111]: [A]: AIN4 (CVBS), [B]: AIN4(CVBS) [10000]: [A]: AIN4(CVBS), [B]: AIN3(CVBS) [10001]: [A]: AIN4 (CVBS), [B]: AIN2(CVBS) [10010]: [A]: AIN4 (CVBS), [B]: AIN1(CVBS) [10011]: [A]: AIN4 (CVBS), [B]: Non-decode [10100]: [A]: Non-decode, [B]: AIN4 (CVBS) [10101]: [A]: Non-decode, [B]: AIN3(CVBS) [10110]: [A]: Non-decode, [B]: AIN2(CVBS) [10111]: [A]: Non-decode, [B]: AIN1(CVBS) [11000]: [A]: AIN1(Y) / AIN3(C), [B]: Non-decode [11001]: [A]: AIN1(Y) / AIN3(C), [B]: AIN1(Y) / AIN3(C) [11010]: [A]: AIN2(Y) / AIN4(C), [B]: Non-decode [11011]: [A]: AIN2(Y) / AIN4(C), [B]: AIN2(Y) / AIN4(C) [11100]: [A]: Non-decode, [B]: AIN1(Y) / AIN3(C) [11101]: [A]: Non-decode, [B]: AIN2(Y) / AIN4(C)

The output block change to power-save mode when [Non-decode] is selected and digital circuit operational is stoped. This will low down the internal power consumption.

The data output is low during this state.

Available pin : DATA_A[7:0], HD_ACT_A, VD_ACT_A, DVALID_A, FIELD_A, DATA_B[7:0], HD_ACT_B, VD_ACT_B, DVALID_B, FIELD_B, NSIG_A, NSIG_B pins.

Note: Output control via pins OE_A, OE_B, PDN, and RSTN takes priority, regardless of the above settings.

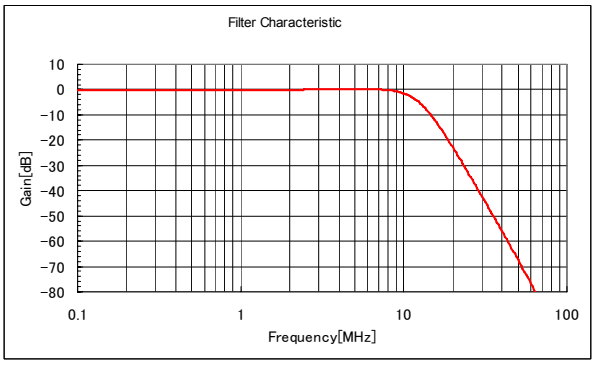
Analog band limiting filter and analog clamp circuit

Analog band limiting filter

The characteristics of the AK8857 internal analog band limiting filter (anti-aliasing), which is in front of the AD converter input, are as follows:

±1dB (~6MHz)

−35dB (27MHz)….Typical value



Analog clamp circuit

In AK8857, the input video signal is clamping with analog circuit.

The clamping method is show as follows.

[CVBS signal decoding]

AK8857 clamps the input signal to sync tip. (analog sync tip clamp)

The clamp timing pulse, with its origin at the falling edge of the internally synchronized and separated sync signal, is generated at approximately the central position of the sync signal.

[S-video signal decoding]

(Y signal)

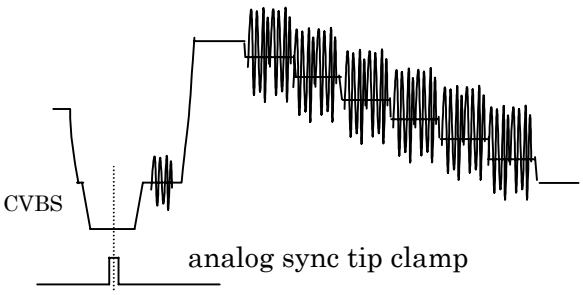
AK8857 clamps the Y signal to sync tip. (analog sync tip clamp)

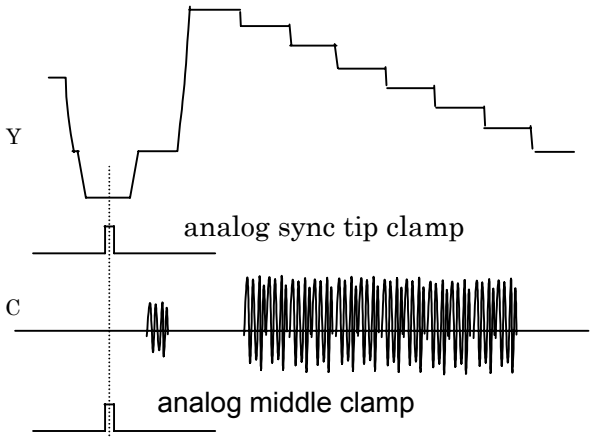
The clamp timing pulse, with its origin at the falling edge of the internally synchronized and separated sync signal, is generated at approximately the central position of the sync signal.

(C signal)

AK8857 clamps the C signal to the middle level. (analog middle clamp)

The clamp timing pulse is generated at same timing with Y signal.





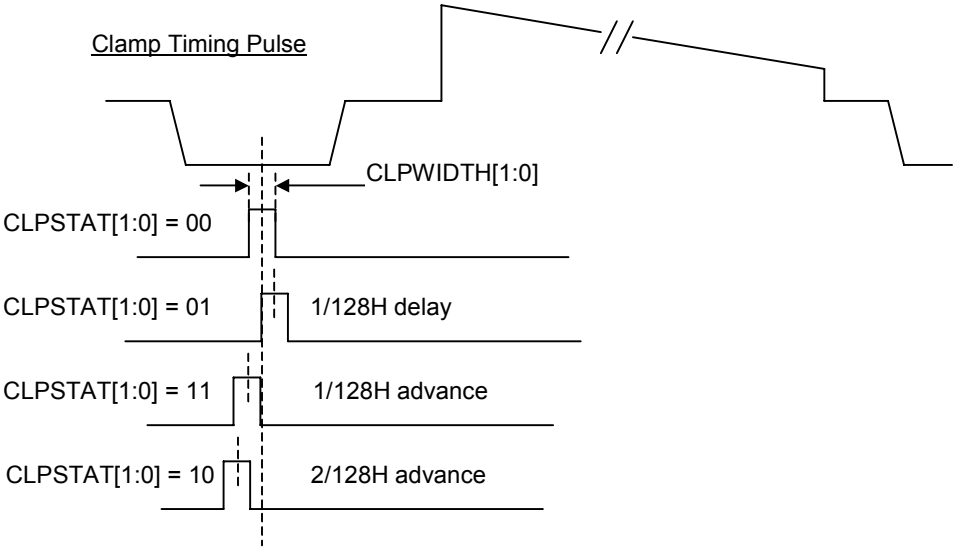
Additionary, the AK8857 can change the position, width and current value of clamp pulse by registers.

○CLPWIDTH[1:0]: Set the width of clamp pulse.

CLPWIDTH[1:0]-bit	Clamp width	Notes
[00]	296nsec	
[01]	593nsec	
[10]	1.1usec	
[11]	2.2usec	

○CLPSTAT[1:0]: Set the position of clamp pulse.

CLPSTAT[1:0]-bit	Clamp position	Notes
[00]	Sync tip/ middle/ bottom clamp: Centor of horizontal sync	The positions of all clamp pulse are changed.
[01]	(1/128) H delay.	
[10]	(2/128) H advance	
[11]	(1/128) H advance	



○CLPG[1:0] : Set the current value of fine clamp in analog block.

CLPG[1:0]-bit	Clamp current value	Notes
[00]	Min.	Middle 1 = (Min. x 3) Middle 2 = (Min. x 5) Max. = (Min. x 7)
[01]	Middle 1 (Default)	
[10]	Middle 2	
[11]	Max.	

○UDG[1:0]: Set the current value of rough clamp in analog block.

UDG[1:0]-bit	Clamp current value	Notes
[00]	Min. (Default)	Middle 1 = (Min. x 2) Middle 2 = (Min. x 3) Max. = (Min. x 4)
[01]	Middle 1	
[10]	Middle 2	
[11]	Max.	

Its digital circuit clamps the digitized input data to the pedestal level (digital pedestal clamp), and will be described later.

Output Data Format Setting (Pixel size / progressive output)

The AK8857 can convert the output pixel size from the original input pixel size.
The AK8857 also can convert the interlaced input signal to progressive output signal.

The AK8857 supported output format is shown below

Input signal	Output pixel size	Interlace / Progressive output	Output Clock	Notes
525 Line NTSC-M, J, NTSC-4.43, PAL-M, PAL-60	720x487 (ITU-R BT.601)	Interlace	27MHz	
		Progressive	54MHz	(*1)
	800x480 (WVGA)	Interlace	27MHz	
		Progressive	54MHz	(*1)
	640x480 (VGA)	Interlace	27MHz	
		Progressive	54MHz	(*1)
	400x240 (WQVGA)	Progressive	27MHz	(*2)
	320x240 (QVGA)	Progressive	27MHz	(*2)
	400x234(EGA)	Progressive	27MHz	(*2)
	480x240(WEGA1)	Progressive	27MHz	(*2)
	480x234(WEGA2)	Progressive	27MHz	(*2)
625 Line PAL-B,D,G,H,I,N, PAL-Nc SECAM	720x576 (ITU-R BT.601)	Interlace	27MHz	
		Progressive	54MHz	(*1)
	800x480 (WVGA)	Interlace	27MHz	
		Progressive	54MHz	(*1)
	640x480 (VGA)	Interlace	27MHz	
		Progressive	54MHz	(*1)
	400x240 (WQVGA)	Progressive	27MHz	(*2)
	320x240 (QVGA)	Progressive	27MHz	(*2)
	400x234(EGA)	Progressive	27MHz	(*2)
	480x240(WEGA1)	Progressive	27MHz	(*2)
	480x234(WEGA2)	Progressive	27MHz	(*2)

(*1) Interlcae signal to progressive signal conversion is using line repeating process.
The Frame rates for progressive output signal is selectable between 30frm/sec* and 60frm/sec*.
(*2) Only progressive output is support for this section.

It's not mentioned here, during the pixel size conversion the data is interpolar before being generated at the output.

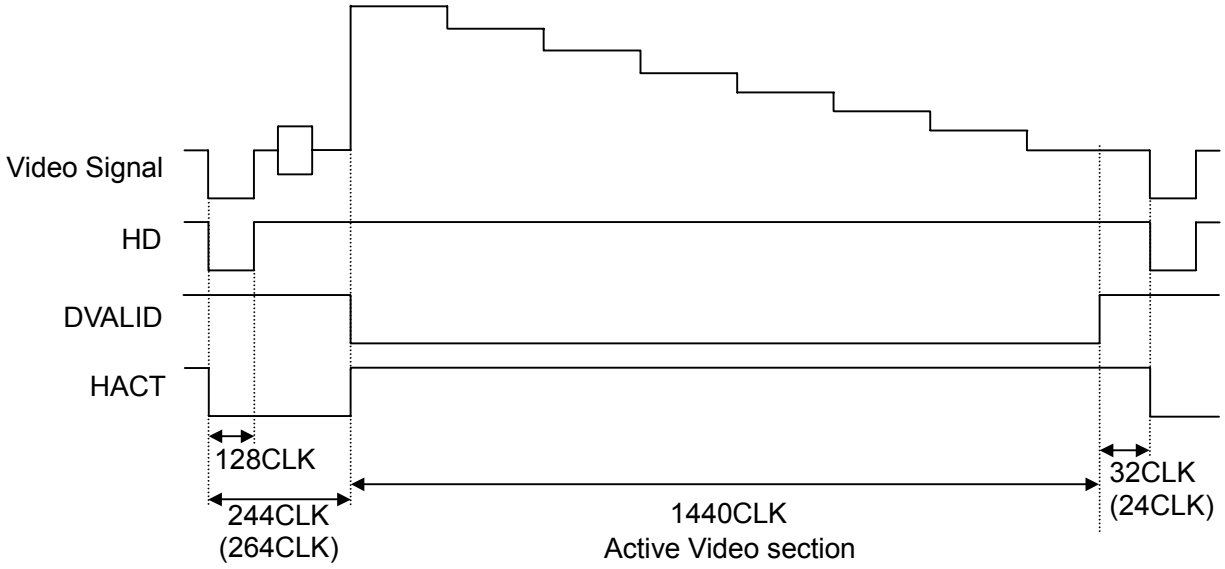
If the input signal quality is poor, there is a case where it cannot satisfy the timing diagram shown below.
Example: If the input signal line is shortened than the normal, it will effect EAV sync signal and HD signal timing for the next line and for that reason the output signal will be effected as well.

*frm/sec: Frame number in 1 sec

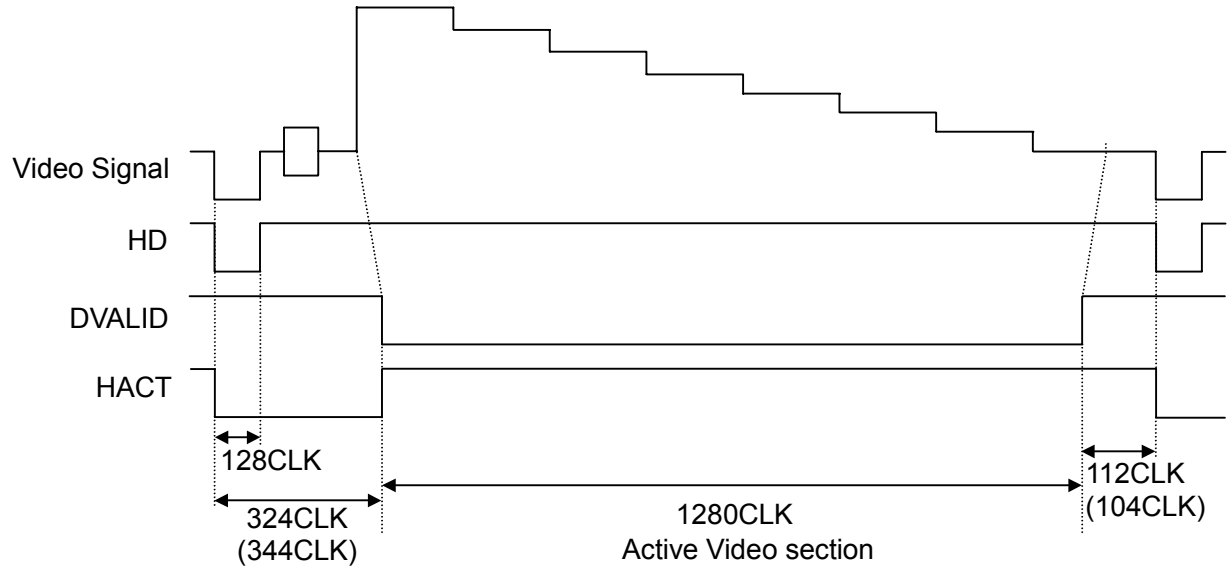
The figure below shows the relationship between 1-line data pixel and sync signal timing for each output pixel size.

*() in the figure below refers to clock pixels of 625-line input.
*Because the data is sampling to a fixed-clock, the cycle period from end of active signal to the next line of horizontal sync signal is fixed is not guarantee.

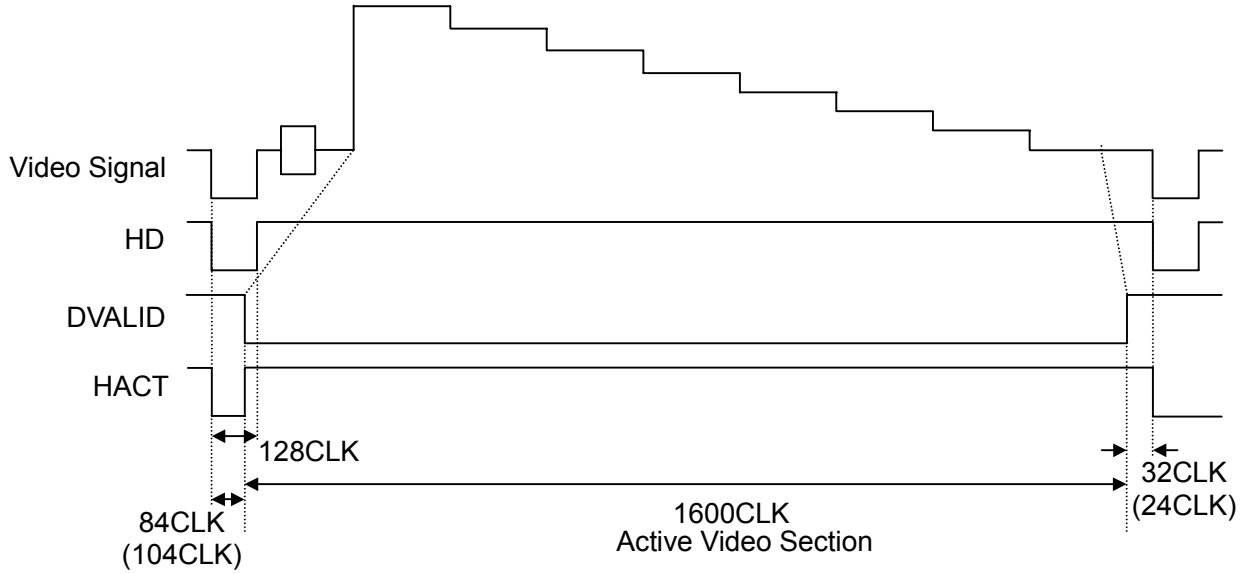
○720x487, 720x576(ITU-R BT.601)



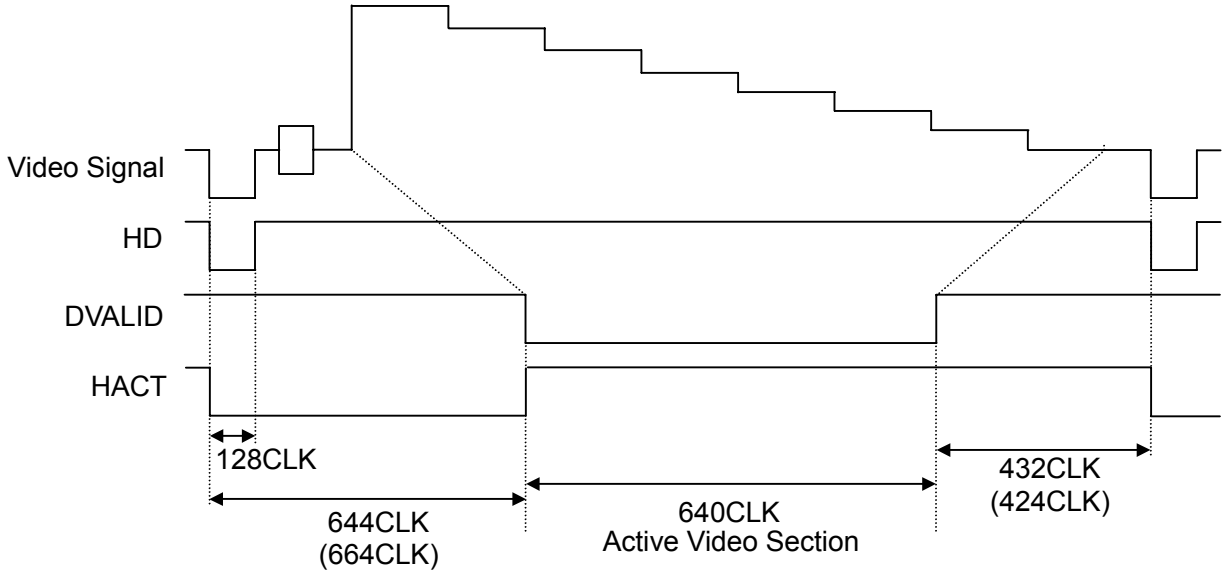
○640x480(VGA)



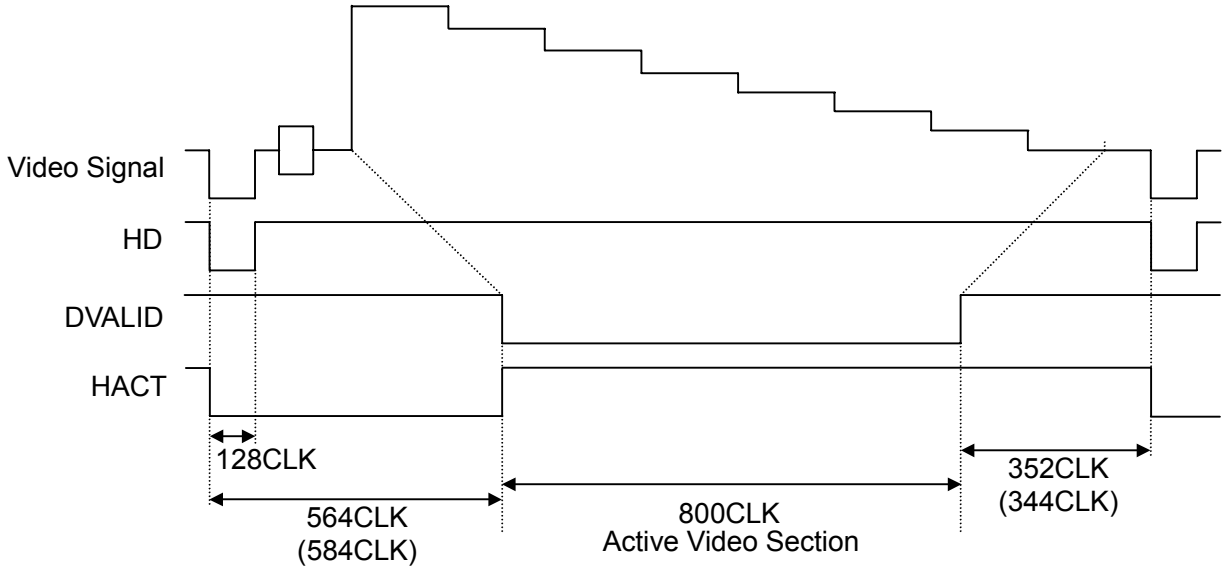
○800x480(WVGA)



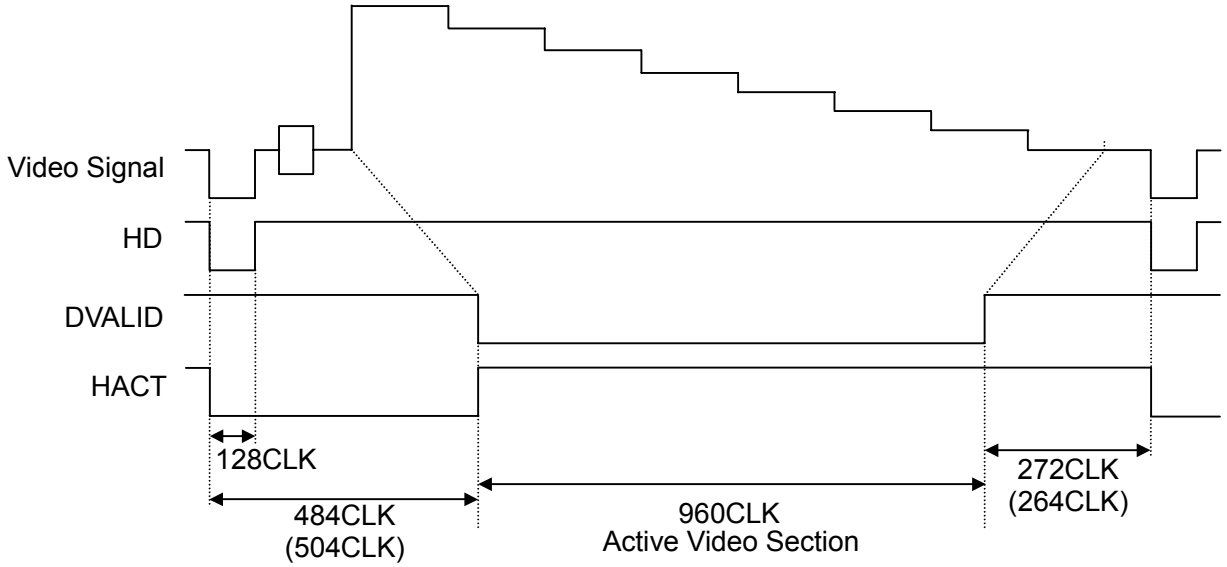
○320x240(QVGA)



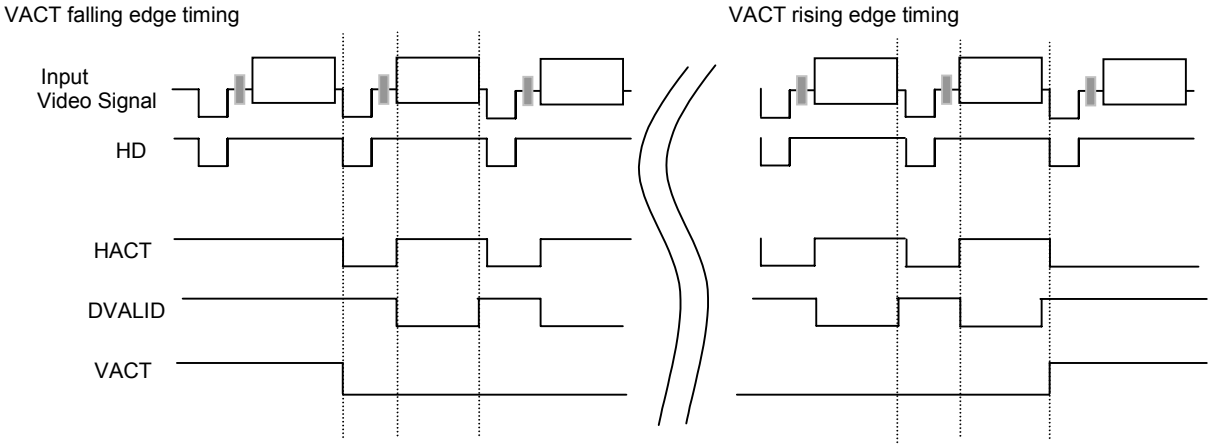
○400x240(WQVGA), 400x234(EGA)



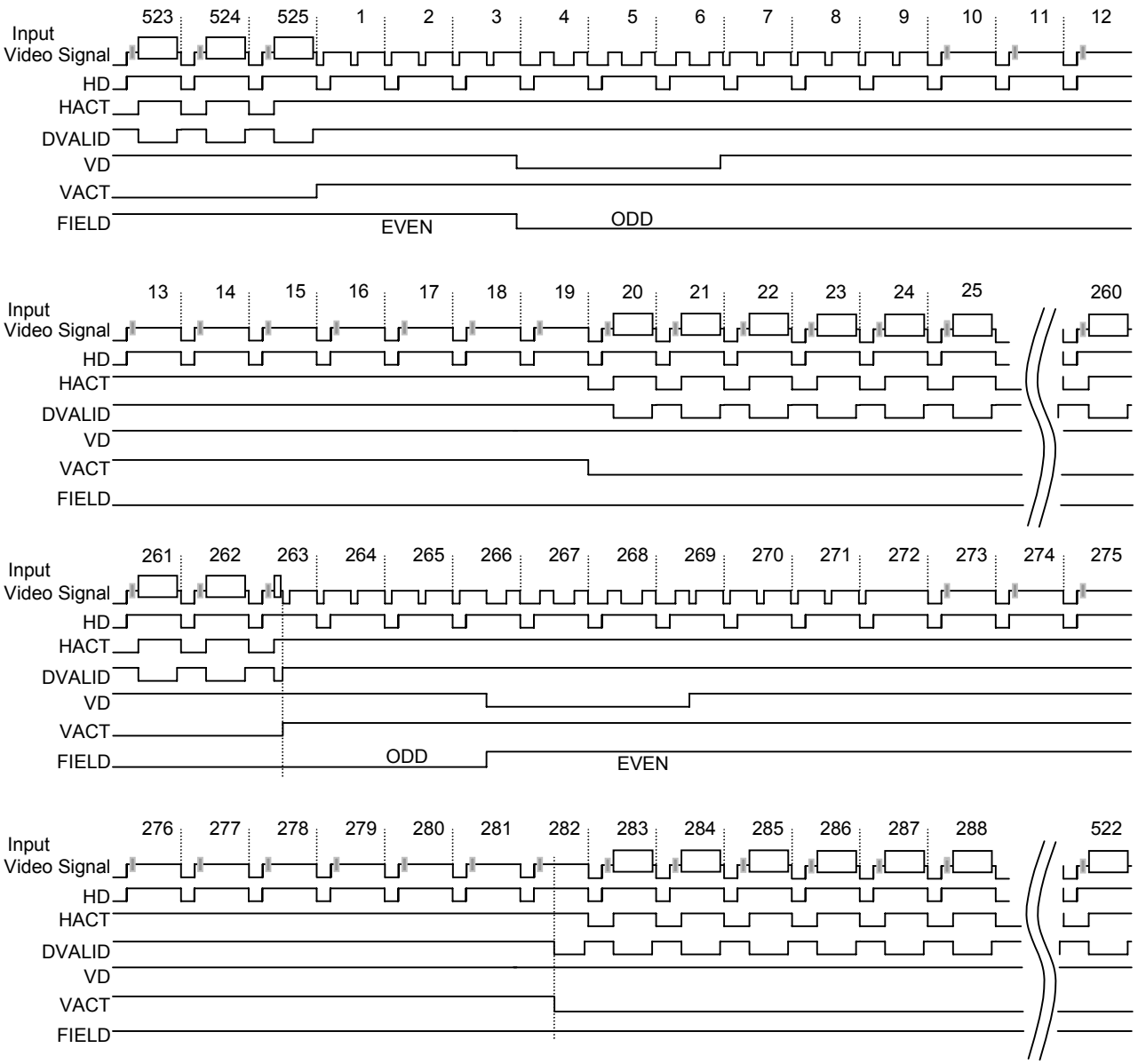
○480x240(WEGA1), 480x234(WEGA2), 480x272



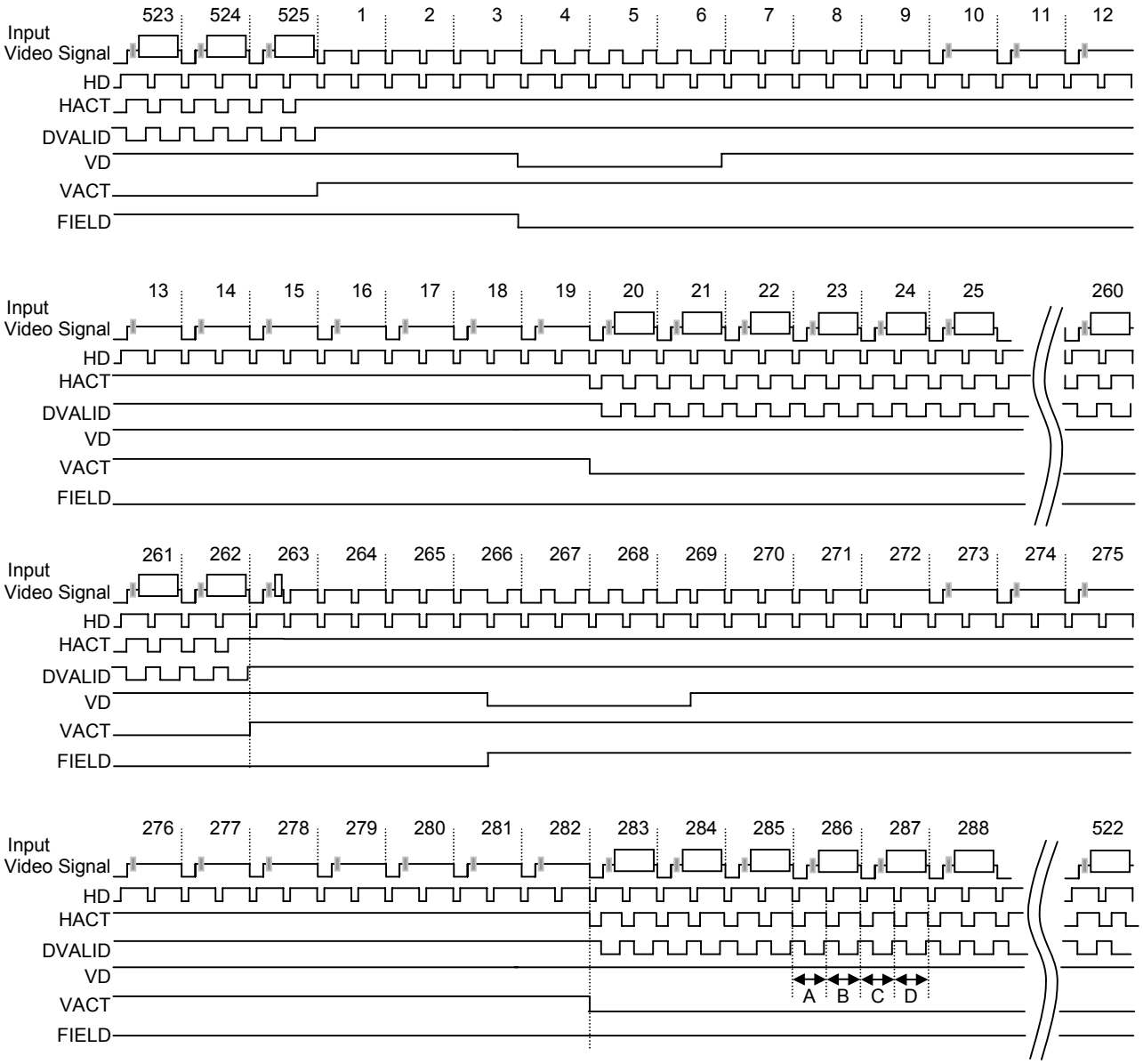
Relationship between Sync timing of 1 frame to the next frame for each output pixel size is shown below.
The timing of HD, HACT, DVALID and VACT signal shown in the figure is enlarge.



Input: 525-line, horizontal : 487-line, Output : Interlace



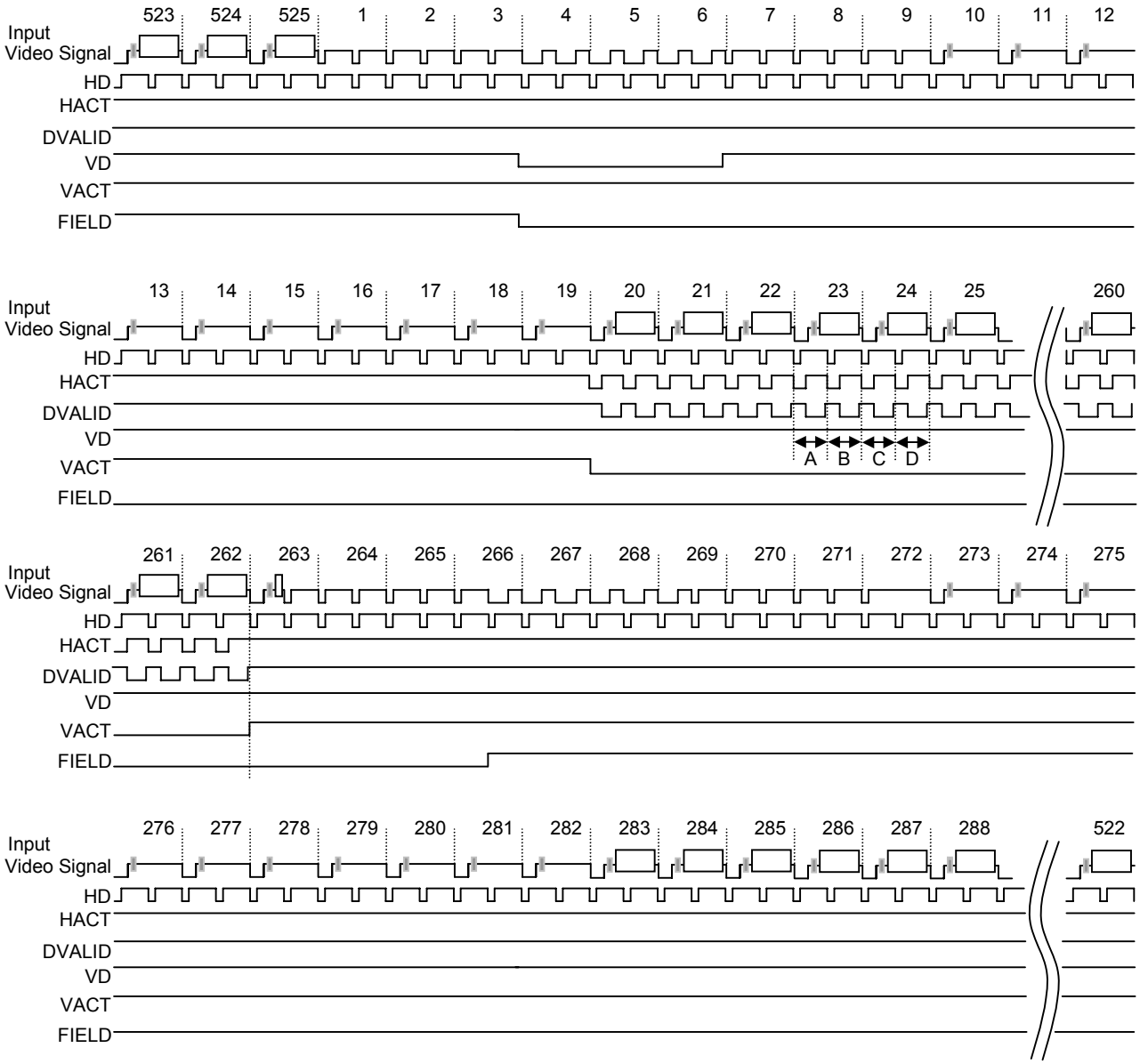
Input: 525-line, horizontal: 487-line, Output: Progressive (60frm/sec)



Because of line repeating process during progressive signal conversion, as shown in the figure above A line and B line / C line and D line is output as the same signal. The FIELD signal is being toggle.

* Both ODD/ EVEN field has 486-line during active section not 487-line.

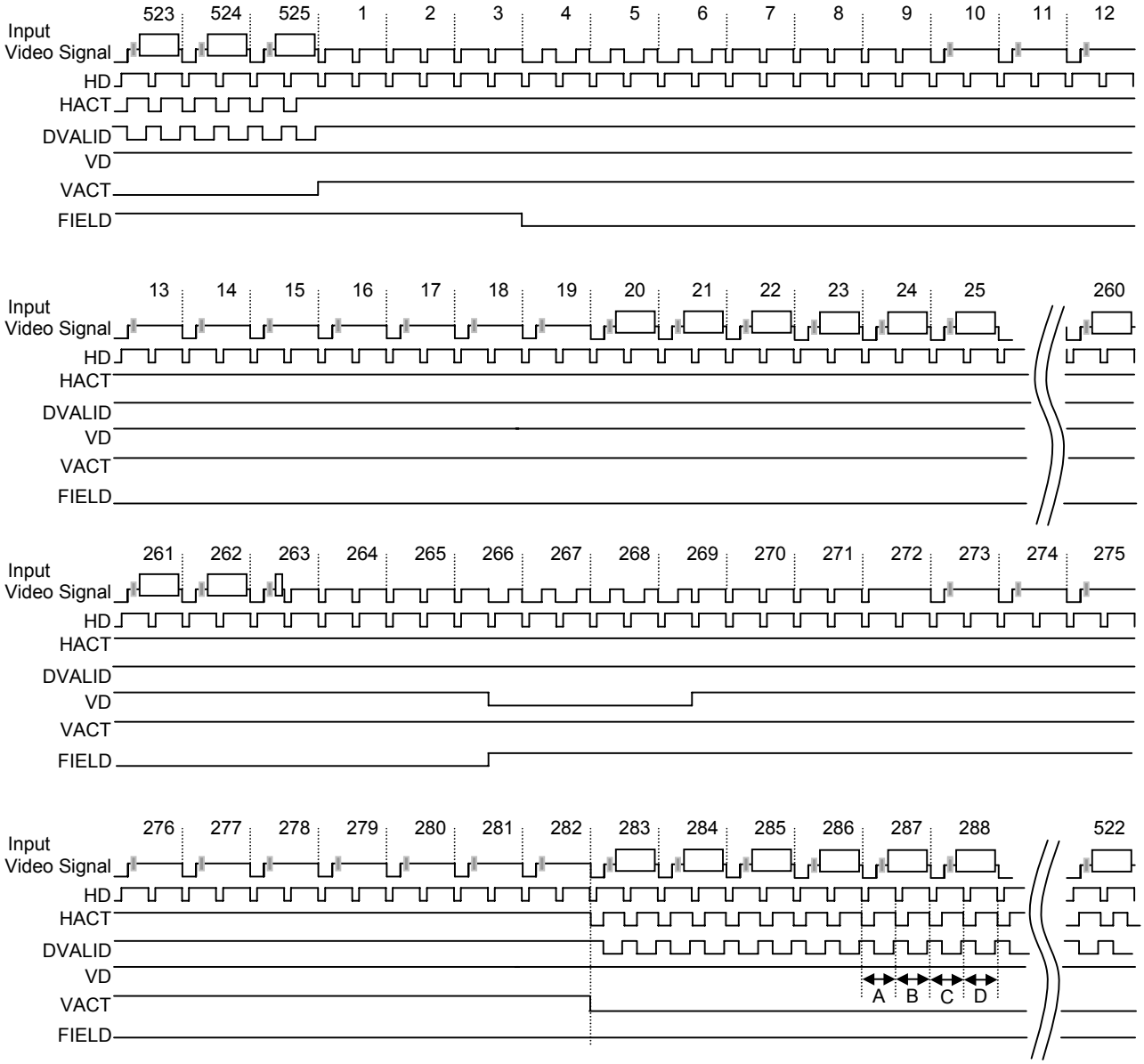
Input : 525-line, Horizontal line : 487-line, Output : Progressive (30frm/sec) (ODD Field output)



Because of line repeating process during progressive signal conversion, as shown in the figure above A line and B line / C line and D line is output as the same signal. The FIELD signal is being toggle.

* Both ODD/ EVEN field has 486-line during active section not 487-line.

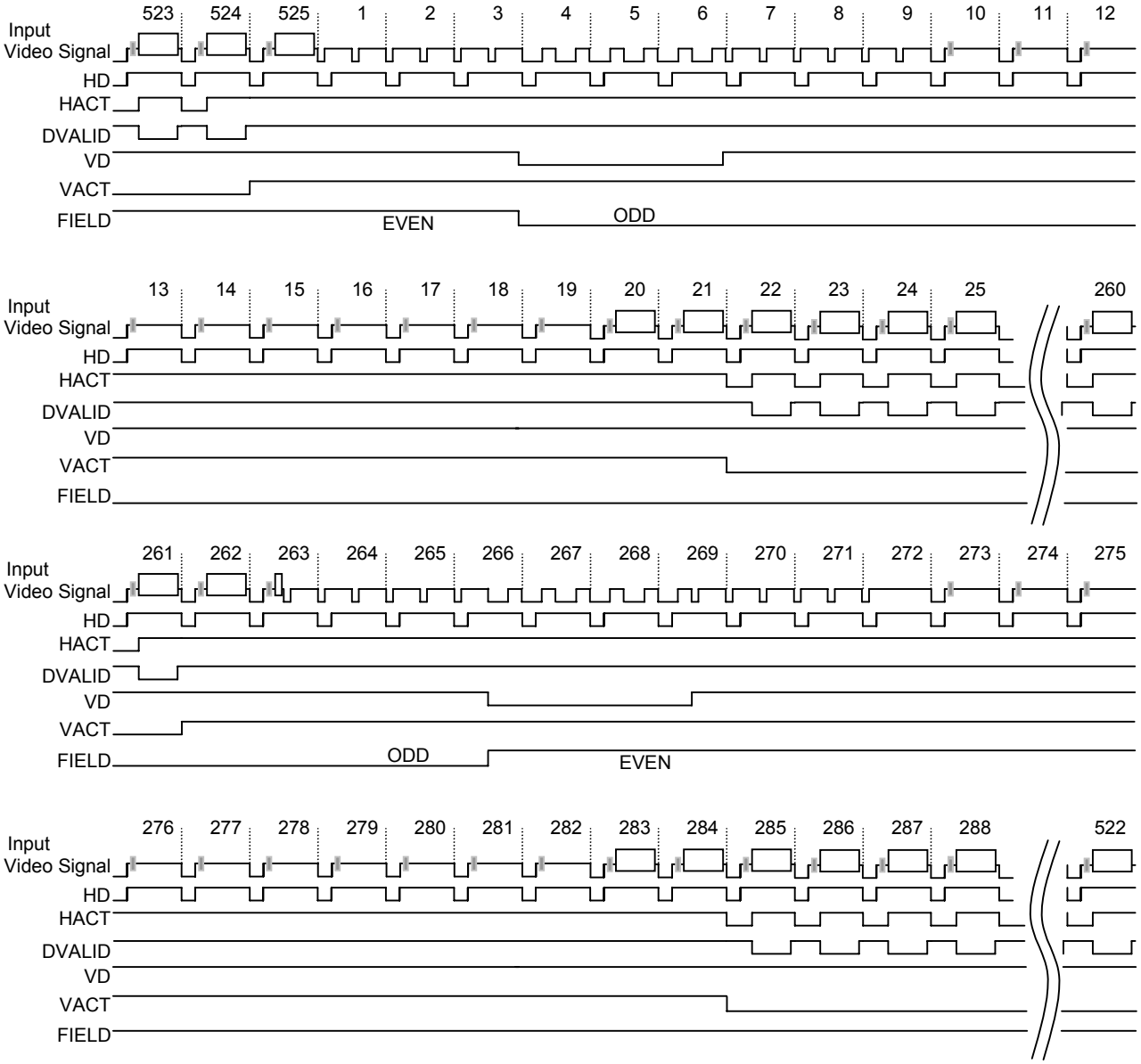
Input : 525-line, Horizontal line : 487-line, Output : Progressive (30frm/sec) (EVEN Field output)



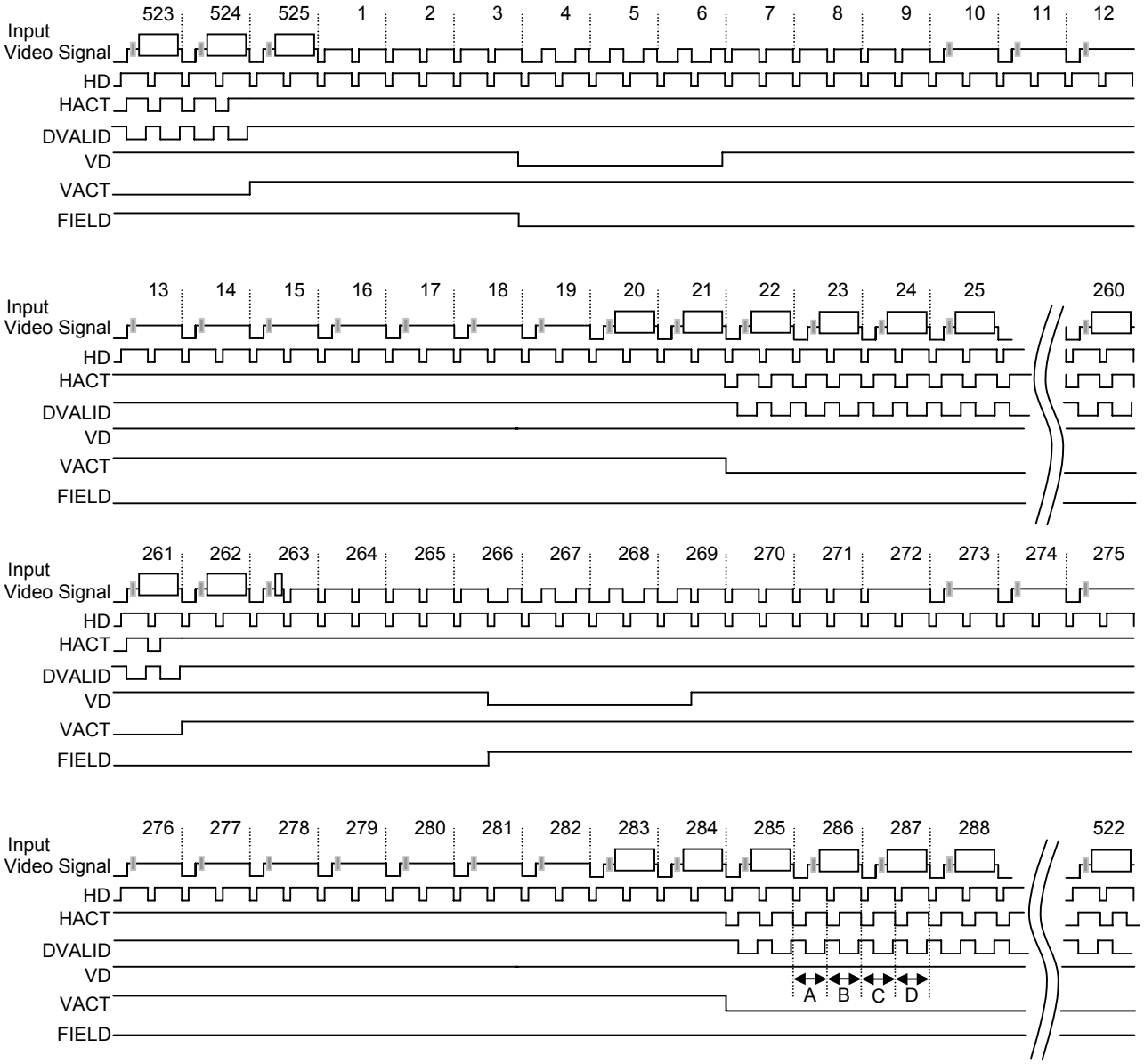
Because of line repeating process during progressive signal conversion, as shown in the figure above A line and B line / C line and D line is output as the same signal. The FIELD signal is being toggle.

* Both ODD/ EVEN field has 486-line during active section not 487-line.

Input : 525-line, Horizontal line : 487-line, Output : Interlace

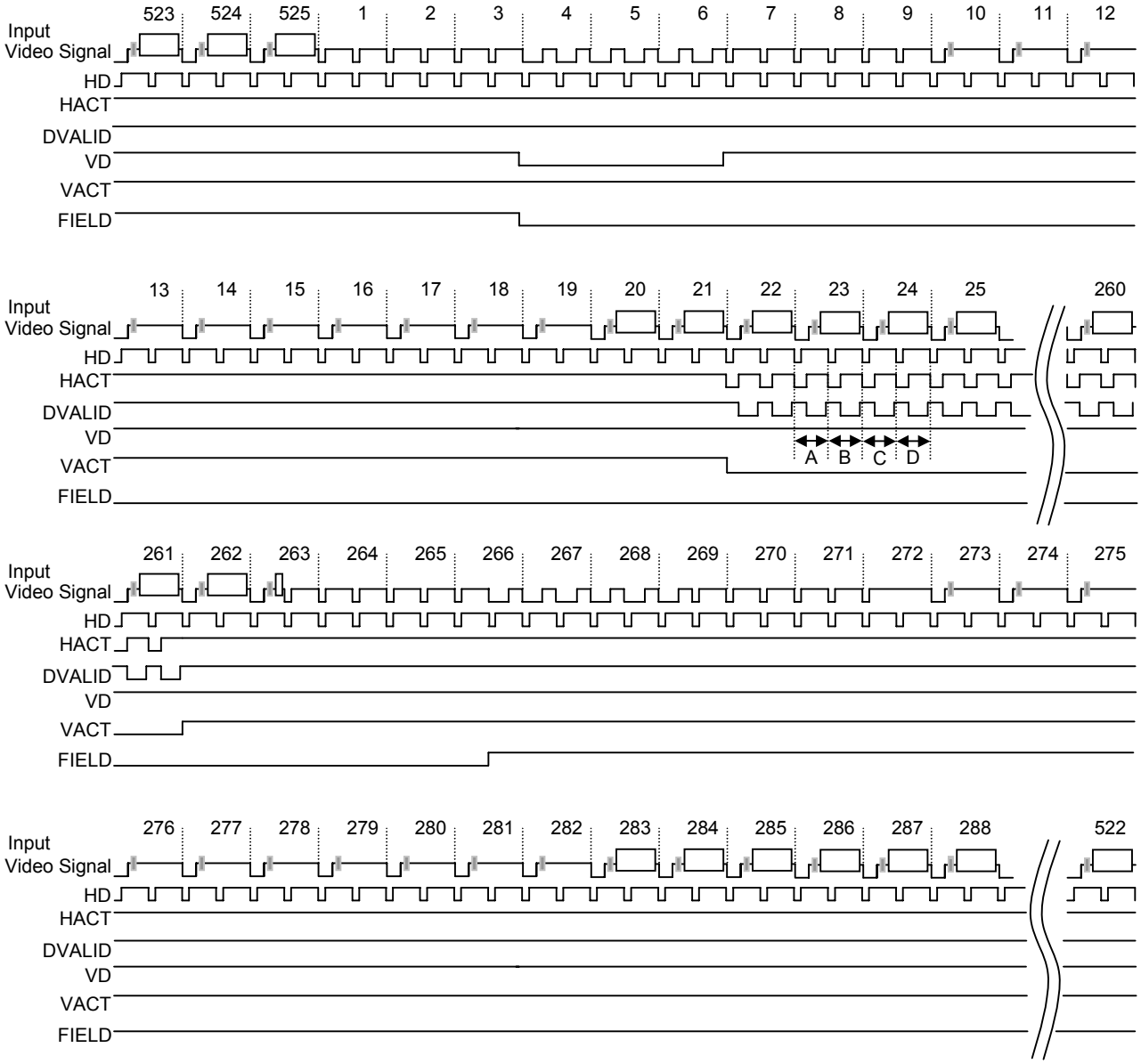


Input : 525-line, Horizontal line : 480-line, Output : Progressive (60frm/sec)



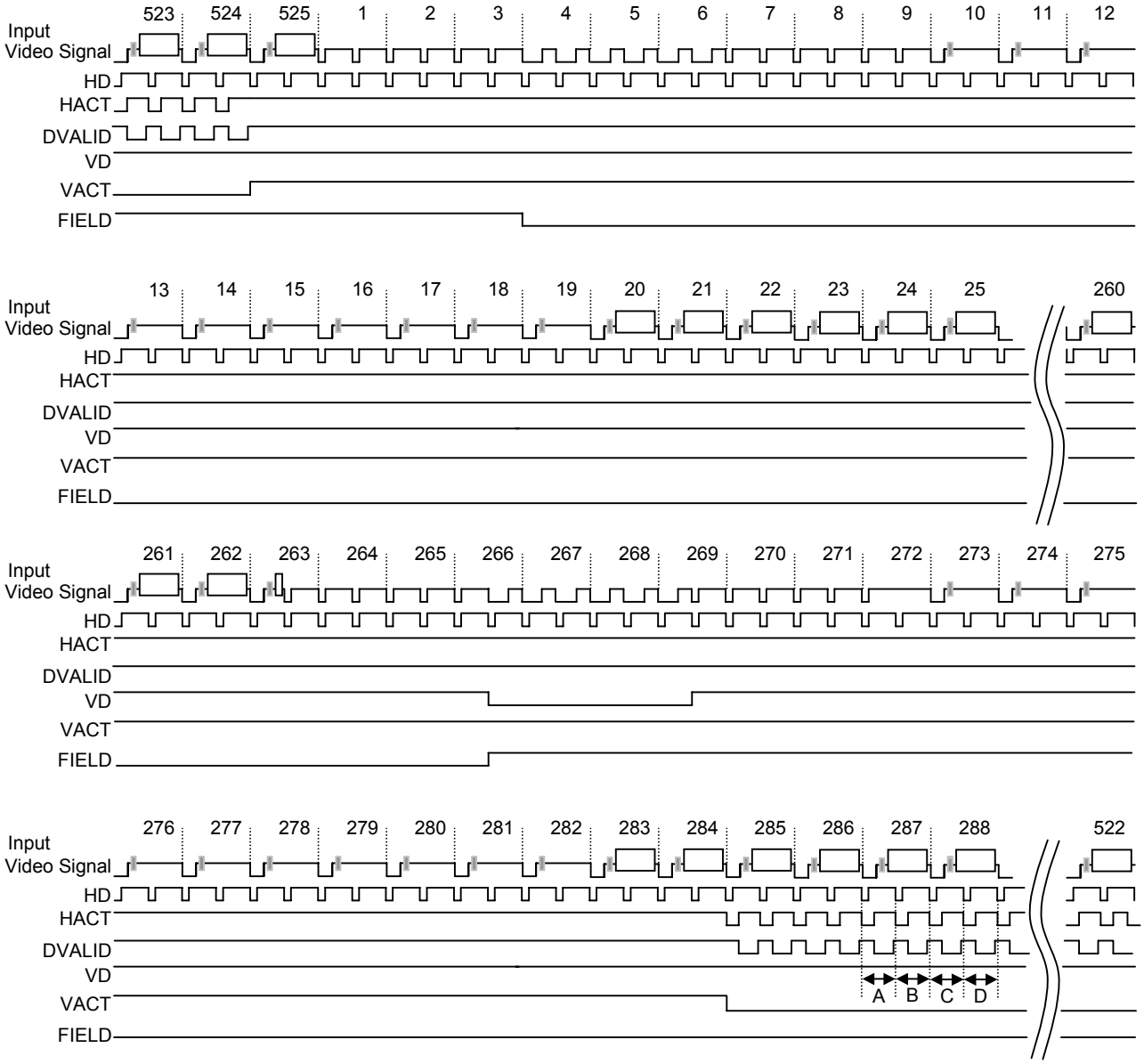
Because of line repeating process during progressive signal conversion, as shown in the figure above A line and B line / C line and D line is output as the same signal. The FIELD signal is being toggle.

Input : 525-line, Horizontal line : 480-line, Output : Progressive (30frm/sec) (ODD field output)



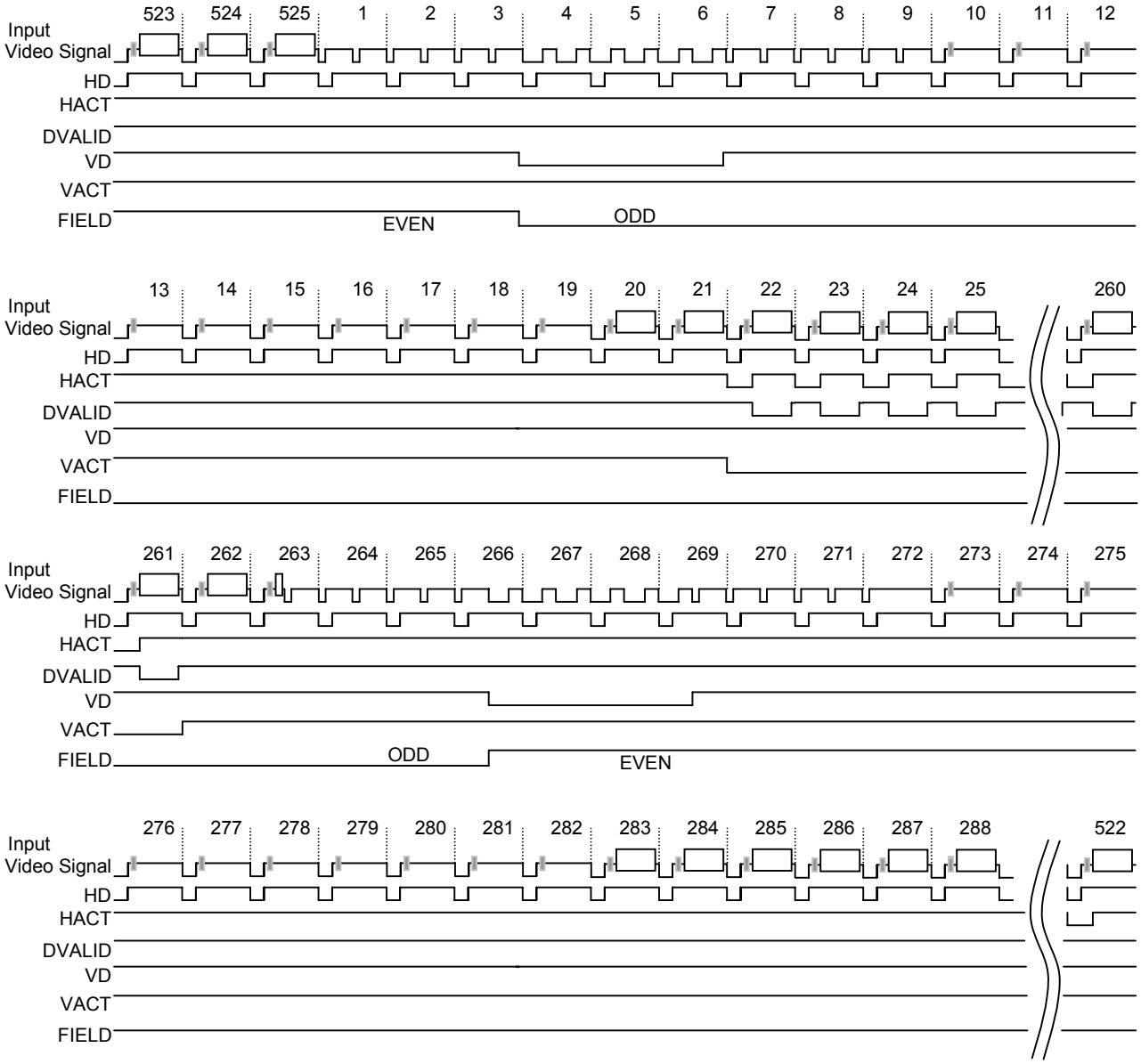
Because of line repeating process during progressive signal conversion, as shown in the figure above A line and B line / C line and D line is output as the same signal. The FIELD signal is being toggle.

Input : 525-line, Horizontal line : 480-line, Output : Progressive (30frm/sec) (EVEN field output)



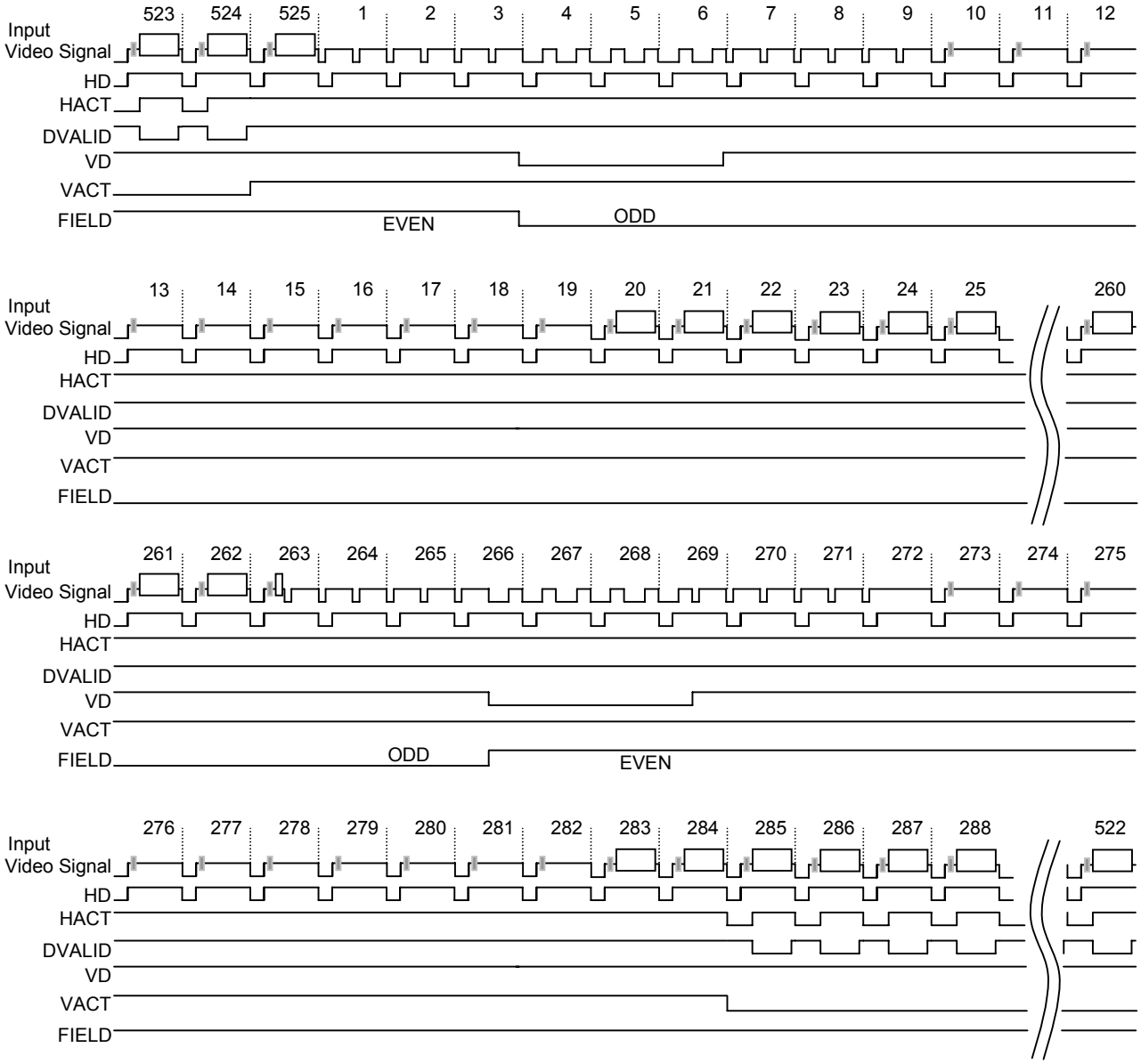
Because of line repeating process during progressive signal conversion, as shown in the figure above A line and B line / C line and D line is output as the same signal. The FIELD signal is being toggle.

Input : 525-line, Horizontal line : 240-line/234-line, Output : (ODD field output)



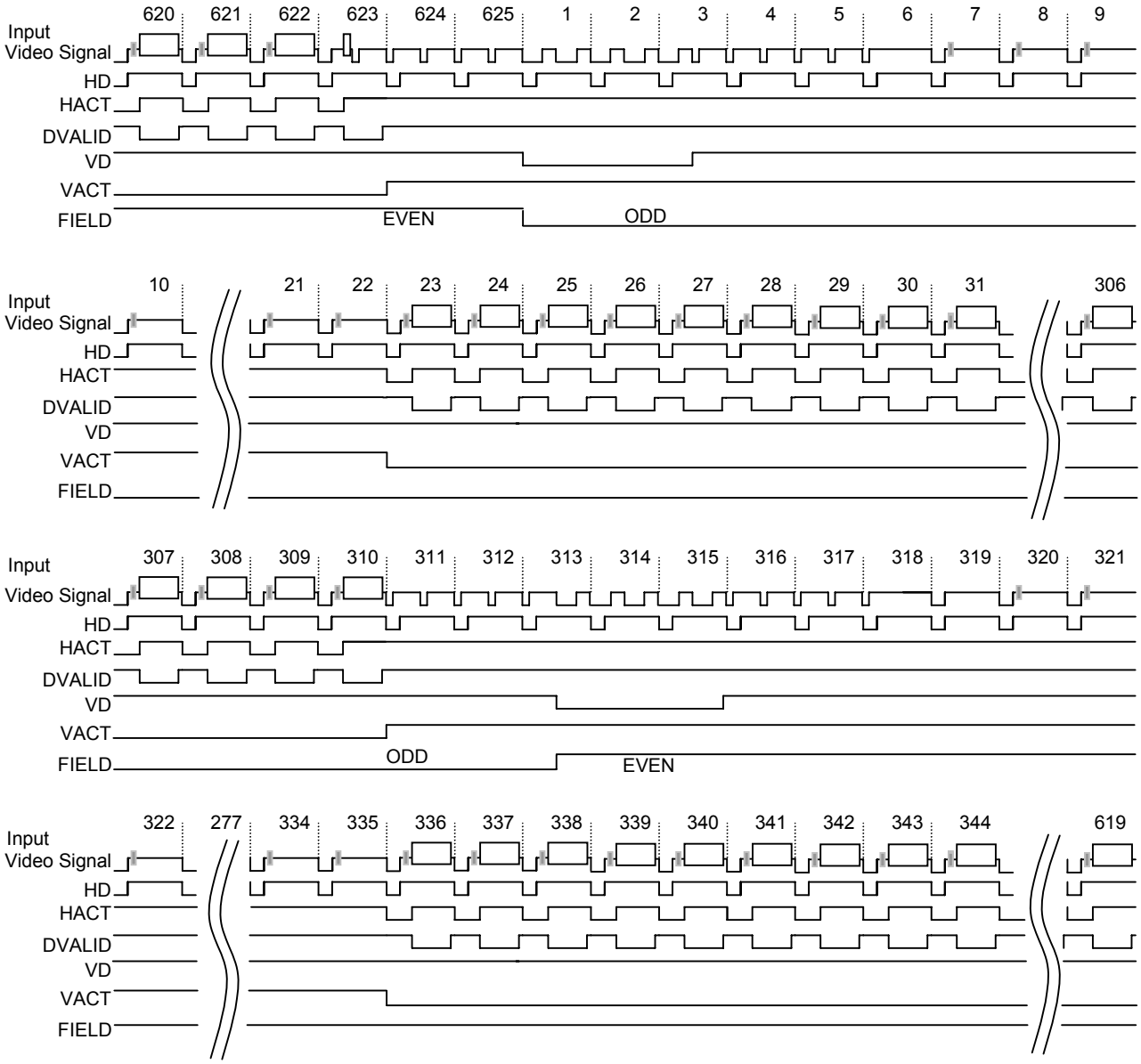
In 234-line output case, as shown above lines from line 22 to 24 and from line 259 to 261 is not count as active line. For that reason, HACT, VACT and DVALID is “High” during the line mentioned above.

Input : 525-line, Horizontal line : 240-line/234-line, Output : (EVEN field output)

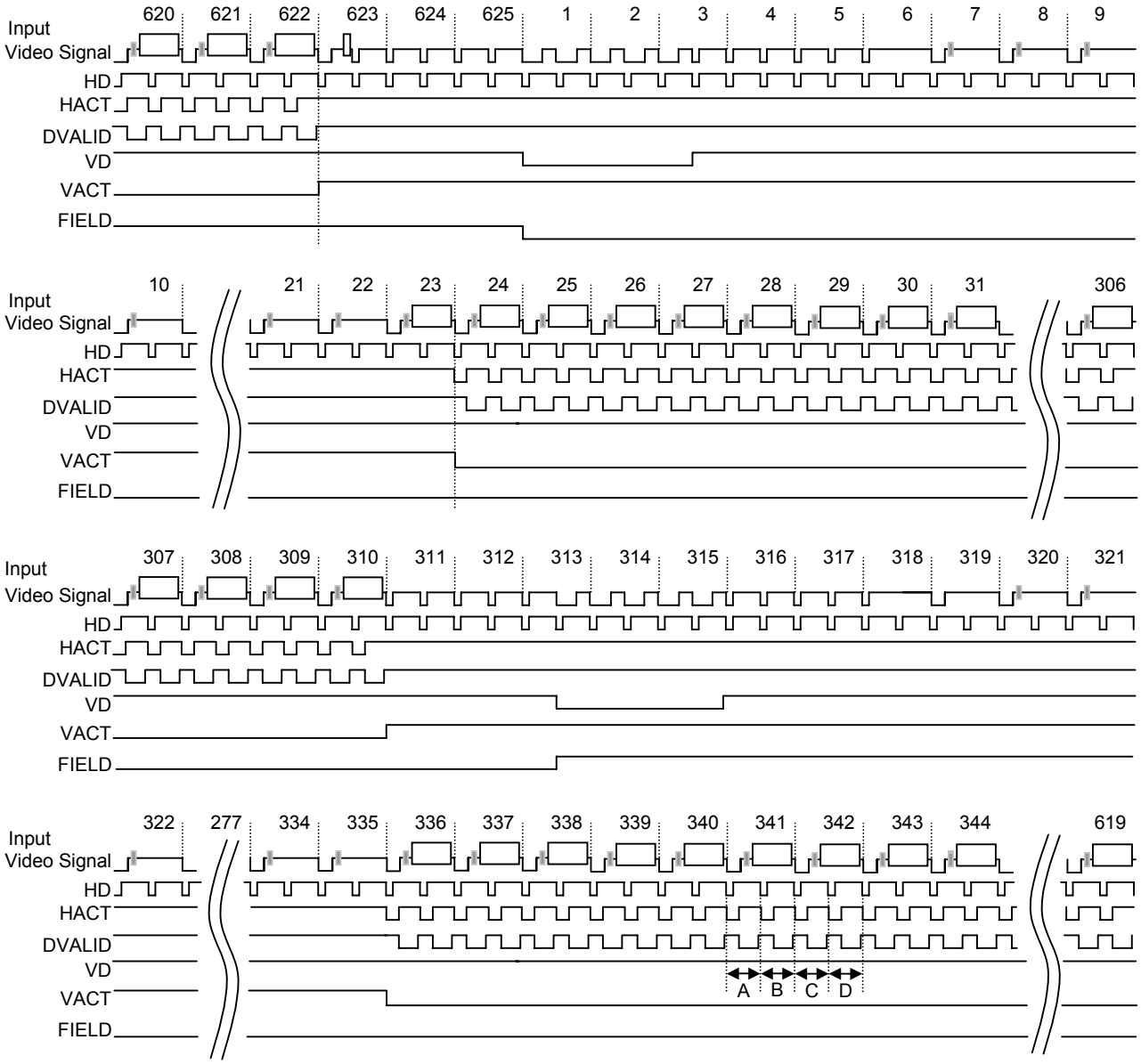


In 234-line output case, as shown above lines from line 22 to 24 and from line 259 to 261 is not count as active line. For that reason, HACT, VACT and DVALID is “High” during the line mentioned above.

Input : 625-line, Horizontal line : 576-line



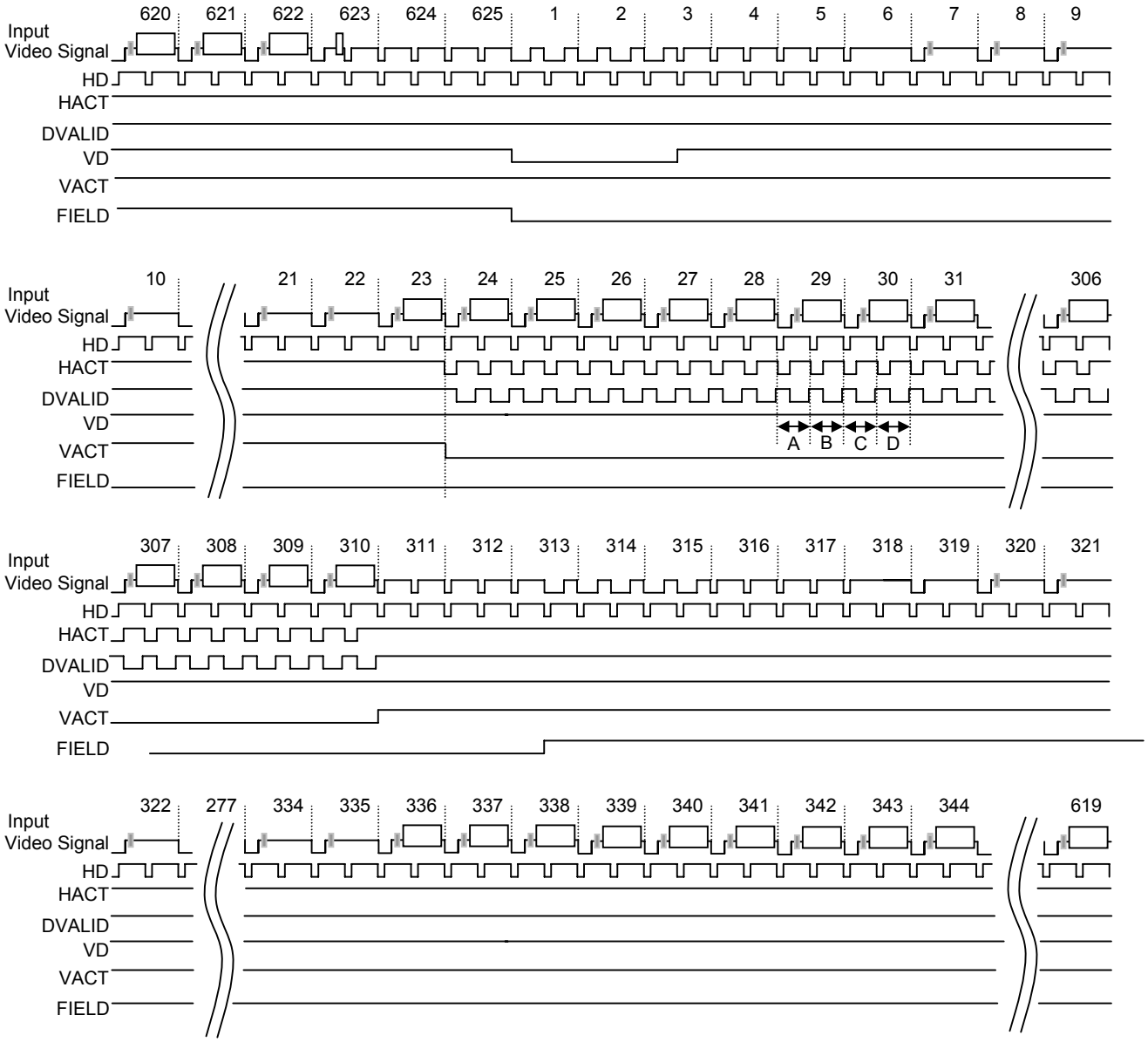
Input : 625-line, Horizontal line : 576-line, Output : Progressive (60frm/sec)



Because of line repeating process during progressive signal conversion, as shown in the figure above A line and B line / C line and D line is output as the same signal. The FIELD signal is being toggle.

* In the above figure, both ODD/EVEN field line number is 574-line. To set the active line to 576-line, set the VBIL[2:0] register to 0x01 value.

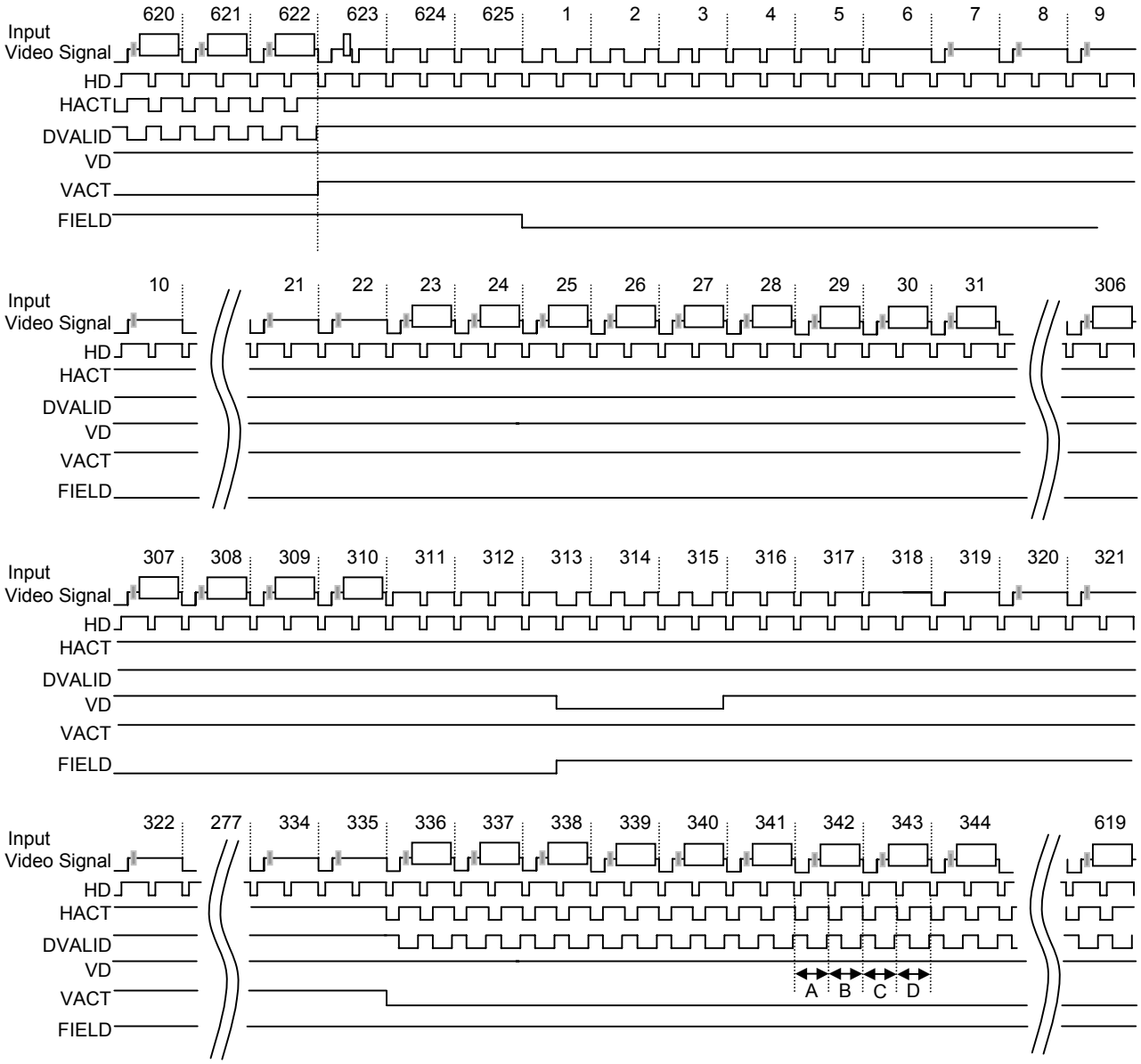
Input : 625-line, Horizontal line : 576-line, Output : Progressive (30frm/sec) (ODD field output)



Because of line repeating process during progressive signal conversion, as shown in the figure above A line and B line / C line and D line is output as the same signal. The FIELD signal is being toggle.

* In the above figure, both ODD/EVEN field line number is 574-line. To set the active line to 576-line, set the VBIL[2:0] register to 0x01 value.

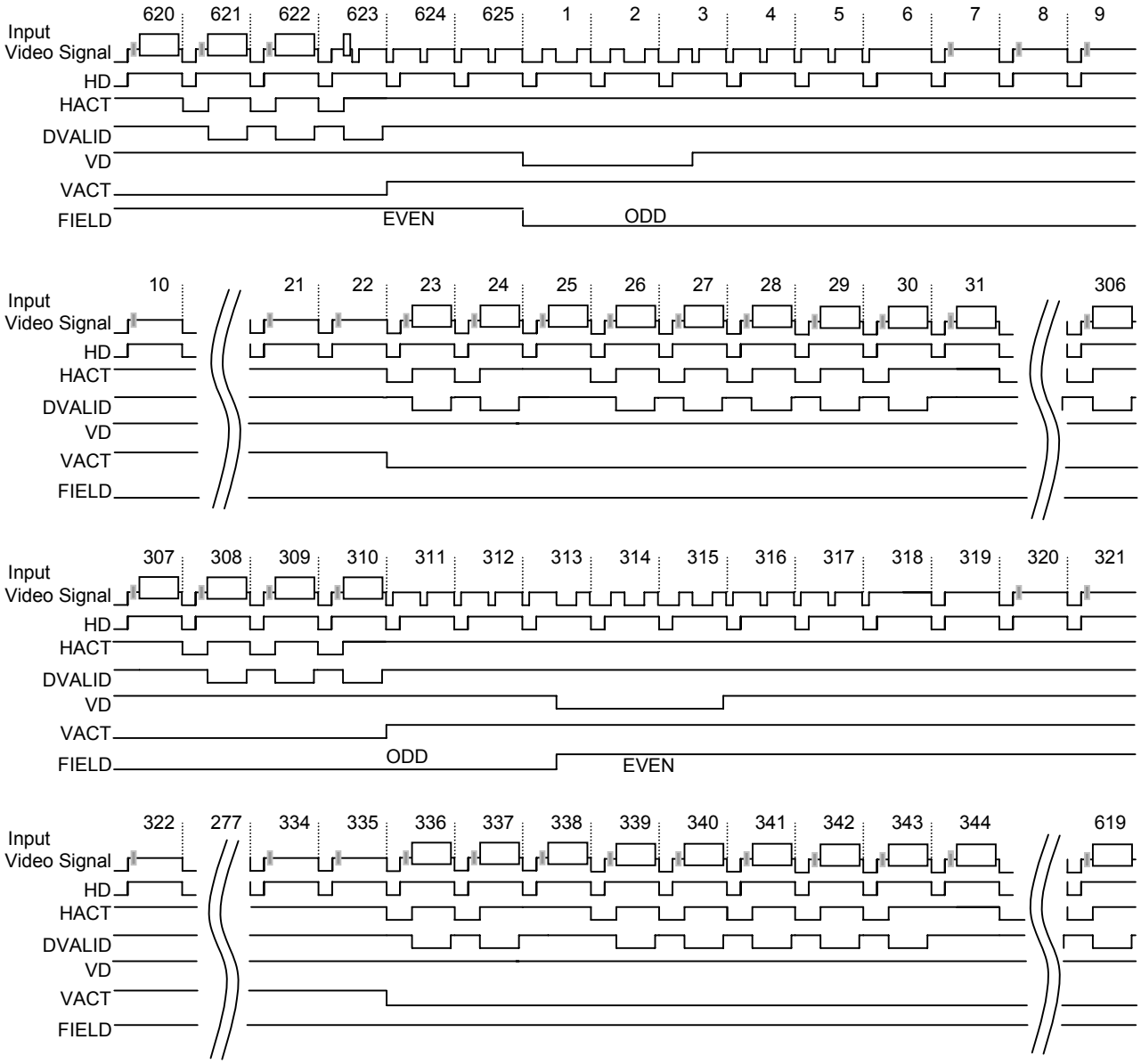
Input : 625-line, Horizontal line : 576-line, Output : Progressive (30frm/sec) (EVEN field output)



Because of line repeating process during progressive signal conversion, as shown in the figure above A line and B line / C line and D line is output as the same signal. The FIELD signal is being toggle.

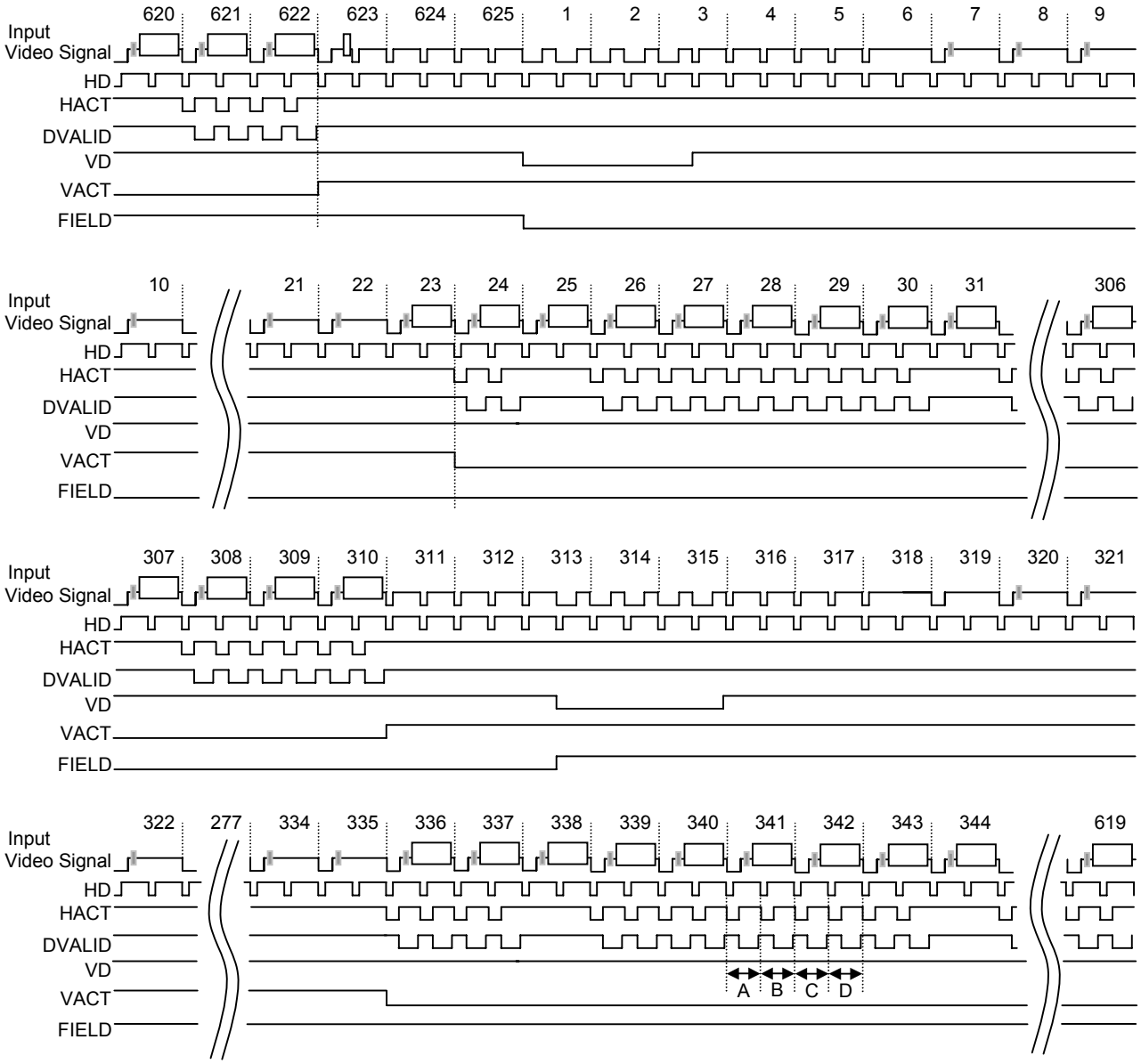
* In the above figure, both ODD/EVEN field line number is 574-line. To set the active line to 576-line, set the VBIL[2:0] register to 0x01 value.

Input : 625-line, Horizontal line : 480-line



As shown in the figure above, start from line 25 / line 338 to the next starting line of each 5 line, the line is output as not active line. HACT and DVALID is “High” during the line mentioned.
EAV sync code is added to the line mentioned above and SAV sync code is not.

Input : 625-line, Horizontal line : 480-line, Output : Progressive (60frm/sec)

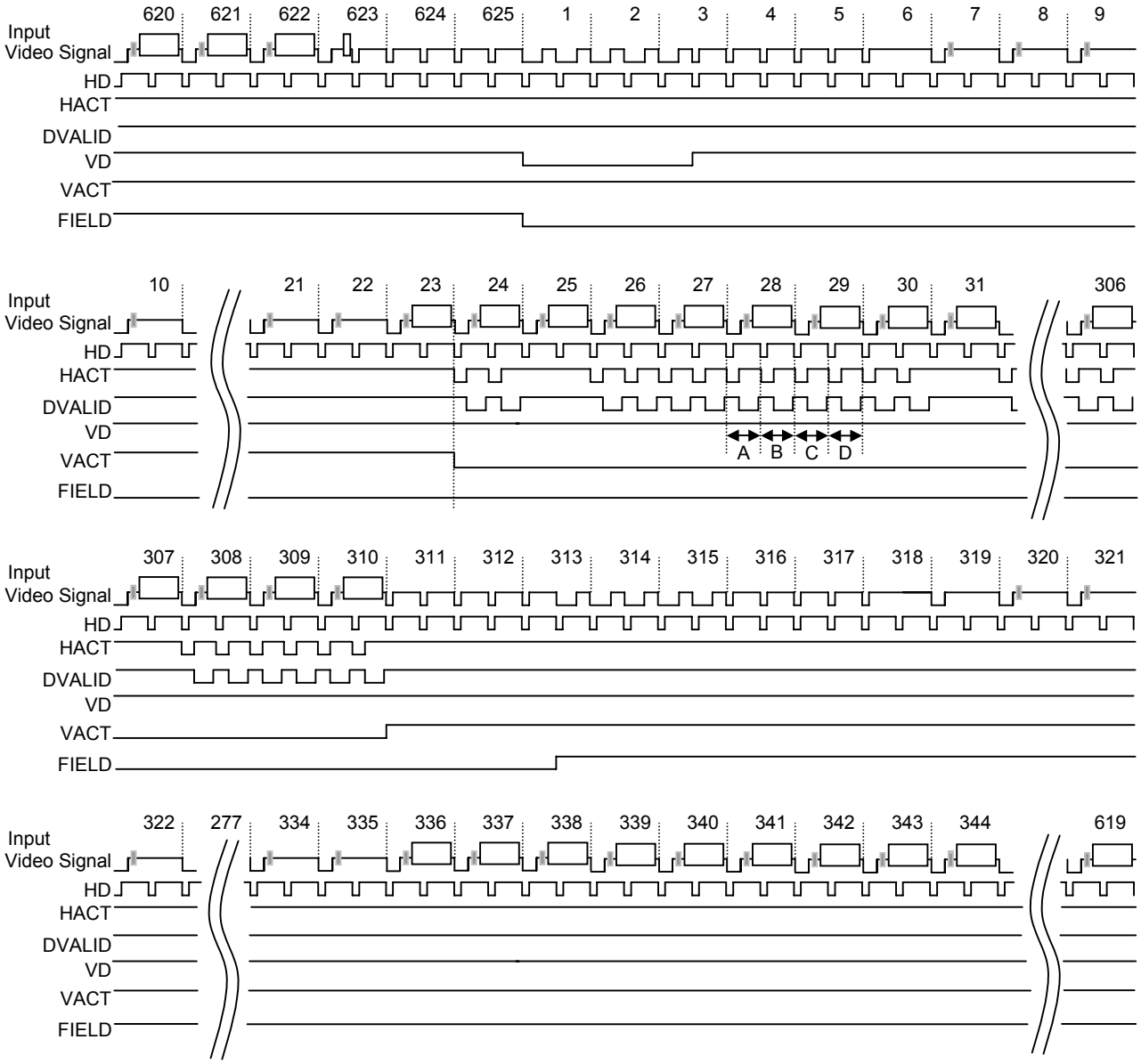


Because of line repeating process during progressive signal conversion, as shown in the figure above A line and B line / C line and D line is output as the same signal. The FIELD signal is being toggle.

As shown in the figure above, start from line 25 / line 338 to the next starting line of each 10 line, the line is output as not active line. HACT and DVALID is “High” during the line mentioned.
EAV sync code is added to the line mentioned above and SAV sync code is not.

* In the above figure, both ODD/EVEN field line number is 478-line. To set the active line to 480-line, set the VBIL[2:0] register value to 0x01.

Input : 625-line, Horizontal line : 480-line, Output : Progressive (30frm/sec) (ODD field output)

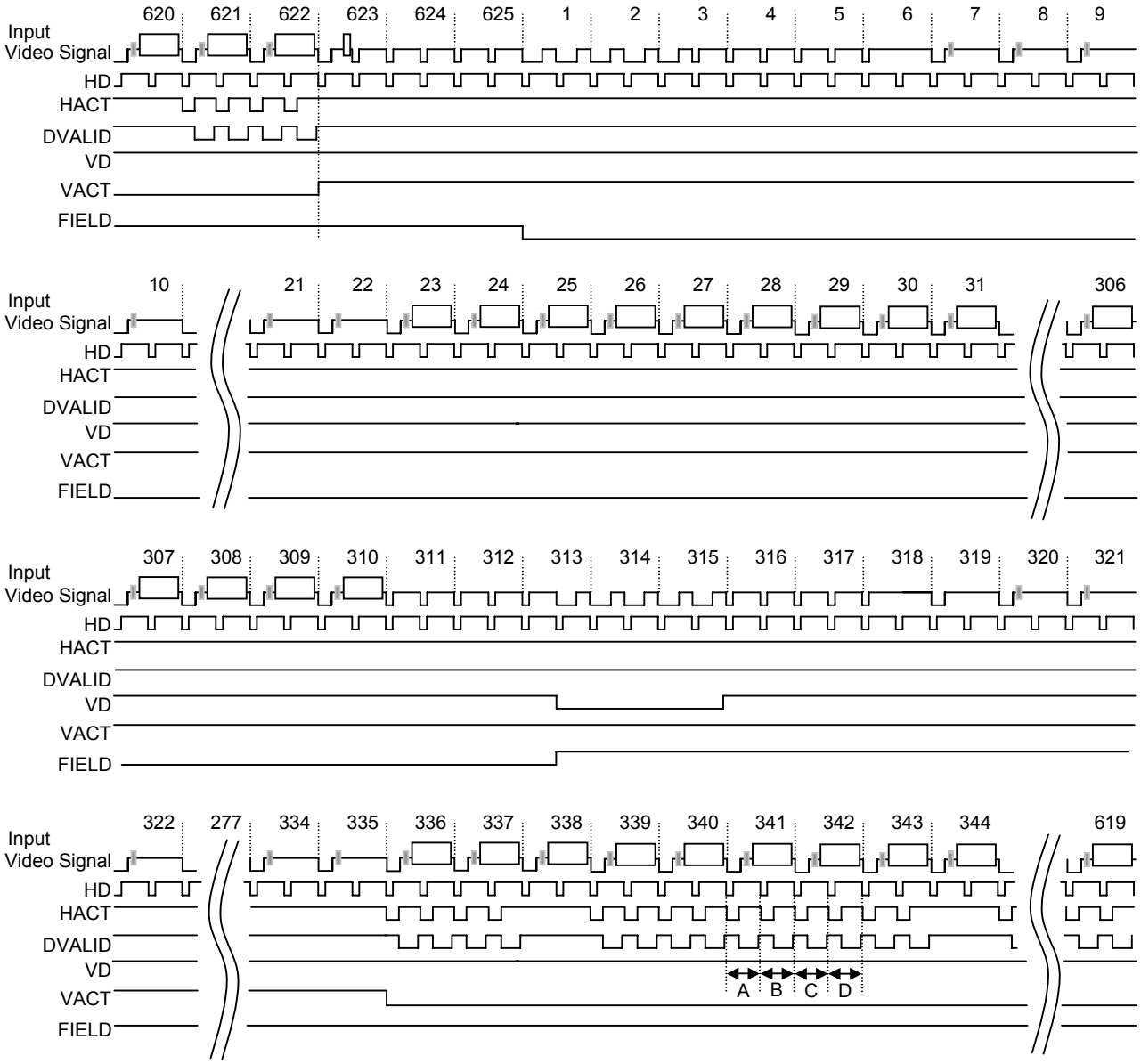


Because of line repeating process during progressive signal conversion, as shown in the above figure A line and B line / C line and D line is output as the same signal. The FIELD signal is being toggle.

As shown in the figure above, start from line 25 to the next starting line of each 10 line, the line is output as not active line. HACT and DVALID is “High” during the line mentioned.
EAV sync code is added to the line mentioned above and SAV sync code is not.

* In the above figure, both ODD/EVEN field line number is 478-line. To set the active line to 480-line, set the VBIL[2:0] register value to 0x01.

Input : 625-line, Horizontal line : 480-line, Output : Progressive (30frm/sec) (EVEN field output)

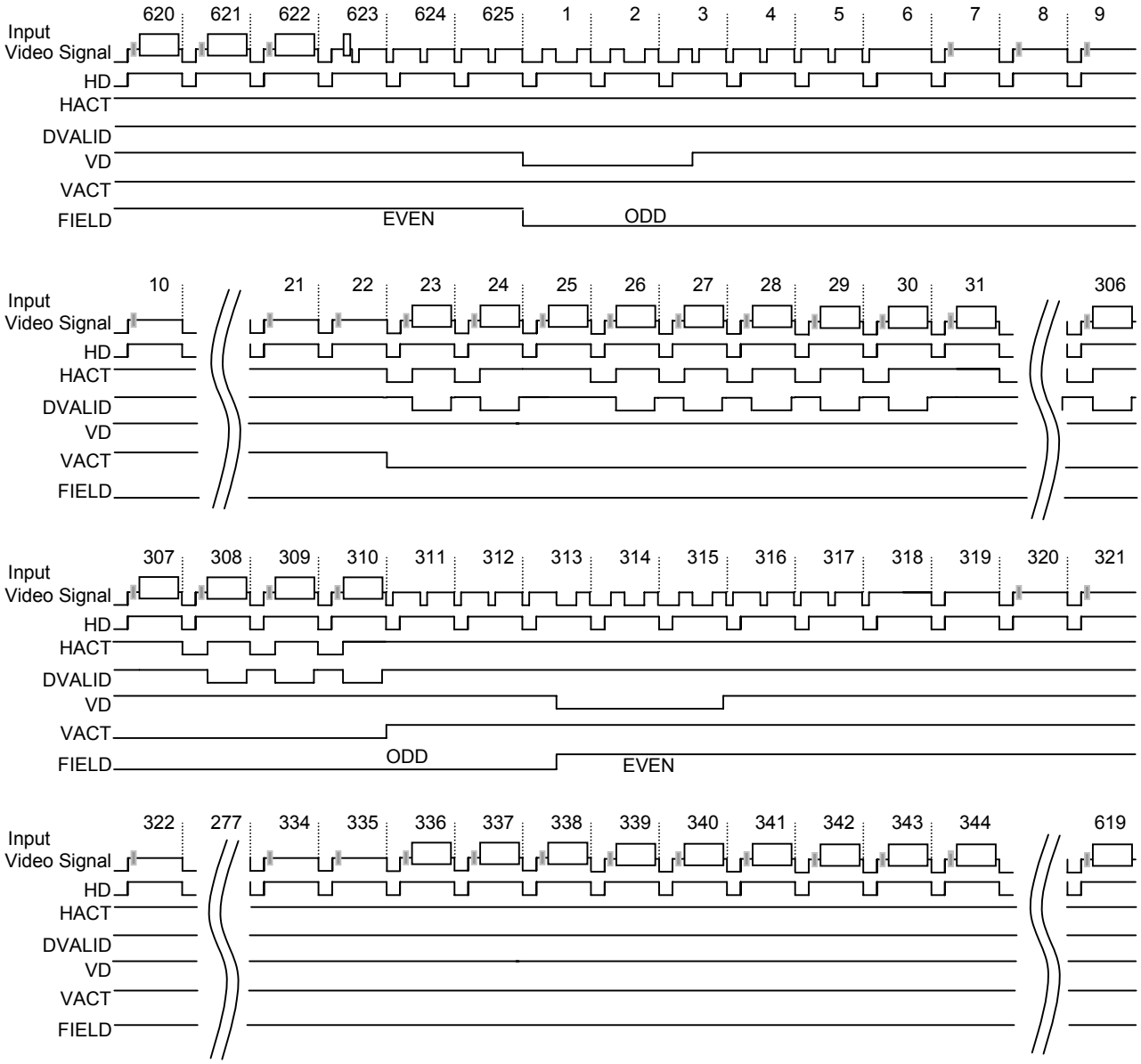


Because of line repeating process during progressive signal conversion, as shown in the figure above, A line and B line / C line and D line is output as the same signal. The FIELD signal is being toggle.

As shown in the figure above, start from line 338 to the next starting line of each 10 line, the line is output as not active line. HACT and DVALID is “High” during the line mentioned.
EAV sync code is added to the line mentioned above and SAV sync code is not.

* In the above figure, both ODD/EVEN field line number is 478-line. To set the active line to 480-line, set the VBIL[2:0] register value to 0x01.

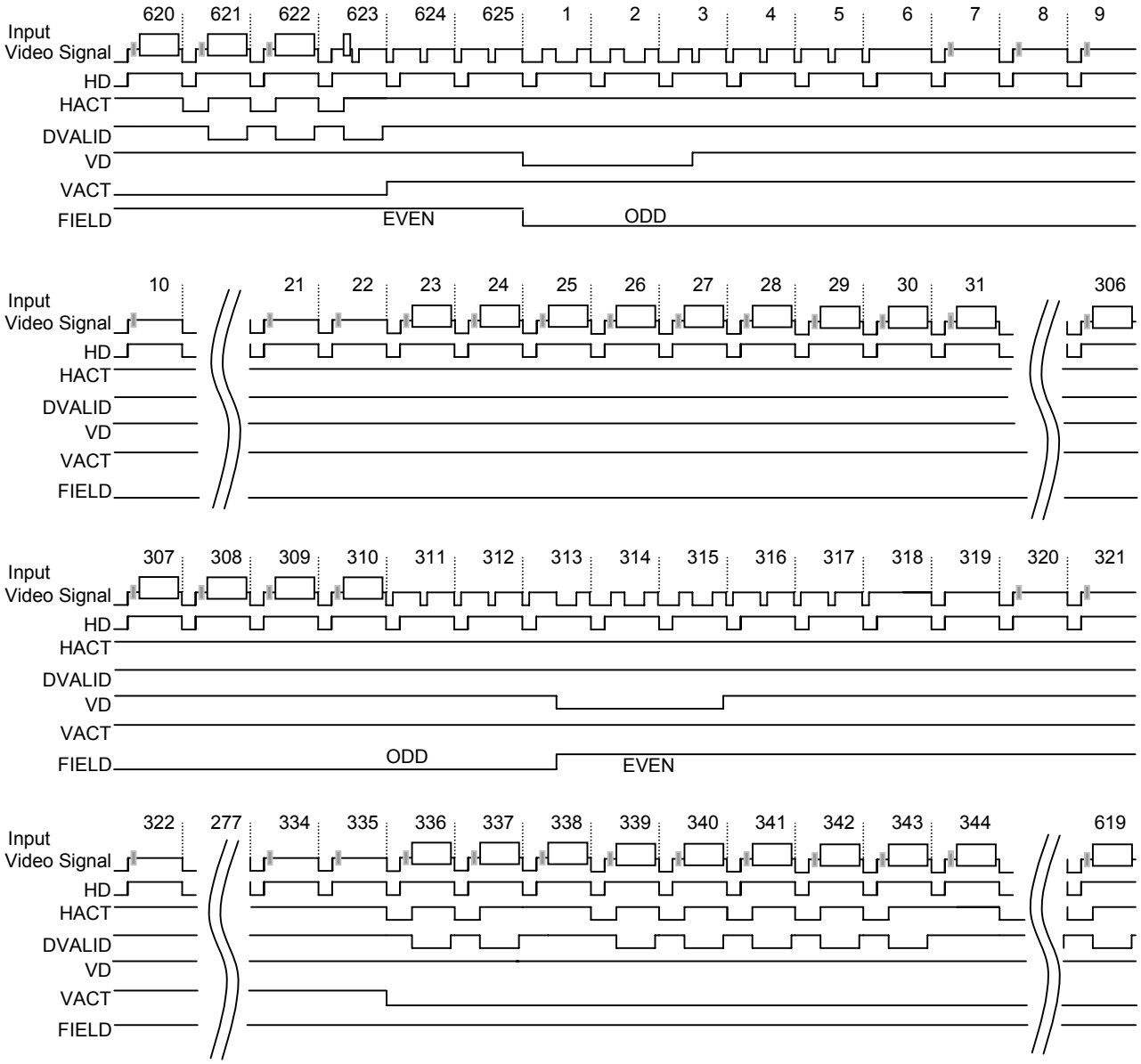
Input : 625-line, Horizontal line : 240-line/234-line, Output : Progressive (ODD field output)



As shown in the figure above, start from line 25 to the next starting line of each 5 line, the line is output as not active line. HACT and DVALID is “High” during the line mentioned.
EAV sync code is added to the line mentioned above and SAV sync code is not.

In 234-line output case, as shown above, lines from line 23 to 26 and from line 308 to 310 is not count as active line. For that reason, HACT, VACT and DVALID output is “High” during the line mentioned above.

Input : 625-line, Horizontal line : 240-line/234-line, Output : Progressive (EVEN field output)



As shown in the figure above, start from line 338 to the next starting line of each 5 line, the line is output as not active line. HACT and DVALID is “High” during the line mentioned.
EAV sync code is added to the line mentioned above and SAV sync code is not.

In 234-line output case, as shown above, lines from line 336 to 339 and from line 621 to 623 is not count as active line. For that reason, HACT, VACT and DVALID output is “High” during the line mentioned above.

Input video signal categorization

The AK8857 can decode the following video signals, in accordance with the register setting.

NTSC-M,J
NTSC-4.43
PAL-B,D,G,H,I,N
PAL-Nc
PAL-M
PAL-60
SECAM

The register settings for the input signal characterization are essentially as follows.

○VSCF[1:0]-bi: Setting for subcarrier frequency of input signal

VSCF[1:0]-bit	Subcarrier frequency (MHz)	Notes
[00]	3.57954545	NTSC-M,J
[01]	3.57561149	PAL-M
[10]	3.58205625	PAL-Nc
[11]	4.43361875	PAL-B,D,G,H,I,N , NTSC-4.43 , PAL-60 SECAM*

*For SECAM input signal, set VSCF[1:0] to [11].

○VCEN[1:0]-bit: Setting for color encode format of input signal.

VCEN[1:0]-bit	Color encode format	Notes
[00]	NTSC	
[01]	PAL	
[10]	SECAM	
[11]	Reserved	

○VLF-bit : Setting for line frequency of each input frame.

VLF-bit	Number of lines	Notes
[0]	525	NTSC-M,J , NTSC-4.43 , PAL-M, PAL-60
[1]	625	PAL-B,D,G,H,I,N,Nc , SECAM

○BW-bit: Setting for decoding of input signal as monochrome signal (monochrome mode)

BW-bit	Signal type	Notes
[0]	Not monochrome (monochrome mode OFF)	
[1]	Decode as monochrome signal (monochrome mode ON)	

In the monochrome mode at CVBS decoding, the input signal is treated as a monochrome signal, and all sampling data digitized the the AD converter passes through the luminance process and is processed as a luminance signal. Thus, with this bit ON, the signal input to the Y/C separation block is all output as luminance signal data to the luminance signal processing block.

In the monochrome mode at S-video decoding, Y signal is only decoded.

In the monochrome mode, the CbCr code is output as 0x80 (601 level data) regardless of the input.

○SETUP-bit: Setting for presence or absence of input signal SETUP.

SETUP-bit	SETUP presence/absence	Notes
[0]	Setup absent	
[1]	Setup present	7.5IRE Setup

With the Setup present setting, the luminance and color signals are processed as follows:

Luminance signal: Y=(Y-7.5)/0.925

Color signal: U=U/0.925, V=V/0.925

Input Signal Auto Detection Function

The register settings for auto detection are essentially as follows.

○AUTODET-bit: Settings for auto detection of input signal (auto detection mode)

AUTODET-bit	Auto detection	Notes
[0]	OFF	Manual setting
[1]	ON	

The auto detection recognizes the following parameters.

Number of lines per frame: 525/625

Carrier frequencies: 3.57954545
3.57561149
3.58205625
4.43361875

Color encoding formats: NTSC
PAL
SECAM

Monochrome signal: Not monochrome/monochrome

Note: Automatic monochrome detection is active if the color kill setting is ON (COLKILL-bit = [1].)

The AK8857 stores the detected parameter to the Input Video Status Register (thus, as an internal notice function).

This enables the host to distinguish among the formats NTSC-M, J; NTSC-4.43; PAL-B, D, G, H, I, N; PAL-M; PAL-Nc; PAL-60; SECAM; and monochrome.

It should be noted that it does not detect NTSC-M, NTSC-J, or PAL-B, D, G, H, I, N formats.

(Notice)

“Direct SYNC VLOCK” (Sub-Address0x03[7]=1) must not use when it is being operated on auto detection function.

Limiting auto input video signal detection function

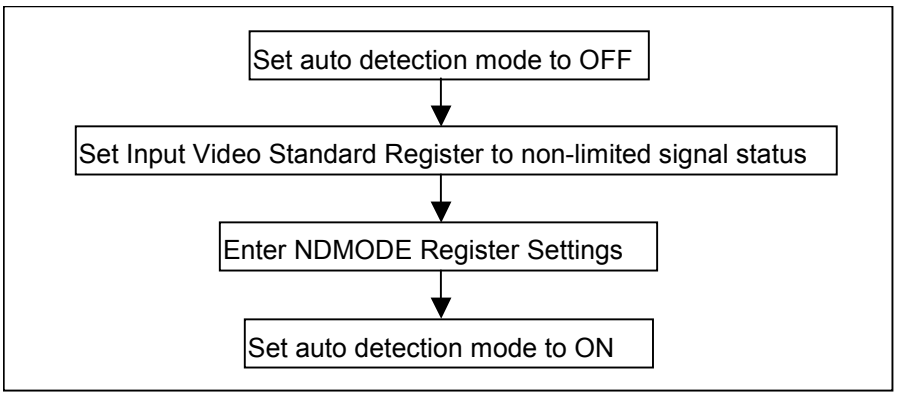
The AK8857 has the function to limit the input video signal to be detected during auto detection mode.

○NDMODE Register: For limiting auto detection candidates

Bit	Register Name		R/W	Definition
bit 0	NDPALM	No Detect PAL-M bit	R/W	[0]: PAL-M candidate [1]: PAL-M non-candidate
bit 1	NDPALNC	No Detect PAL-Nc bit	R/W	0]: PAL-Nc candidate [1]: PAL-Nc non-candidate
bit 2	NDSECAM	No Detect SECAM bit	R/W	[0]: SECAM candidate [1]: SECAM non-candidate
bit 3	Reserved	Reserved	R/W	Reserved
bit 4	NDNTSC443	No Detect NTSC-4.43 bit	R/W	0]: NTSC-4.43 candidate [1]: NTSC-4.43 non-candidate
bit 5	NDPAL60	No Detect PAL-60 bit	R/W	[0]: PAL-60 candidate [1]: PAL-60 non-candidate
bit 6	ND525L	No Detect 525Line bit	R/W	[0]: 525 line candidate [1]: 525 line non-candidate
bit 7	ND625L	No Detect 625Line bit	R/W	[0]: 625 line candidate [1]: 625 line non-candidate

In making the above register settings, the following restrictions is apply,

1. Setting both NDNTSC443(bit 4) and NDPAL60(bit 5) to [1] (High) is prohibited.
2. Setting both ND525L(bit 6) and ND625L(bit 7) to [1] (High) is prohibited.
3. To limit candidate formats, it is necessary to have the auto detection mode OFF while first setting the register to non-limited signal status and next the NDMODE settings, and then setting the auto detection mode to ON.



Output Data format

In the AK8857, the settings for the output code and the vertical blanking intervals for the output signal are as follows.

○601LIMIT-bit: Settings for output data code Min/Max

601LIMIT-bit	Output data code Min~Max	Notes
[0]	Y: 1~254 Cb, Cr: 1~254	Default
[1]	Y: 16~235 Cb, Cr: 16~240	

All internal calculating operations are made with Min = 1, Max = 254.
With 601LIMIT-bit set to [1], codes 1~15 and 236~254 are respectively clipped to 16,235.

○TRSVSEL-bit: Settings for V-bit handling in ITU-R BT.656 format

TRSVSEL-bit	525-line		625-line	
	V-bit=0	V-bit=1	V-bit=0	V-bit=1
[0] ITU-R BT 656-3	Line10~Line263 Line273~Line525	Line1~Line9 Line264~Line272	Line23~Line310 Line336~Line623	Line1~Line22 Line311~Line335 Line624~Line625
[1] ITU-R BT 656-4 SMPTE125M	Line20~Line263 Line283~Line525	Line1~Line19 Line264~Line282		

The TRSVSEL register only available during the interlace output decode by ITU-R BT.601 output size.
These values are unaffected by the VBIL[2:0]-bits setting.

○VBIL[2:0]-bit: Settings for vertical blanking interval

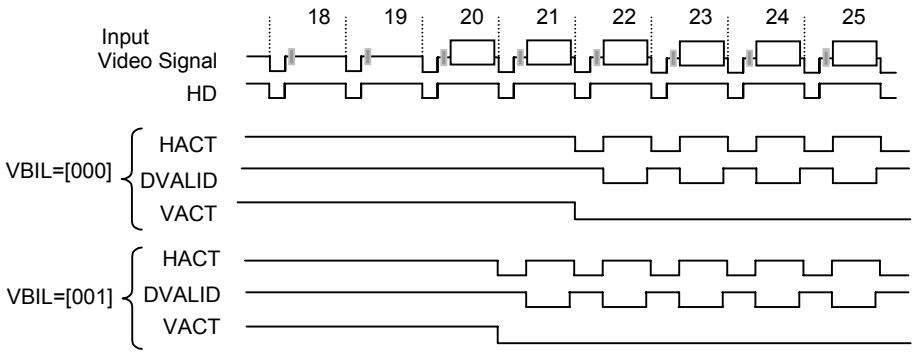
VBIL[2:0]-bit	Line Adjustment width	Notes
[000]	Default	
[001]	1Line advance	*1
	2Line advance	*2
[010]	2Lines advance	*1
	4Lines advance	*2
[011]	3Lines advance	*1
	6Lines advance	*2
[100]	4Lines advance	*1
	8Lines advance	*2
[101]	5Lines advance	*1
	10Lines advance	*2
[110]	6Lines advance	*1
	12Lines advance	*2
[111]	7Lines advance	*1
	14Lines advance	*2

*1: Other than progressive output

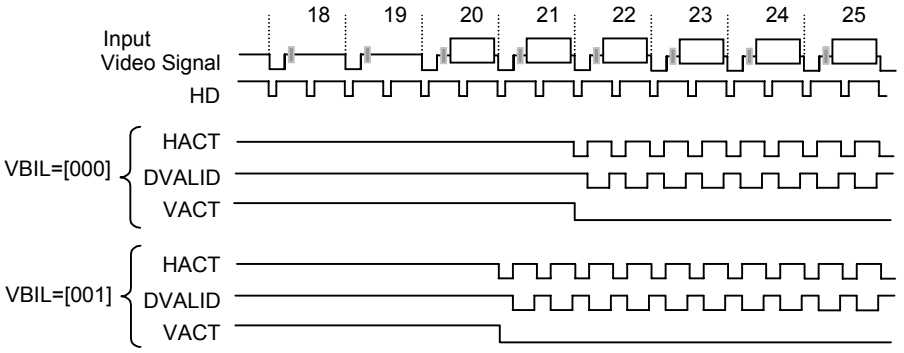
*2: Progressive output

The starting position of HACT signal and DVALID signal is changed according to VACT signal starting position.

*1



*2



○SLLVL-bit: Settings for slice level

SLLVL-bit	Slice level
[0]	25IRE
[1]	50IRE

The results of VBI slicing by the AK8857 slicing function are output as ITU-R BT.601 digital data. The VBI interval is set via VBIL[2:0]-bits. VBI slicing is performed in the luminance signal processing path, so that the Cb/Cr value of the effective line 601 output code is output at the same level as the corresponding luminance signal.
The slice level and the output code are set via the register. The output code value is set via the Hi/Low Slice Data Set Register, as follows.

Hi Slice Data Set Register*: Setting for higher of two values resulting from slicing.
Default: 0xEB(235)

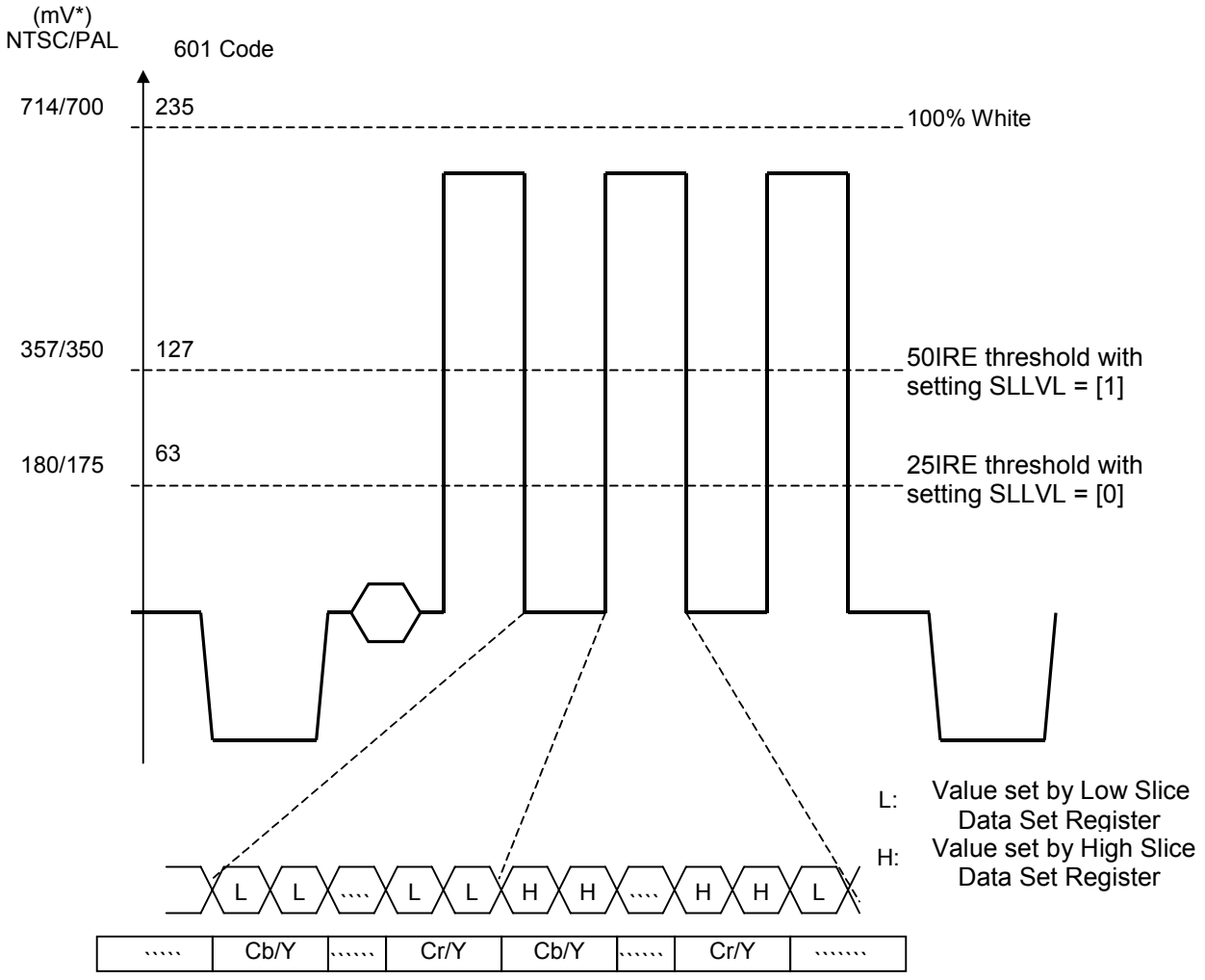
Low Slice Data Set Register*: Setting for lower of two values resulting from slicing.
Default: 0x10(16)

*Note that a setting of 0x00 or 0xFF corresponds to a special 601 code.

○VBIDEC[1:0]-bit: Settings for decode data in the VBI period

VBIDEC[1:0]-bit	Decode data	Notes
[00]	Black level output	Y = 0x10 Cb/Cr = 0x80
[01]	Monochrome mode	Y = data converted to 601 level Cb/Cr = 0x80
[10]	Sliced data output during VBI	Y/Cb/Cr = value corresponding to slice level (Value set at Hi/Low Slice Data Set Register)
[11]	Reserved	Reserved

Note that, with VBI period settings of Lines 1~9 and 263.5~272.5 in the 525 Line and Lines 623.5~6.5 and 311~318 in the 625 Line, the setting VBIDEC[1:0] will not be entered and the output will be in Black level code.



*Threshold values (mV) are approximate.

High/Low conversion is performed for either the Cb/Y or the Cr/Y combination. The above figure is an example of the conversion points for Cb/Y.

Output pin status

For normal operation, the output from the DATA_A[7:0], HD_ACT_A, VD_ACT_A, DVALID_A, FIELD_A, NSIG_A, DATA_B[7:0], HD_ACT_B, VD_ACT_B, DVALID_B, FIELD_B, NSIG_B pins can each be fixed at Low via the Output Control Register.
The black level and blue level output have the priority to be output from the DATA_A[7:0] and DATA_B[7:0] pins regardless of these register settings.
Note, however, that the OE_A, OE_B, PDN, RSTN pins and AINSEL[4:0] (non decode) states will have priority regardless of these register settings.

Output pin timing signal

The timing signal can be output from the HD_ACT_A, VD_ACT_A, DVALID_A, FIELD_A, HD_ACT_B, VD_ACT_B, DVALID_B, FIELD_B pins. The polarity of each timing signal at the output pin can be invert by register setting.
At the HD_ACT output pin, the output signal can be selected between HD signal and HACT signal by register setting.
At the VD_ACT output pin, the output signal can be selected between VD signal and VACT signal by register setting.

○VDACTSEL-bit : VD/ VACT signal output setting

VDACTSEL-bit	VD_ACT output pin setting
[0]	VD signal is output
[1]	VACT signal is output

○HDACTSEL-bit : HD/ HACT signal output setting

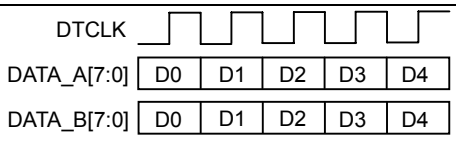
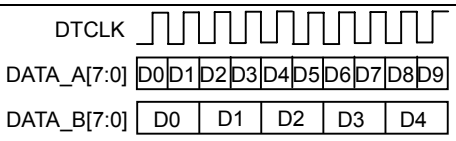
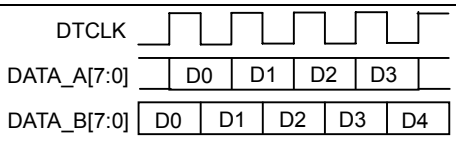
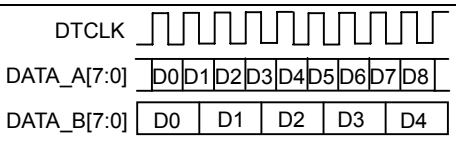
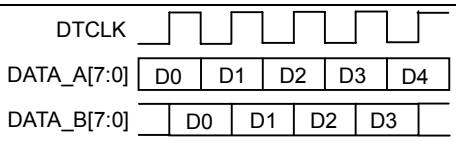
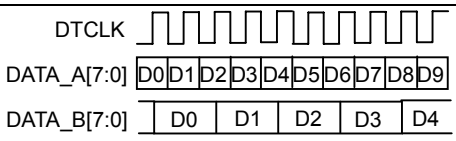
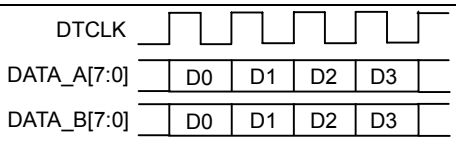
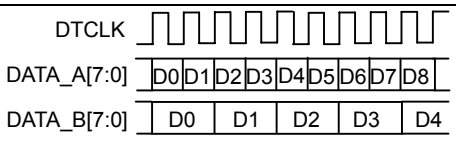
HDACTSEL-bit	HD_ACT output pin setting
[0]	HD signal is output
[1]	HACT signal is output

The polarity of output from the DATA_A[7:0] / DATA_B[7:0] and DTCLKcan be inverted.

○CLKINV-bit: DTCLK signal polarity setting

CLKINV-bit	Polarity setting
[0]	Rising edge
[1]	Falling edge

If each of A or B output 54MHz, DTCLK pin output 54MHz. So, Not IP conversion data is alternated by 2CLK.

CLKINV-bit	A and B block at 27Mhz/54Mhz output	A block : IP conversion output
A Block : CLKINV=[0] B Block : CLKINV=[0]		
A Block : CLKINV=[1] B Block : CLKINV=[0]		
A Block : CLKINV=[0] B Block : CLKINV=[1]		
A Block : CLKINV=[1] B Block : CLKINV=[1]		

Output data timing

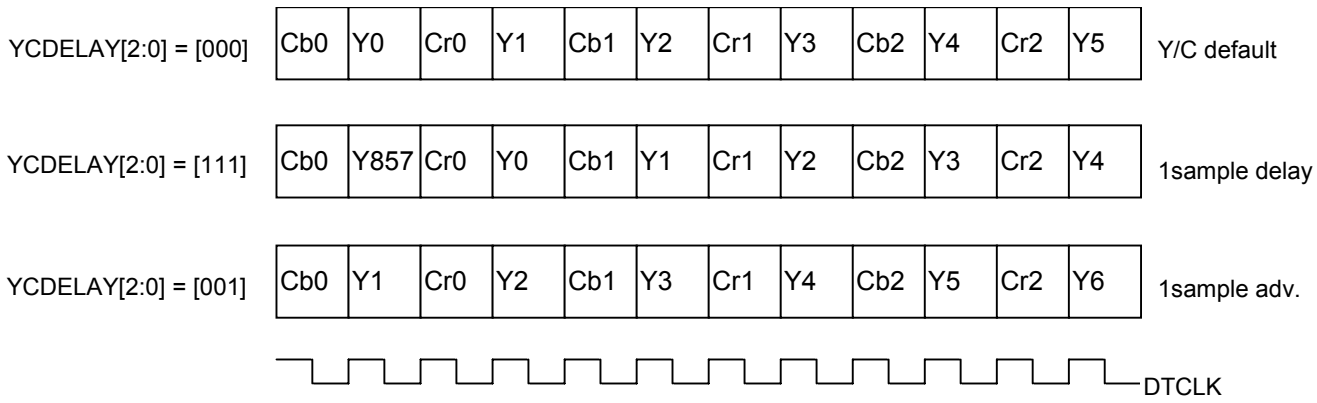
The AK8857 can control timing of output data.

○YCDELAY[2:0]-bit: Adjustment of Y and C timing.

YCDELAY[2:0]-bit	Y and C timing	Notes
[001]	Y advance 1sample toward C.	2clk advance
[010]	Y advance 2 sample toward C.	4clk advance
[011]	Y advance 3 sample toward C.	6clk advance
[000]	No Delay and advance.	Default value
[101]	Y delay 3 sample toward C.	6clk delay
[110]	Y delay 2 sample toward C.	4clk delay
[111]	Y delay 1 sample toward C.	2clk delay
[100]	Reserved	

*Setting by 2 complement

Because each sample is delay/advance toward C, 1sample is equall to 1clk width.

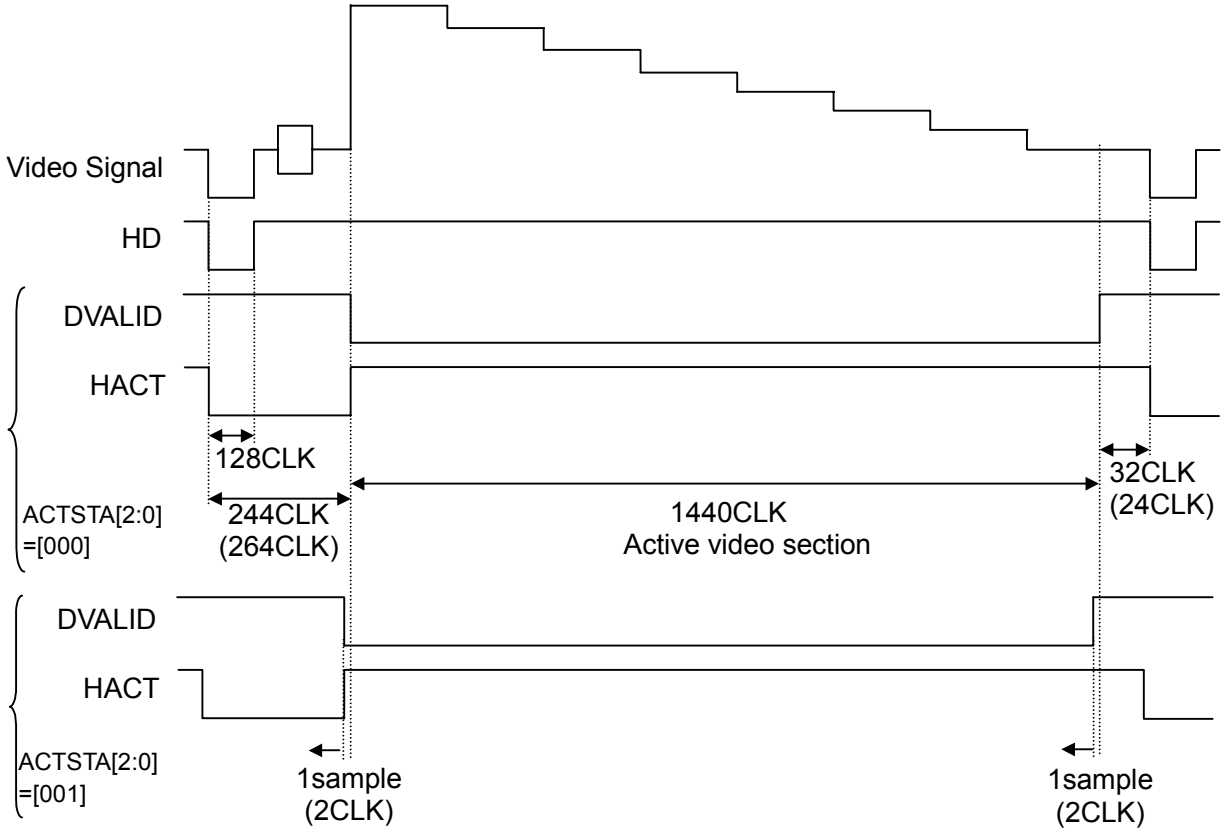


○ACTSTA[2:0]-bit: Adjustment of active video start position

ACTSTA[2:0]-bit	Line and active video start		Notes
[001]	525 Line	Starting postion is delay 1 sample	2clk delay
[010]	525 Line	Starting postion is delay 2 sample	4clk delay
[011]	525 Line	Starting postion is delay 3 sample	6clk delay
[000]	525 Line	Default value	Normal position
[101]	525 Line	Starting postion is advance 3 sample	6clk advance
[110]	525 Line	Starting postion is advance 2 sample	4clk advance
[111]	525 Line	Starting postion is advance 1 sample	2clk advance
[100]	Reserved	Reserved	

When the start position of active video is changed, the end position of active video also changed. (Active video space is fixed)

Example : 720x487, 720x576(ITU-R BT.601)



VLOCK mechanism

The AK8857 synchronizes internal operation with the input signal frame structure. If, for example, the frame structure of the input signal comprises 524 lines, the internal operation will have a structure of 524 lines per frame. This mechanism is termed the VLOCK mechanism. If an input signal changes from a structure of 525 lines per frame to one of 524 lines per frame, internal operation will change accordingly, and the VLOCK mechanism will go to UnLock via a pull-in process. In such case, the UnLock status can be confirmed via the control register [VLOCK-bit]. Note that the time required for locking of the VLOCK mechanism upon channel or other input signal switching will be about 2 frames. (PLL SYNC VLOCK)

Additionary, AK8857 supports “direct locking” mode that is not using VLOCK operation. (Direct SYNC VLOCK)

VLOCKSEL-bit	Internal operation with the input signal frame structure
[0]	PLL SYNC VLOCK
[1]	Direct SYNC VLOCK

(Notice)
“Auto detection function” (Sub-Address0x0E[7]=1, 0x26[7]=1) must not use when it is being operated on Direct SYNC VLOCK.

Auto Gain Control_AGC

The AGC of the AK8857 measures the size of the input sync signal (i.e., the difference between the sync tip and pedestal levels), and adjusts the PGA value to bring the sync signal level to 286[a] or 300[b] mV. The AGC function amplifies the input signal to the appropriate size and enables input to the AD converter. The AGC function in the AK8857 is adaptive, and thus includes peak AGC as well as sync AGC.

Peak AGC is effective for input signals in which the sync signal level is appropriate and only the active video signal is large.

[a] NTSC-M, J; NTSC-4.43; PAL-M……..286mV

[b] PAL-B, D, G, H, I, N; PAL-Nc; PAL-60; SECAM……300mV

○AGCT[1:0]-bit : Settings for AGC time constant

AGCT[1:0]-bit	Time constant	Notes
[00]	Disable	AGC OFF, PGA register enabled.
[01]	Fast	T= 1Field
[10]	Middle	T= 7Fields
[11]	Slow	T= 29Fields

T is the time constant.

Manual setting of the PGA register is possible only if AGC is disabled.

○AGCC-bit : Settings for AGC non-sensing range

AGCC[1:0]-bit	Non-sensing range	Notes
[00]	±2LSB	
[01]	±3LSB	
[10]	±4LSB	
[11]	None	

○AGCFRZ-bit : Settings for freezing AGC function

AGCFRZ-bit	AGC status	Notes
[0]	Non-frozen	
[1]	Frozen	

Note. The gain value at the time of freezing is maintained during the frozen state, and it is then possible to read out the gain value via the PGA1,2 Control Register.

○AGCTL-bit : Settings for selection of quick or slow transition between peak and sync AGC

AGCTL-bit	AGC transition	Notes
[0]	Quick	
[1]	Slow	

Auto Color Control (ACC)

The ACC of the AK8854 measures the level of the input signal color burst, and adjusts the level to 286 or 300 mV, as appropriate. The ACC is not applicable to SECAM input.
As in AGC, both ACC time constant and ACC freeze settings can be entered.

NTSC-M,J , NTSC-4.43 , PAL-M……..286mV
PAL-B,D,G,H,I,N , PAL-Nc , PAL-60……. 300mV

○ACCT[1:0]-bit : Settings for ACC time constant

ACCT[1:0]-bit	Time constant	Notes
[00]	Disable	ACC OFF
[01]	Fast	T= 2Fields
[10]	Middle	T= 8Fields
[11]	Slow	T= 30Fields

○ACCFRZ-bit : Settings for freezing ACC function

ACCFRZ-bit	ACC status	Notes
[0]	Non-frozen	
[1]	Frozen	

The ACC and Color saturation functions operate independently. If ACC is enabled, the color saturation adjustment is applied to the signal that has been adjusted to the appropriate level by the ACC.

No-signal output

If no input signal is found (as shown by the control bit NOSIG-bit), the output signal is black-level, blue level (blueback), or input-state (sandstorm), depending on the register setting.

○NSIGMD-bit : Settings for output signals for no input signal

NSIGMD [1:0]-bit	Output	Notes
[00]	Black-level	
[01]	Blue-level (blueback)	
[10]	Input-state (sandstorm)	
[11]	Reserved	

Y/C separation

The adaptive two-dimensional Y/C separation of the AK8857 utilizes a correlation detector to select the best-correlated direction from among vertical, horizontal, and diagonal samples, and selects the optimum Y/C separation mode. For NTSC-4.43, PAL-60, and SECAM inputs, the Y/C separation is one-dimensional only, regardless of the setting.

○YCSEP[1:0]-bit : Settings for Y/C separation method

YCSEP[1:0]-bit	Y/C separation mode	Notes
[00]	Adaptive	
[01]	1-D	1D (BPF)
[10]	2-D	NTSC-M, J, PAL-M: 3 Line 2-D PAL-B, D, G, H, I, N, Nc: 5 Line 2-D (*1)
[11]	Reserved	

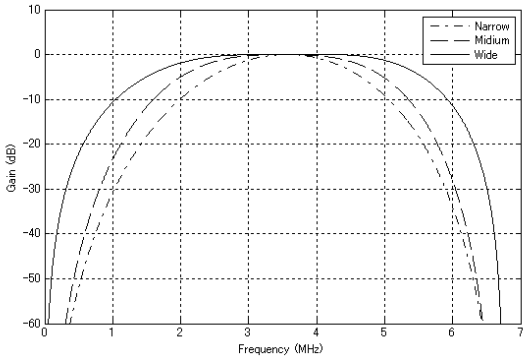
For NTSC-4.43, PAL-60, and SECAM inputs, Y/C separation is 1-D only, regardless of the setting.

C filter

The bandwidth of the C filter can be set via the register, as follows.

○C358FIL[1:0]: Settings for C filter bandwidth, for input signal with 3.58 MHz subcarrier wave

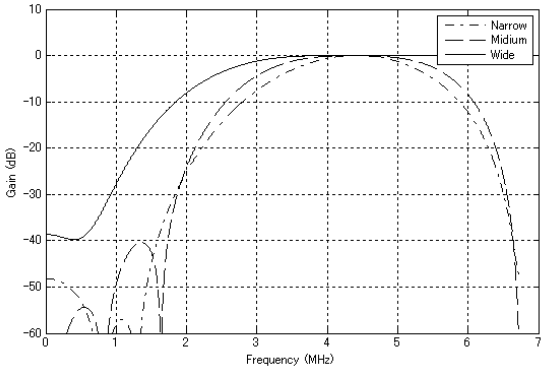
C358FIL[1:0] -bit	C filter bandwidth setting	Notes
[00]	Narrow	NTSC-M, J, PAL-M, PAL-Nc
[01]	Medium	
[10]	Wide	
[11]	Reserved	



○C443FIL[1:0]: Settings for C filter bandwidth, for input signal with 4.43 MHz subcarrier wave

C443FIL[1:0] -bit	C filter bandwidth setting	Notes
[00]	Narrow	PAL-B,D,G,H,I,N , NTSC-4.43 , PAL-60
[01]	Medium	
[10]	Wide	
[11]	Reserved	

Note. No bandwidth selection is possible for SECAM input.

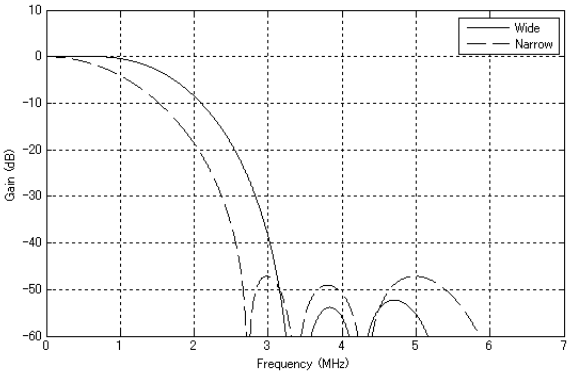


UV filter

The UV bandwidth can be changed by switch between low pass filters types for the demodulated C signal.

○UVFILSEL-bit : Settings for UV filter switching (CVBS or S-video input)

UVFILSEL–bit	Bandwidth	Notes
[0]	Wide	
[1]	Narrow	



Digital Pixel Interpolator

The digital pixel interpolator of the AK8857 aligns vertical pixel positions and it also aligns horizontal pixel position in fixed-clock operating modes.

○INTPOLOFF-bit : Settings for pixel interpolator operation

INTPOLOFF-bit	Interpolator operation	Notes
[0]	ON	
[1]	OFF	

Clock

The AK8857 is operational by fixed-clock. To synchronized analog video signal, it doesn't have PLL internally. The input clock is 27Mhz. Only when progressive output of 720x487, VGA, WVGA output format, the data is sampling to 54Mhz generated internally from the input clock 27Mhz.

Phase correction

In PAL-B, D, G, H, I, N, Nc, 60, and M decoding, the AK8857 performs phase correction for each line. With this function ON, color averaging is performed for each line. In the adaptive phase correction mode, interline phase correlation is sampled and color averaging is performed for correlated samples. Interline color averaging is also performed in NTSC-M and J decoding.

No phase correction or color averaging is performed in SECAM decoding.

○DPAL[1:0]-bit : Settings for phase correction

DPAL[1:0]-bit	Status	Notes
[00]	Adaptive phase correction mode	
[01]	Phase correction ON	
[10]	Phase correction OFF	
[11]	Reserved	

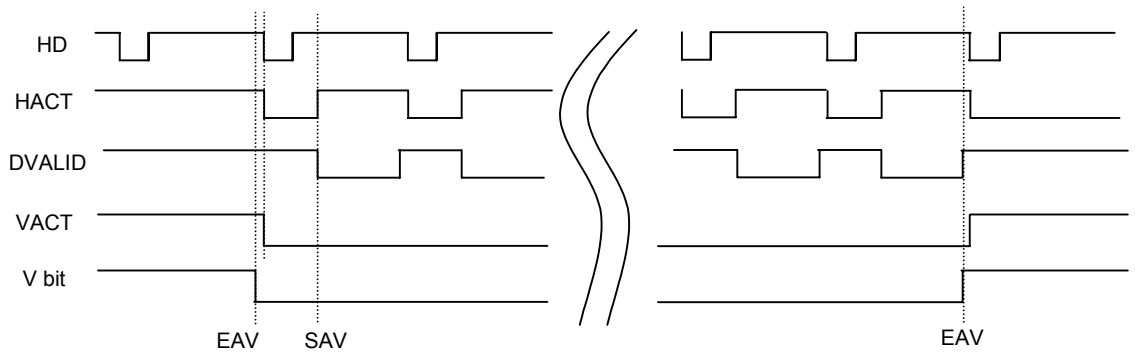
Output interface

[1] Interface with EAV/SAV Sync

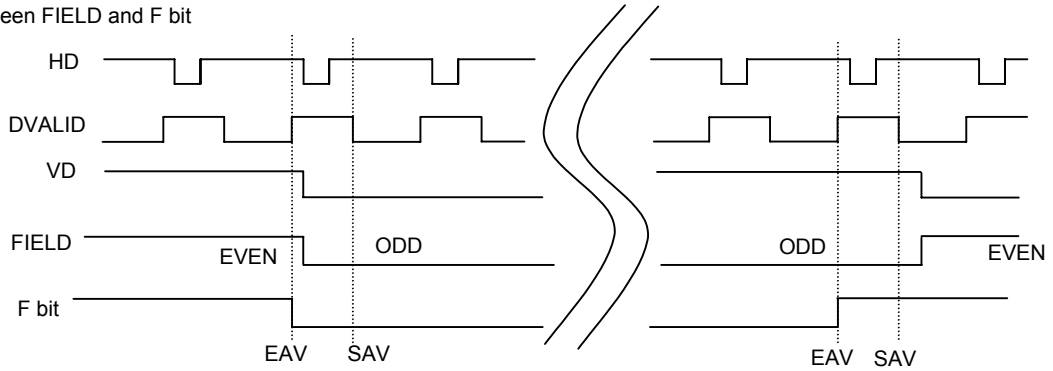
The EAV/SAV Sync code of ITU-R BT.656 standard interface can be added to the output data of AK8857 when ITU-R BT.601 output size interlaced format is selected.

For the output size other than ITU-R BT.601 output size format, 2 pixels is added to the EAV/SAV Sync code at the outside of DVALID signal active section. The changes also apply to V bit and Fbit according to the lines where the polarity of VACT signal and FIELD signal is changed.

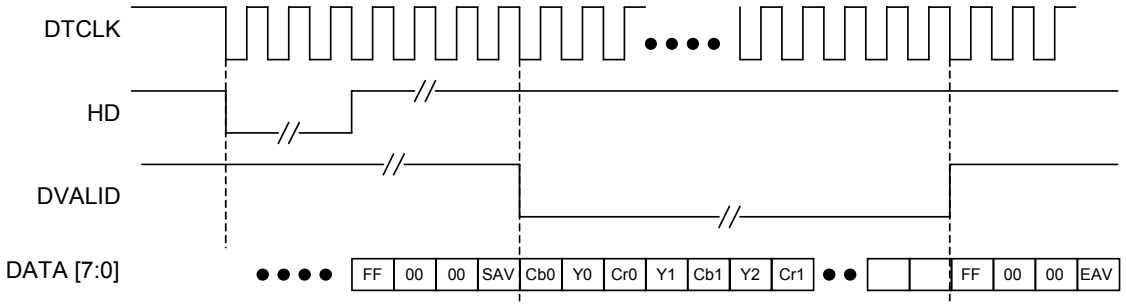
Relation between VACT and V bit



Relation between FIELD and F bit



Realtion between DVALID and EAV/SAV Sync



Since the AK8857 data is sampling using fixed-clock, the sample number from EAV to SAV is not guarantee. For that reason, the default data output is in SAV format.

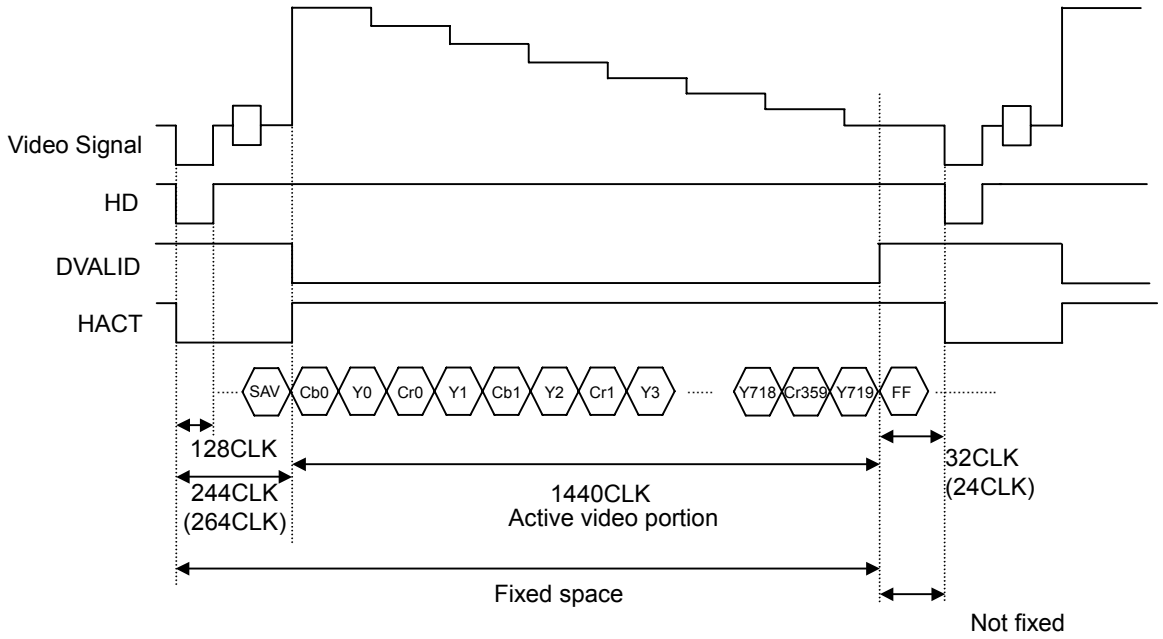
○EAVSAV-bit : EAV/SAV sync code is superimposed to the output data setting.

EAVSAV-bit	Status	Notes
[0]	Add	Default value
[1]	No change	

[2] Interface with Timing signal

The AK8857 can output the HD signal, VD signal, HACT signal, VACT signal, DVALID signal and FIELD signal at the output pins. Please refer to the Output Data Format setting for the correct timing of each signal.

The space between DVALID signal is changed from low to high, and HD/HACT signals is changed from high to low is not guarantee and for that reason the sample number for 1 line also is not guarantee. But the space between HD/HACT signals is changed from high to low and DVALID signal is changed from low to high, the timing is fixed.



Automatic setup processing

In auto detection mode, the AK8857 can perform automatic setup processing in accordance with the detected signal.

Setup processing of the signal to be decoded consists of the following.

Luminance signal: Y=(Y-7.5)/0.925

Color signal: U=U/0.925, V=V/0.925

Automatic setup processing (AK8857 in auto detection mode)

Detected signal	Register setting		Detected signal setup processing status
	Setup-bit	STUPATOFF-bit (Automatic setup processing)	
NTSC-M,J PAL-B,D,G,H,I,N PAL-Nc , 60 SECAM	[0]	[0]	Disable
		[1]	Disable
	[1]	[0]	Enable
		[1]	Enable
PAL-M NTSC-4.43	[0]	[0]	Enable
		[1]	Disable
	[1]	[0]	Enable
		[1]	Enable

In the auto detection mode, the setup processing status will be determined by the register setting on the basis of the detected signal category, with no detection as to the presence or absence of input signal setup.

PGA (programmable gain amp)

The AK8857 digital PGA is buit internally.

The setting value can be set in range of −3dB to 10dB using ADC output data.

The register default setting is 0x1F (=0dB).

When analog video signal (0.5Vpp) is input to AIN ch, the setting value becomes the default value.

$$G = 20\log\left[\frac{0.625 - \{0.006 \times (31 - PGA)\}}{0.625}\right]$$

G：PGA gain(dB)

PGA：PGA register setting(Dec.)

○PGA1[7:0]-bit : Sets the PGA value.

○PGA2[7:0]-bit : Sets the PGA value.

CVBS input : PGA1 is enable for A Block data output and PGA2 is enable for B Block data output.

S-video input : PGA1 is enable for luminance signal and PGA2 is enable for color signal.

Notes : If the output of A block and B block are selected from the same AIN ch, only PGA1 setting is valid and PGA2 is not valid.

This register can read the AGC setting value.

If AGC is enabled, the PGA[7:0]-bits setting value has no effect, and the PGA setting can be manually entered in the register only if AGC is disabled.

Signal input to the AK8857 should be made with the input level attenuated approximately 39% (-8.19 dB) by resistance splitting.

Sync separation, sync detection, and black-level fine tuning

The AK8857 performs sync separation and sync detection on the digitized input signal, uses the detected sync signal as the timing reference for the decoding process, and calculates the phase error from the separated sync signal and applies it to control of the sampling clock. Black-level tuning can be performed in the sync separation block. The black-level fine-tuning band, which is 10 bits wide before REC 601 conversion, can be adjusted -8~+7 LSB in 1-LSB steps, with one step resulting in a change of about 0.4 LSB in the output code

○BKLVL[3:0]-bit : Settings for black-level fine tuning

BKLVL[3:0]-bit	Code adjustment of black level	Approx. change in 601 level (LSB)
[0001]	+1	+0.4
[0010]	+2	+0.8
[0011]	+3	+1.2
[0100]	+4	+1.6
[0101]	+5	+2.0
[0110]	+6	+2.4
[0111]	+7	+2.8
[0000]	Default	None
[1000]	-8	-3.2
[1001]	-7	-2.8
[1010]	-6	-2.4
[1011]	-5	-2.0
[1100]	-4	-1.6
[1101]	-3	-1.2
[1110]	-2	-0.8
[1111]	-1	-0.4

The black level is adjusted upward or downward by the value of the setting, which must be in 2's-complement form. Black-level adjustment is also enabled during the vertical blanking interval.

Digital pedestal clamp

The digitally converted input signal is clamped in the digital signal processing block. The internal clamp position depends on the input signal type (either 286 mV sync or 300 mV sync), but pedestal position is output as code 16 for both types. The digital pedestal clamp function can adjust the time constant and set the coring level.

○DPCT[1:0]-bit : Settings for digital pedestal clamp time constant

DPCT[1:0]-bit	Transition time constant	Notes
[00]	Fast	
[01]	Middle	
[10]	Slow	
[11]	Disable	Digital pedestal clamp OFF

○DPCC[1:0]-bit : Settings for digital clamp pedestal coring level

DPCC[1:0]-bit	Transition time constant (bit)	Notes
[00]	±1bit	
[01]	±2bit	
[10]	±3bit	
[11]	Non-coring	

Color killer

In CVBS or S-video input, the chroma signal quality of the input signal is determined by comparison of its color burst level against the threshold setting in the color killer control register. If the level is below the threshold, the color killer is activated, resulting in processing of the input as a monochrome signal and thus with CbCr data fixed at 0x80. Depending on the register setting, the color killer may also be activated by failure of the color decode PLL lock.

○COLKILL-bit: Settings for color killer ON and OFF

COLKILL-bit		Notes
[0]	Enable	
[1]	Disable	

○CKLVL[3:0]-bit: For threshold setting; default setting [1000] = −23dB.

○CKSCM[1:0]-bit: Used for threshold setting with SECAM input

CKSCM [1:0]		Notes
[00]	{CKLVL [3:0]}	
[01]	{0, CKLVL [3:1]}	1bit shift to right
[10]	{0,0, CKLVL [3:2]}	2bit shift to right
[11]	Reserved	

○CKILSEL: Settings for color killer activation

CKILSEL-bit	Condition for activation	Notes
[0]	Burst level below threshold setting in CKLVL[3:0]-bits	
[1]	Burst level below threshold setting in CKLVL[3:0]-bits, or Failure of color decode PLL lock	*

* PLL lock for color decode is not activate during SECAM signal is decode. The color killer ON/OFF status also depends on No-signal and Burst-level judgement and will not effect by CKILSEL setting.

Image quality adjustments

Image quality adjustments consist of contrast, brightness, sharpness, color saturation, and hue adjustment. All image quality adjustments are disabled during the vertical blanking interval, but contrast and brightness adjustment can be enabled by the register setting.

1. Contrast adjustment

CONT[7:0]-bits: For contrast adjustment; default value 0x80 (no adjustment)

Contrast adjustment involves multiplication by the gain factor setting in this register. The equation of the multiplication can be modified by register setting as follows.

If CONTSEL = [0], then YOUT = (CONT/128) x (YIN – 128) + 128

If CONTSEL = [1], then YOUT = (CONT/128) x YIN

YOUT: Contrast obtained by the calculation

YIN: Contrast before the calculation

CONT: Contrast gain factor (register setting value)

The gain factor can be set in the range 0~255. If the calculated value is outside the specified contrast range, it is clipped to the upper '254' or lower '1' limit. With a control bit 601LIMIT setting of [1], the output will be in the range 16~235.

○CONTSEL-bit : Settings for contrast adjustment Inclination

CONTSEL -bit	Inclination	Notes
[0]	Toward luminance of 128	
[1]	Toward luminance of 0	

2. Brightness adjustment

BR[7:0]-bits: For brightness adjustment; settings in 2's complement;
default value 0x00 (no adjustment)

Brightness adjustment involves multiplication of the 8Bit data luminance signal, after ITU-R BT.601 conversion, by the gain factor setting in this register, as follows.

YOUT = YIN + BR

YOUT: Brightness obtained by the calculation

YIN: Brightness before the calculation

BR: Brightness gain factor (register setting value)

The gain factor can be set in the range -127 to +127 in steps of 1, by 2's complement entry. If the calculated value is outside the specified contrast range, it is clipped to the upper '254' or lower '1' limit. With a control bit 601LIMIT setting of [1], the output will be in the range 16~235.

3. Color saturation adjustment

SAT[7:0]-bits: For color saturation adjustment; default value 0x80 (no adjustment)

Saturation adjustment involves multiplication of the color signal by the gain factor setting in this register. The calculated result is U/V demodulated.

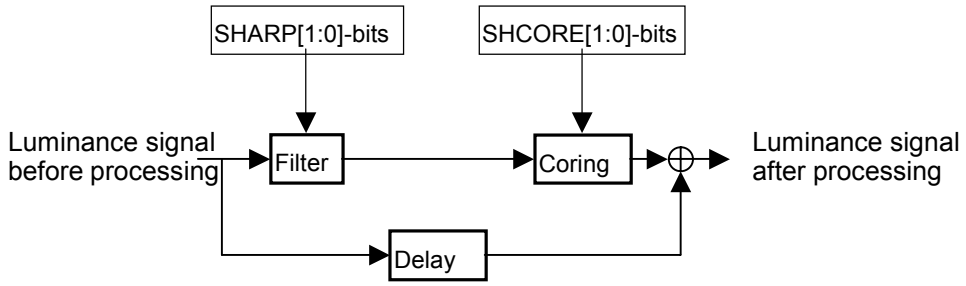
The gain factor can be set in the range 0 to 255/128, in steps of 1/128.

4. Hue adjustment

HUE[7:0]-bits: For hue adjustment; settings in 2's complement; default value 0x00 (no adjustment)
The AK8854 can perform hue rotation with a phase rotation range of ±45° in steps of about 0.35°.

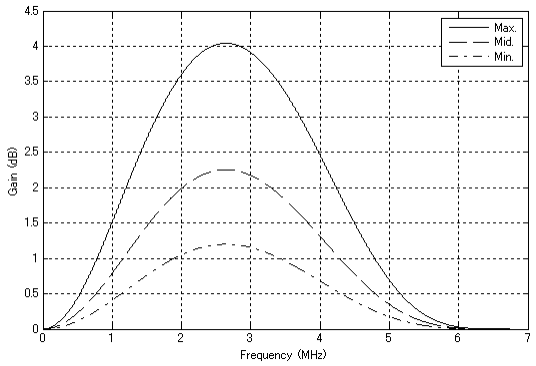
5. Sharpness adjustment

Sharpness adjustment is performed on the luminance signal as shown in the following process diagram. The filter characteristics and the coring level can be selected by following register. A sharp image can be obtained by selection of the filter with the appropriate characteristics.



○SHARP[1:0]-bit: Settings for filter characteristics selection

SHARP[1:0]-bit	Filter characteristics	Notes
[00]	No filtering	Filter disabled
[01]	Min	
[10]	Middle	
[11]	Max	



○SHCORE[1:0]-bit : Settings for coring level after sharpness filtering

SHCORE[1:0]-bit	Coring level (LSB)	Notes
[00]	No coring	Settings apply only to filtered signal.
[01]	±1LSB	
[10]	±2LSB	
[11]	±3LSB	

○VBIIMGCTL-bit: Settings for brightness and contrast adjustment status (ON/OFF) during VBI

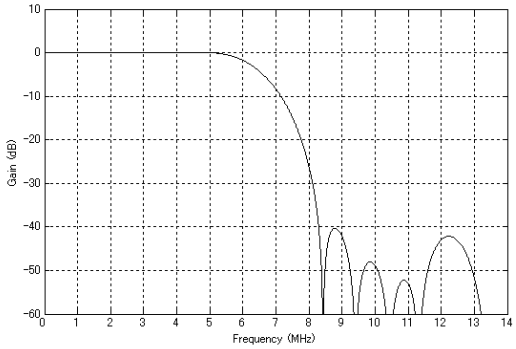
VBIIMGCTL -bit	Status during VBI	Notes
[0]	Disable	
[1]	Enable	

Luminance bandwidth adjustment

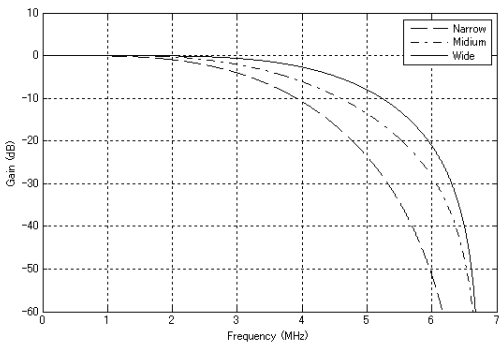
Luminance bandwidth adjustment can be performed for MPEG compression etc. The band-limiting filters for pre-compression limiting can be selected by the following register settings. Without these filters, the frequency response of the luminance signal is determined by the decimation filter.

○LUMFIL[1:0]-bit : Settings for luminance bandwidth filter

LUMFIL [1:0]-bit	Filter characteristic	Notes
[00]	No filter. No bandwidth limit.	-3dB at 6.29MHz
[01]	Narrow	-3dB at 2.94MHz
[10]	Mid	-3dB at 3.30MHz
[11]	Wide	-3dB at 4.00MHz



Luminance signal decimation filter



Luminance bandwidth filter

Sepia output

Sepia-colored output of the decoded signal can be obtained by the following register setting.

○SEPIA-bit : Settings for sepia output of decoded signal
(Sub-address 0x14_[6])

SEPIA –bit	Output	Notes
[0]	Normal	
[1]	Sepia output	

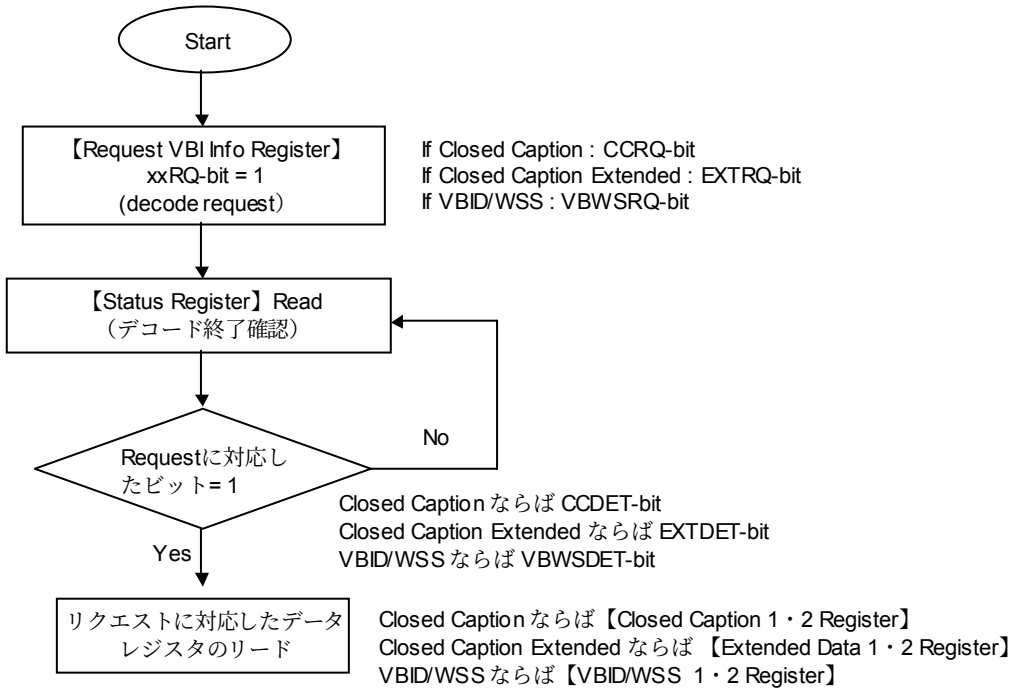
VBI information decoding

The AK8857 decodes closed-caption, closed-caption-extended, VBID(CGMS), and WSS signals on the vertical blanking signal, and writes the decoded data into a storage register. The AK8857 reads each data bit in Request VBI Information Register(R/W)-[3:0] as a decoding request and thereupon enters a data wait state. Data detection and decoding to the storage register are then performed which indicates the presence or absence of data at STATUS 2 Register-[3:0] for host. The host can therefore determine the stored values by reading the respective storage registers. The value in each storage register is retained until a new value is written in by data renewal. For VBID data (CGMS-A), the CRCC code is decoded and only the arithmetic result is stored in the register.

Signal type	Superimposed line	Notes
Closed Caption	Line21	525-Line
Closed Caption Extended Data	Line284	525-Line
VBID	Line20 / 283 Line20 / 333	525-Line 625-Line
WSS	Line23	625-Line

The storage registers for each of the signal types are as follows. For storage bit allocations, please refer to the respective register setting descriptions.

Closed Caption 1 Register, Closed Caption 2 Register
WSS 1 Register, WSS 2 Register
Extended Data 1 Register, Extended Data 2 Register
VBID 1 Register, VBID 2 Register



Internal status indicators

○NOSIG-bit: Indicates presence or absence of signal

NOSIG –bit	Status of signal input	Notes
[0]	Signal detected	
[1]	No signal detected	

○VLOCK-bit: Indicates status of VLOCK

VLOCK-bit	Status of synchronization	Notes
[0]	Synchronized	
[1]	Non-synchronized	

○COLKILON: Indicates status of color killer (ON/OFF)

COLKILON –bit	Status of color killer	Notes
[0]	Not operation	
[1]	Operation	

○SCLKMODE -bit: Indicates status of color killer

SCLKMODE –bit	Clock mode	Notes
[00]	Fixed-clock	
[01]	Line-locked	
[10]	Frame-locked	
[11]	Reserved	

○PKWHITE: Indicates status of luminance decode result after passage through AGC block

PKWHITE –bit	Status of luminance decode result	Notes
[0]	Normal	
[1]	Overflow	

○OVCOL: Indicates status of color decode result after passage through ACC block

OVCOL –bit	Status of color decode result	Notes
[0]	Normal	
[1]	Overflow	

○REALFLD-bit: Indicates decoding signal field status

REALFLD -bit	Decoding field	Notes
[0]	Even	
[1]	Odd	

○AGCSTS-bit: Indicates status of adaptive AGC

AGCSTS -bit	Status of AGC operation	Notes
[0]	Sync AGC operation	
[1]	Peak AGC operation	

○Status 2-Ragister: Indicates closed caption, extended data, VBID, and WSS signal status.

○Input Video Status-Register: Indicates status of automatic input signal detection

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	ST_VSF0 ~ ST_VSF1	Status of Video Sub-Carrier Frequency	R	Input signal subcarrier frequency: [ST_VSF1 : ST_VSF0] (MHz) [00] : 3.57954545 (NTSC-M,J) [01] : 3.57561149 (PAL-M) [10] : 3.58205625 (PAL-Nc) [11] : 4.43361875 (PAL-B,D,G,H,I,N,60 , NTSC-4.43)
bit 2 ~ bit 3	ST_VCEN0 ~ ST_VCEN1	Status of Video Color Encode	R	Input signal color encode format: [ST_VCEN1 : ST_VCEN0] [00] : NTSC [01] : PAL [10] : SECAM [11] : Reserved
bit 4	ST_VLF	Status of Video Line Frequency	R	Input signal line frequency [0]: 525 line (NTSC-M,J, 4.43, PAL-M,60) [1]: 625 line (PAL-B,D,G,H,I,N,Nc , SECAM)
bit 5	ST_BW	Status of B/W Signal	R	Input signal monochrome or non-monochrome : (*1) [0] : Non-monochrome detected [1] : Monochrome
bit 6	UNDEF	Un_define bit	R	Input signal presence or absence (*2) [0] : Input signal detected [1] : No input signal detected
bit 7	FIXED	Input Video Standard fixed bit	R	Input signal detection phase (*3) [0] : Input signal search in progress [1] : Input signal search complete

(*1) Monochrome auto detection is enabled if the color killer setting is ON(COLKILL-bit = [1]).
ST_BW-bit changes to [1] when the color killer operates.
If the user has deliberately entered the B/W-bit setting Sub Address 0x01, input signal detection is limited to 525/625 line detection, and only the ST_VLF information is relevant.

(*2) Shows results of input signal detection.
If an input signal is detected, the value is [0]; if no input signal is detected, the value is [1].

(*3) Shows the operating phase of the automatic input signal detector.
The value is [0] while the detection operation is in progress, and [1] when it is completed; thus, when UNDEF-bit = [1], FIXED-bit = [0].

The VBI information storage registers are as follows.

Closed Caption 1 Register

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0

Closed Caption 2 Register

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8

WSS 1 Register

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
G2-7	G2-6	G2-5	G2-4	G1-3	G1-2	G1-1	G1-0

WSS 2 Register

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	G4-13	G4-12	G4-11	G3-10	G3-9	G3-8

Extended Data 1 Register

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT7	EXT6	EXT5	EXT4	EXT3	EXT2	EXT1	EXT0

Extended Data 2 Register

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT15	EXT14	EXT13	EXT12	EXT11	EXT10	EXT9	EXT8

VBID 1 Register

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	VBID1	VBID2	VBID3	VBID4	VBID5	VBID6

VBID 2 Register

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBID7	VBID8	VBID9	VBID10	VBID11	VBID12	VBID13	VBID14

7.Device control interface

The AK8857 is controlled via I^{2}C bus control interface, as described below.

[I2C bus SLAVE Address]
The I^{2}C slave address can be selected by a SELA pin setting of either [1000100] or [1000101].

	Slave Address							
SELA pin status	MSB							LSB
Pulldown [Low]	1	0	0	0	1	0	0	R/W
Pullup [High]	1	0	0	0	1	0	1	R/W

[I^{2}C Control Sequence]
(1) Write sequence
After receiving a write-mode slave address first byte, the AK8857 receives the sub-address in the second byte and data in the subsequent bytes. The write sequence may be single-byte or multi-byte.

(a) Single-byte write sequence

S	Slave Address	w	A	Sub Address	A	Data	A	Stp
	8-bit		1-bit	8-bit	1-bit	8-bit	1-bit	

(b) Multi-byte write sequence (m-bytes, sequential write operation)

S	Slave Address	w	A	Sub Address (n)	A	Data(n)	A	Data (n+1)	A	,,,,,,	Data (n+m)	A	stp
	8-bit		1-bit	8-bit	1-bit	8-bit	1-bit	8-bit	1-bit		8-bit	1-bit	

(2) Read sequence
After receiving a read-mode salve address as the first byte, the AK8857 sends data in the second and subsequent bytes.

S	Slave Address	w	A	Sub Address (n)	A	rS	Slave Address	R	A	Data1	A	Data 2	A	Data3	A	,,,,
	8-bit		1	8-bit	1		8-bit		1	8-bit	1	8-bit	1	8-bit	1	

,,,,,,,, ,,

Data n	!A	stp
8-bit	1	

Symbols and abbreviations
S : Start Condition
rS : repeated Start Condition
A : Acknowledge (SDA Low)
!A : Not Acknowledge (SDA High)
stp : Stop Condition
R/W 1 : Read 0 : Write
: Received from master device (normally microprocessor)

: Output by slave device (AK8857)

8. Register Definitions

Sub Address	Register	Default	R/W	Block	Function
0x00	Input Channel Select	0x00	R/W	Common	Input channel setting
0x01	AFE Control	0x01	R/W	Common	Analog front-end setting
0x02	Output Control	0x00	R/W	Common	Output data setting
0x03	Start and Delay Control	0x00	R/W	Common	Output data timing adjustment
0x04	Control 1	0x00	R/W	Common	Control register type
0x05	Control 2	0x00	R/W	Common	Control register type
0x06	Pedestal Level Control	0x00	R/W	Common	Pedestal level adjustment
0x07	Color Killer Control	0x08	R/W	Common	Color killer setting
0x08	Image Control	0x00	R/W	Common	Image control setting
0x09	High Slice Data Set	0xEB	R/W	Common	VBI slicer data high setting
0x0A	Low Slice Data Set	0x10	R/W	Common	VBI slicer data low setting
0x0B	PGA Control 1	0x3E	R/W	Common	PGA1 gain setting
0x0C	PGA Control 2	0x3E	R/W	Common	PGA2 gain setting
0x0D	Output Data Format A	0x00	R/W	A	Output data format setting
0x0E	Input Video Standard A	0x00	R/W	A	Input video signal setting
0x0F	NDMODE A	0x00	R/W	A	Auto detection limit setting
0x10	Output Pin Control 0 A	0x00	R/W	A	Output pin status setting
0x11	Output Pin Control 1 A	0x00	R/W	A	Output pin status setting
0x12	AGC & ACC A Control	0x00	R/W	A	AGC and ACC setting
0x13	Control 0 A	0x00	R/W	A	Control register type
0x14	Contrast Control A	0x80	R/W	A	Contrast adjustment
0x15	Brightness Control A	0x00	R/W	A	Brightness adjustment
0x16	Saturation Control A	0x80	R/W	A	Saturation adjustment
0x17	HUE Control A	0x00	R/W	A	Hue adjustment
0x18	Request VBI Infomation A	0x00	R/W	A	VBI interval decode request
0x19	Status 1 A		R	A	Internal status indicator
0x1A	Status 2 A		R	A	Internal status indicator
0x1B	Reserved		R	A	Reserved
0x1C	Input Video Status A		R	A	Input signal detection indicator
0x1D	Closed Caption 1 A		R	A	Closed caption data indicator
0x1E	Closed Caption 2 A		R	A	Closed caption data indicator
0x1F	WSS 1 A		R	A	WSS data indicator
0x20	WSS 2 A		R	A	WSS data indicator
0x21	Extended Data 1 A		R	A	CC-Extended data indicator
0x22	Extended Data 2 A		R	A	CC-Extended data indicator

Sub Address	Register	Default	R/W	Block	Function
0x23	VBID 1 A		R	A	VBID data indicator
0x24	VBID 2 A		R	A	VBID data indicator
0x25	Output Data Format A	0x00	R/W	B	Output data format setting
0x26	Input Video Standard B	0x00	R/W	B	Input video signal setting
0x27	NDMODE B	0x00	R/W	B	Auto detection limit setting
0x28	Output Pin Control 0 B	0x00	R/W	B	Output pin status setting
0x29	Output Pin Control 1 B	0x00	R/W	B	Output pin status setting
0x2A	AGC & ACC B Control	0x00	R/W	B	AGC and ACC setting
0x2B	Control 0 B	0x00	R/W	B	Control register type
0x2C	Contrast Control B	0x80	R/W	B	Contrast adjustment
0x2D	Brightness Control B	0x00	R/W	B	Brightness adjustment
0x2E	Saturation Control B	0x80	R/W	B	Saturation adjustment
0x2F	HUE Control B	0x00	R/W	B	Hue adjustment
0x30	Request VBI Infomation B	0x00	R/W	B	VBI interval decode request
0x31	Status 1 B		R	B	Internal status indicator
0x32	Status 2 B		R	B	Internal status indicator
0x33	Reserved		R	B	Reserved
0x34	Input Video Status B		R	B	Input signal detection indicator
0x35	Closed Caption 1 B		R	B	Closed caption data indicator
0x36	Closed Caption 2 B		R	B	Closed caption data indicator
0x37	WSS 1 B		R	B	WSS data indicator
0x38	WSS 2 B		R	B	WSS data indicator
0x39	Extended Data 1 B		R	B	CC-Extended data indicator
0x3A	Extended Data 2 B		R	B	CC-Extended data indicator
0x3B	VBID 1 B		R	B	VBID data indicator
0x3C	VBID 2 B		R	B	VBID data indicator
0x3D	Device and Revision ID		R	Common	Device ID and revision ID indicator

For all other registers, write-in is prohibited.
For all reserved registers, write-in must be limited to the default value.

“Common” is Common Register
To R/W register to A block and B block can be done by REGSEL bit setting of Sub-address”0x00”.
For R/W of [Input Channel Select], [PGA Control 1], [PGA Control 2], [Device and Revision ID] register, REGSEL bit setting is not necessary.

“A” is referred to A block register. “B” is referred to B block register.

9. Register settings overview

Input Channel Select Register (R/W) [Sub Address 0x00]

Input signal channel selection and clock mode selection register.

Sub Address 0x00 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	Bit 1	bit 0
P1DRV1	P1DRV0	REGSEL	AINSEL4	AINSEL3	AINSEL2	AINSEL1	AINSEL0
Default Value							
0	0	0	0	0	0	0	0

Input Channel Select Register Definition

Bit	Register Name		R / W	Definition
bit 0 ~ bit 4	AINSEL0 ~ AINSEL4	Analog Input Select	R / W	A block and B lock output video signal selection : [AINSEL4: AINSEL0] [00000]: [A]: AIN1(CVBS), [B]: AIN4(CVBS) [00001]: [A]: AIN1(CVBS), [B]: AIN3(CVBS) [00010]: [A]: AIN1(CVBS), [B]: AIN2(CVBS) [00011]: [A]: AIN1(CVBS), [B]: AIN1(CVBS) (*2) [00100]: [A]: AIN1(CVBS), [B]: Non-decode(*1) [00101]: [A]: AIN2(CVBS), [B]: AIN4(CVBS) [00110]: [A]: AIN2(CVBS), [B]: AIN3(CVBS) [00111]: [A]: AIN2(CVBS), [B]: AIN2(CVBS) (*2) [01000]: [A]: AIN2(CVBS), [B]: AIN1(CVBS) [01001]: [A]: AIN2(CVBS), [B]: Non-decode (*1) [01010]: [A]: AIN3(CVBS), [B]: AIN4(CVBS) [01011]: [A]: AIN3(CVBS), [B]: AIN3(CVBS) (*2) [01100]: [A]: AIN3(CVBS), [B]: AIN2(CVBS) [01101]: [A]: AIN3(CVBS), [B]: AIN1(CVBS) [01110]: [A]: AIN3(CVBS), [B]: Non-decode (*1) [01111]: [A]: AIN4(CVBS), [B]: AIN4(CVBS) (*2) [10000]: [A]: AIN4(CVBS), [B]: AIN3(CVBS) [10001]: [A]: AIN4(CVBS), [B]: AIN2(CVBS) [10010]: [A]: AIN4(CVBS), [B]: AIN1(CVBS) [10011]: [A]: AIN4(CVBS), [B]: Non-decode (*1) [10100]: [A]: Non-decode, [B]: AIN4(CVBS) (*1) [10101]: [A]: Non-decode, [B]: AIN3(CVBS) (*1) [10110]: [A]: Non-decode, [B]: AIN2(CVBS) (*1) [10111]: [A]: Non-decode, [B]: AIN1(CVBS) (*1) [11000]: [A]: AIN1(Y) / AIN3(C), [B]: Non-decode (*1, *2) [11001]: [A]: AIN1(Y) / AIN3(C), [B]: AIN1(Y) / AIN3(C) (*1, *2) [11010]: [A]: AIN2(Y) / AIN4(C), [B]: Non-decode (*1, *2) [11011]: [A]: AIN2(Y) / AIN4(C), [B]: AIN2(Y) / AIN4(C) (*1, *2) [11100]: [A]: Non-decode, [B]: AIN1(Y) / AIN3(C) (*1, *2) [11101]: [A]: Non-decode, [B]: AIN2(Y) / AIN4(C) (*1, *2)

bit 5	REGSEL	Register Select	R / W	Common register setting method selection (*2) [0]: A block : Write/ Read enable [1]: B block : Write/ Read enable
bit 6 ~ bit 7	P1DRV0 ~ P1DRV1	PVDD1 Drive	R / W	The digital P1 output pin buffer drive setting is set according to PVDD1 input voltage setting.(*3) [P1DRV1: P1DRV0] [00]: PVDD1 = 3.0 ~ 3.6V [01]: PVDD1 = 2.3 ~ 2.7V [10]: Reserved [11]: PVDD1 = 1.7 ~ 2.0V

(*1) If [Non-decode] is select at the output block, the output pins will be in powersave mode and the internal digital circuit operational is stop. This will save the power consumption.

(*2) If the output of A block and B block is selected from the same channel of input video signal, the setting of Sub-address0x01 [AFE Control Register] register only enable if REGSEL=[0] and disable if REGSEL=[1].
During S-video signal decode, the output block register setting is enable if REGSEL=[0] and disable if REGSEL=[1].

(*3) Digital P1 pin: DATA_A[7:0], HD_ACT_A, VD_ACT_A, DVALID_A, FIELD_A, DATA_B[7:0], HD_ACT_B, VD_ACT_B, DVALID_B, FIELD_B, DTCLK pin.

AFE Control Register (R/W) [Sub Address 0x01] (Common Register)

Analog front end register setting.
R/W block is depends on REGSEL setting of Sub-Address “0x00”.

Sub Address 0x01 Default Value : 0x01

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLPWIDTH1	CLPWIDTH0	CLPSTAT1	CLPSTAT0	UDG1	UDG0	CLPG1	CLPG0
Default Value							
0	0	0	0	0	0	0	1

AFE Control Register 1 Definition

Bit	Register Name		R / W	Definition
bit 0 ~ bit 1	CLPG 0 ~ CLPG1	Clamp Gain	R / W	Set the current value of fine clamp in analog block [00]: Min. [01]: Middle 1 (Default) [10]: Middle 2 [11]: Max
bit 2 ~ bit 3	UDG 0 ~ UDG 1	Up Down Gain	R / W	Set the current value of rough clamp in analog block. [00]: Min. (Default) [01]: Middle 1 [10]: Middle 2 [11]: Max
bit 4 ~ bit 5	CLPSTAT0 ~ CLPSTAT1	Clamp Start	R / W	Set the position of clamp pulse [CLPSTAT1 : CLPSTAT0] [00] : Center of horizontal sync [01] : (1/128) H delay [10] : (2/128) H advance [11] : (1/128) H advance
bit 6 ~ bit 7	CLPWIDTH0 ~ CLPWIDTH1	Clamp Pulse Width	R / W	Set the width of clamp pulse. [CLPWIDTH1 : CLPWIDTH0] [00] : 296nsec [01] : 593nsec [10] : 1.1usec [11] : 2.2usec

If the output of A block and B block is selected from the same channel of input video signal, the setting of Sub-address0x01 [AFE Control Register] register only enable if REGSEL=[0] and disable if REGSEL=[1].
During S-video signal decode, the output block register setting is enable if REGSEL=[0] and disable if REGSEL=[1].

Output Control Register (R/W) [Sub Address 0x02] (Common register)

Output data setting register.
R/W block is depends on REGSEL setting of Sub-Address “0x00”.

Sub Address 0x02 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBIDEC1	VBIDEC0	SLLVL	TRSVSEL	601LIMIT	VBIL2	VBIL1	VBIL0
Default Value							
0	0	0	0	0	0	0	0

Output Format Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 2	VBIL0 ~ VBIL2	Vertical Blanking Length	R/W	VACT signal active starting position adjustment. [VBIL2 : VBIL0] [000]: Default [001]: 1Line (2Line*) advance [010]: 2Line (4Line*) advance [011]: 3Line (6Line*) advance [100]: 4Line (8Line*) advance [101]: 5Line (10Line*) advance [110]: 6Line (12Line*) advance [111]: 7Line (14Line*) advance
bit 3	601LIMIT	601 Output Limit	R/W	Output data code limit (Min-Max) setting [0] : 1-254 (Y/Cb/Cr) [1] : 16-235 (Y) /16-240 (Cb/Cr)
bit 4	TRSVSEL	Time Reference Signal V Select	R/W	Setting of lines for “Time reference signal” V-bit value change in ITU-R BT.656 format With 525-line input Setting [0]: V=1 (lines 1~9 and 264~272) V=0 (lines 10~263 and 273~525) Setting [1]: V=1 (lines 1~19 and 264~282) V=0 (lines 20~263 and 283~525) With 625-line input Always (regardless of setting in this register): V=1 (lines 1~22 and 311~335) V=0 (lines 23~310 and 336~623)
bit 5	SLLVL	Slice Level	R/W	Slice level setting [0] : Slice level approx. 25 IRE [1] : Slice level approx. 50 IRE
bit 6 ~ bit 7	VBIDEC0 ~ VBIDEC1	VBI Decode	R/W	Setting for type of data output during interval set in Vertical Blanking Interval register * [VBIDEC1 : VBIDEC0] [00] : Black level data output [01] : Monochrome data output [10] : Slice result data output [11] : Reserved

*Only support progressive output size of ITU-R BT.601, VGA, WVGA format.

Start and Delay Control Register (R/W) [Sub Address 0x03] (Common register)

Output data timing adjustment register.
R/W block is depends on REGSEL setting of Sub-Address “0x00”.

Sub Address 0x03 Default Value : 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VLOCKSEL	ACTSTA2	ACTSTA1	ACTSTA0	Reserved	YCDELAY2	YCDELAY1	YCDELAY0
Default Value							
0	0	0	0	0	0	0	0

Start and Delay Control Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 2	YCDELAY0 ~ YCDELAY2	Y/C Delay Control	R/W	Adjustment of Y and C timing. [YCDELAY2 : YCDELAY0] [001] : Y advance 1sample toward C. [010] : Y advance 2sample toward C. [011] : Y advance 3sample toward C. [000] : No Delay and advance. [101] : Y delay 3 sample toward C. [110] : Y delay 2 sample toward C. [111] : Y delay 1 sample toward C. [100] : Reserved
bit 3	Reserved	Reserved	R/W	Reserved
bit 4 ~ bit 6	ACTSTA0 ~ ACTSTA2	Active Video Start Control	R/W	Fine-tuning video data decode start position by delay or advance in 1-sample units. [ACTSTA2: ACTSTA0] [001]: 1-sample delay [010]: 2-sample delay [011]: 3-sample delay [000]: Normal start position [101]: 3-sample advance [110]: 2-sample advance [111]: 1-sample advance [100]: Reserved
bit 7	VLOCKSEL	Vlock Select	R/W	Select of internal operation with the input signal frame structure [0]: PLL SYNC VLOCK [1]: Direct SYNC VLOCK

Control 1 Register (R/W) [Sub Address 0x04] (Common register)

Control register setting.
R/W block is depends on REGSEL setting of Sub-Address “0x00”.

Sub Address 0x04 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	EAVSAV	CLKINV	INTPOLOFF	Reserved	UVFILSEL	YCSEP1	YCSEP0
Default Value							
0	0	0	0	0	0	0	0

Control 1 Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 1	YCSEP0 ~ YCSEP1	YC Separation Control	R/W	Y/C separation setting [YCSEP1 : YCSEP0] [00] : Adaptive Y/C separation [01] : 1-dimensional Y/C separation [10] : 2-dimensional Y/C separation [11] : Reserved
bit 2	UVFILSEL	UV Filter Select	R/W	UV filter setting [0]: Wide [1]: Narrow
bit 3	Reserved	Reserved	R/W	Reserved
bit 4	INTPOLOFF	Interpolator Mode Select	R/W	Pixel interpolator setting [0]: ON [1]: OFF
bit 5	CLKINV	CLK Invert Set	R/W	DTCLK signal output polarity selection [0] : Normal output (write in data at rising edge) [1] : Data and clock reversed (write in data at falling edge)
bit 6	EAVSAV	EAV/ SAV SELECT	R/W	EAV/SAV sync code add setting [0]: Sync code is added [1]: not added.
bit 7	Reserved	Reserved	R/W	Reserved

Control 2 Register (R/W) [Sub Address 0x05] (Common register)

Control register setting.
R/W block is depends on REGSEL setting of Sub-Address “0x00”.

Sub Address 0x05 Default Value : 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CKILSEL	STUPATOFF	Reserved	Reserved	Reserved	Reserved	DPAL1	DPAL0
Default Value							
0	0	0	0	0	0	0	0

Control 2 Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 1	DPAL0 ~ DPAL1	Deluxe PAL	R/W	Setting for color averaging* (PAL phase correction block) [DPAL1 : DPAL0] [00] : Adaptive phase correction ON [01] : Phase correction ON [10] : Phase correction OFF [11] : Reserved
bit 2 ~ bit 5	Reserved	Reserved	R/W	Reserved
bit 6	STUPATOFF	Setup Auto Control Off	R/W	Setup auto switching setting (ON/OFF) in auto signal detection mode [0] : Auto setup switching ON [1] : Auto setup switching OFF
bit 7	CKILSEL	Color killer Select	R/W	Color killer activation setting [0] : Activation when burst color level is below CKLVL[3:0]-bits threshold setting [1] : Activation when burst color level is below CKLVL[3:0]-bits threshold setting or color decode PLL lock fails

Pedestal Level Control Register (R/W) [Sub Address 0x06] (Common register)

Pedestal level adjustment setting register.
R/W block is depends on REGSEL setting of Sub-Address “0x00”.

Sub Address 0x06 Default Value : 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DPCC1	DPCC0	DPCT1	DPCT0	BKLVL3	BKLVL2	BKLVL1	BKLVL0
Default Value							
0	0	0	0	0	0	0	0

Pedestal Level Control Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 3	BKLVL0 ~ BKLVL3	Black Level	R/W	Setting for change from current pedestal level by adding to or subtracting from black level [BKLVL3 : BKLVL0] [0001] : Add 1 [0010] : Add 2 [0011] : Add 3 [0100] : Add 4 [0101] : Add 5 [0110] : Add 6 [0111] : Add 7 [0000] : Default [1000] : Subtract 8 [1001] : Subtract 7 [1010] : Subtract 6 [1011] : Subtract 5 [1100] : Subtract 4 [1101] : Subtract 3 [1110] : Subtract 2 [1111] : Subtract 1
bit 4 ~ bit 5	DPCT0 ~ DPCT1	Digital Pedestal Clamp Control	R/W	Time-constant setting for digital pedestal clamp [DPCT1 : DPCT0] [00] : Fast [01] : Middle [10] : Slow [11] : Disable
bit 6 ~ bit 7	DPCC0 ~ DPCC1	Digital Pedestal Clamp Coring Control	R/W	Non-sensing bandwidth setting for digital pedestal clamp [DPCC1 : DPCC0] [00] : ±1bit [01] : ±2bit [10] : ±3bit [11] : No non-sensing band

Color Killer Control Register (R/W) [Sub Address 0x07] (Common register)

Color killer setting register
R/W block is depends on REGSEL setting of Sub-Address “0x00”.

Sub Address 0x07 Default Value : 0x08

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
COLKILL	CONTSEL	CKSCM1	CKSCM0	CKLVL3	CKLVL2	CKLVL1	CKLVL0
Default Value							
0	0	0	0	1	0	0	0

Color Killer Control Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 3	CKLVL0 ~ CKLVL3	Color Killer Level Control	R/W	Burst level setting for color killer activation Default value, approx. −23 dB
bit 4 ~ bit 5	CKSCM0 ~ CKSCM1	Color Killer Level for SECAM	R/W	Burst level setting for color killer activation in SECAM mode Adds 2 bits to CKLVL[3:0]
bit 6	CONTSEL	Contrast Select	R/W	Contrast selector [0] : toward luminance of 128 [1] : toward luminance of 0
bit 7	COLKILL	Color killer Set	R/W	Color killer ON/OFF setting [0] : Enable [1] : Disable

Image Control Register (R/W) [Sub Address 0x08] (Common register)

Sharpness control, Luminance bandwidth filter control, Sepia color output setting and VBI interval setting register.
R/W block is depends on REGSEL setting of Sub-Address “0x00”.

Sub Address 0x08 Default Value : 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBIIMGCTL	SEPIA	LUMFIL1	LUMFIL0	SHCORE1	SHCORE0	SHARP1	SHARP0
Default Value							
0	0	0	0	0	0	0	0

Image Control Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 1	SHARP0 ~ SHARP1	Sharpness Control	R/W	Sharpness control (filter effect) setting [SHARP1 : SHARP0] [00] : No filtering [01] : Min effect [10] : Middle effect [11] : Max effect
bit 2 ~ bit 3	SHCORE0 ~ SHCORE1	Sharpness Coring	R/W	Setting for level of coring after passage through sharpness filter Enabled except with [SHARP1:SHARP0] register setting of [00] [SHCORE1 : SHCORE0] [00] : No coring [01] : ±1LSB [10] : ±2LSB [11] : ±3LSB
bit 4 ~ bit 5	LUMFIL0 ~ LUMFIL1	Luminance Filter	R/W	Setting for luminance band limit filter [LUMFIL1 : LUMFIL0] [00] : No filtering [01] : Narrow [10] : Mid [11] : Wide
bit 6	SEPIA	Sepia Output	R/W	Setting (ON/OFF) for sepia coloring of decode results * [0]: Normal output [1]: Sepia output
bit 7	VBIIMGCTL	VBI Image Control	R/W	Setting (ON/OFF) for image adjustment during brightness and contrast adjustment VBI* [0]: Image adjustment inactive during VBI [1]: Image adjustment active during VBI

* DOA register of Sub-address “0x10” and DOB register of Sub-address “0x28” setting takes priority regardless to above SEPIA register setting.

High Slice Data Set Register (R/W) [Sub Address 0x09] (Common register)

Register for setting sliced data from VBI slicer to High value (Default code is 235).
R/W block is depends on REGSEL setting of Sub-Address “0x00”.

Sub Address 0x09 Default Value : 0xEB

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
H7	H6	H5	H4	H3	H2	H1	H0
Default Value							
1	1	1	0	1	0	1	1

High Slice Data Set Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 7	H0 ~ H7	High Data 0~7 Set	R/W	Register for setting sliced data from VBI slicer to High value (Default code is 235) Important: Corresponds to 601 special code if set to 0x00 or 0xFF

Low Slice Data Set Register (R/W) [Sub Address 0x0A] (Common register)

Register for setting sliced data from VBI slicer to Low value (Default code is 16)
R/W block is depends on REGSEL setting of Sub-Address “0x00”.

Sub Address 0x0A Default Value : 0x10

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
L7	L 6	L 5	L 4	L 3	L 2	L 1	L 0
Default Value							
0	0	0	1	0	0	0	0

Low Slice Data Set Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 7	L0 ~ L7	Low Data 0~7 Set	R/W	Register for setting sliced data from VBI slicer to Low value (Default code is 16) Important: Corresponds to 601 special code if set to 0x00 or 0xFF

PGA Control 1 Register (R/W) [Sub Address 0x0B]

PGA1 control register
In case of CVBS signal decode, its control the gain setting for A block output.
In case of S-Videosignal decode, its control the gain setting for Y signal output.

Sub Address 0x0B Default Value : 0x1F

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PGA1_7	PGA1_6	PGA1_5	PGA1_4	PGA1_3	PGA1_2	PGA1_1	PGA1_0
Default Value							
0	0	1	1	1	1	1	0

PGA Control 1 Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 7	PGA1_0 ~ PGA1_7	PGA1 Gain Set	R/W	PGA gain setting, in steps of approx. 0.1 dB

*1 When CVBS signal decode, if the output of A block and B block is the same video signal, only PGA1 control register is enable and PGA2 control register is disable.
*2 When CVBS signal decode, if the output block is selected to [non-decode], the gain setting is set to “0x00” value.

PGA Control 2 Register (R/W) [Sub Address 0x0C]

PGA2 control register
In case of CVBS signal decode, its control the gain setting for B block output.
In case of S-Videosignal decode, its control the gain setting for C signal output.

Sub Address 0x0C Default Value : 0x1F

bit 7	Bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PGA2_7	PGA2_6	PGA2_5	PGA2_4	PGA2_3	PGA2_2	PGA2_1	PGA2_0
Default Value							
0	0	1	1	1	1	1	0

PGA Control 2 Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 7	PGA2_0 ~ PGA2_7	PGA2 Gain Set	R/W	PGA gain setting, in steps of approx. 0.1 dB

*1 When CVBS signal decode, if the output of A block and B block is the same video signal, only PGA1 control register is enable and PGA2 control register is disable.
*2 When CVBS signal decode, if the output block is selected to [non-decode], the gain setting is set to “0x00” value.

Output Data Format A Register (R/W) [Sub Address 0x0D] (A block register)
Output Data Format A Register (R/W) [Sub Address 0x25] (B block register)

Output Data format setting register.
This register is applied to set the A block output data.

Sub Address 0x0D, 0x25 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	ODEVA ODEVB	ODFORMA3 ODFORMB3	ODFORMA2 ODFORMB2	ODFORMA1 ODFORMB1	ODFORMA0 ODFORMB0
Default Value							
0	0	0	0	0	0	0	0

Output Data Format A Register Definition

Bit	Register Name		R / W	Definition
bit 0 ~ bit 3	ODFORMA/B0 ~ ODFORMA/B3	Output Data Format_A/B	R / W	Output data format selection : [ODFORMA/B3: ODFORMA/B0] [0000] : 601 (Interlace) (525 line : 720x487) (625 line : 720x576) [0001] : 601 (Progressive, 60frm/s) (525 line : 720x487) (625 line : 720x576) [0010] : 601 (Progressive, 30frm/s) (525 line : 720x487) (625 line : 720x576) [0011]: WVGA (Interlace) (800x480) [0100]: WVGA (Progressive, 60frm/s) (800x480) [0101]: WVGA (Progressive, 30frm/s) (800x480) [0110]: VGA (Interlace) (640x480) [0111]: VGA (Progressive, 60frm/s) (640x480) [1000]: VGA (Progressive, 30frm/s) (640x480) [1001]: WQVGA (Progressive, 30frm/s) (400x240) [1010]: QVGA (Progressive, 30frm/s) (320x240) [1011]: EGA (Progressive, 30frm/s) (400x234) [1100]: WEGA1 (Progressive, 30frm/s) (480x240) [1101]: WEGA2 (Progressive, 30frm/s) (480x234)
bit 4	ODEVA/B	ODD EVEN Select_A/B	R / W	Decode field selection during (Progressive, 30frm/s) output. [0]: ODD FIELD [1]: EVEN FIELD
bit 5 ~ bit 7	Reserved	Reserved	R / W	Reserved

Input Video Standard A Register (R/W) [Sub Address 0x0E] (A Block Register)
Input Video Standard A Register (R/W) [Sub Address 0x26] (B Block Register)

This register is applied to set the analog input signal.

Sub Address 0x0E, 0x26 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
AUTODETA AUTODETB	SETUPA SETUPB	BWA BWB	VLFA VLFB	VCENA1 VCENB1	VCENA0 VCENB0	VSCFA1 VSCFB1	VSCFA0 VSCFB0
Default Value							
0	0	0	0	0	0	0	0

Input Video Standard A/B Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 1	VSCFA/B 0 ~ VSCFA/B 1	Video Sub-Carrier Frequency_A/B	R/W	Input video signal subcarrier frequency setting [VSCFA/B 1 : VSCFA/B 0] (MHz) [00] : 3.57954545 (NTSC-M,J) [01] : 3.57561149 (PAL-M) [10] : 3.58205625 (PAL-Nc) [11] : 4.43361875 (PAL-B,D,G,H,I,N,60,NTSC-4.43, SECAM)*1
bit 2 ~ bit 3	VCENA/B 0 ~ VCENA/B 1	Video Color Encode_A/B	R/W	Input signal color encode format setting [VCENA/B 1 : VCENA/B 0] [00] : NTSC [01] : PAL [10] : SECAM [11] : Reserved
bit 4	VLFA/B	Video Line Frequency_A/B	R/W	Input signal line frequency setting [0] : 525 line (NTSC-M,J , NTSC-4.43 , PAL-M,60) [1] : 625 line (PAL-B,D,G,H,I,N , PAL-Nc , SECAM)
bit 5	BWA/B	Black & White_A/B	R/W	Monochrome mode (ON/OFF) setting *2 [0] : Monochrome mode OFF [1] : Monochrome mode ON
bit 6	SETUPA/B	Setup_A/B	R/W	Setup process setting [0] : Process as input signal with no setup [1] : Process as input signal with setup
bit 7	AUTODETA/B	Video Standard Auto Detect_A/B	R/W	Input signal auto detection setting *3 [0]: OFF (auto detection disabled; set manually) [1]: ON (auto detection enabled)

*1 For SECAM input signal, change VSCF[1:0] setting to [11].

*2 DOA register of Sub-address “0x10” and DOB register of Sub-address “0x28” setting takes priority regardless to above BW register setting.

*3 “Auto detection function” must not use when it is being operated on Direct SYNC VLOCK (Sub-Address0x03[7]=1).

NDMODE A Register (R/W) [Sub Address 0x0F] (A block register)
NDMODE B Register (R/W) [Sub Address 0x27] (B block register)
For limiting auto input video signal detection candidates of A block output data.

Sub Address 0x0F, 0x27 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ND625LA ND625LB	ND525LA ND525LB	NDPAL60A NDPAL60B	NDNT443A NDNT443B	Reserved Reserved	NDSECAMA NDSECAMB	NDPALNCA NDPALNCB	NDPALMA NDPALMB
Default Value							
0	0	0	0	0	0	0	0

NDMODE A/B Register Definition

Bit	Register Name		R/W	Definition
bit 0	NDPALMA/B	No Detect PAL-M_A/B	R/W	[0] : PAL-M candidate [1] : PAL-M non-candidate
bit 1	NDPALNCA/B	No Detect PAL-Nc_A/B	R/W	[0] : PAL-Nc candidate [1] : PAL-Nc non-candidate
bit 2	NDSECAMA/B	No Detect SECAM_A/B	R/W	[0] : SECAM candidate [1] : SECAM non-candidate
bit 3	Reserved	Reserved	R/W	Reserved
bit 4	NDNT443A/B	No Detect NTSC-4.43_A/B	R/W	[0] : NTSC-4.43 candidate [1] : NTSC-4.43 non-candidate
bit 5	NDPAL60A/B	No Detect PAL-60_A/B	R/W	[0] : PAL-60 candidate [1] : PAL-60 non-candidate
bit 6	ND525LA/B	No Detect 525Line_A/B	R/W	[0] : 525 line candidate [1] : 525 line non-candidate
bit 7	ND625LA/B	No Detect 625Line_A/B	R/W	[0] : 625 line candidate [1] : 625 line non-candidate

In making the above register settings, the following restrictions are apply,

[1] Setting both NDNT443A/B (bit 4) and NDPAL60A/B (bit 5) to [1] (High) is prohibited.

[2] Setting both ND525LA/B (bit 6) and ND625LA/B (bit 7) to [1] (High) is prohibited.

[3] To limit candidate formats, it is necessary to have the auto detection mode OFF while first setting the register to non-limited signal status and next the NDMODE settings, and then setting the auto detection mode to ON.

Output Pin Control 0 A Register (R/W) [Sub Address 0x10] (A block register)
Output Pin Control 0 B Register (R/W) [Sub Address 0x28] (B block register)

A block output pin output status setting

Sub Address 0x10, 0x28 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	FLA FLB	HDACTLA HDACTLB	NLA NLB	DVALIDLA DVALIDLB	VDACTLA VDACTLB	DOA1 DOB1	DOA0 DOB0
Default Value							
0	0	0	0	0	0	0	0

Output Control 0 A/B Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 1	DOA/B 0 ~ DOA/B 1	Data Output _A/B	R/W	[00]: Normal output [01]: DATA_A/B [7: 0] pin output fixed at Low [10]: Black level output [11]: Blue level output
bit 2	VDACTLA/B	VD/ VACT Low_A/B	R/W	[0] : Normal output [1]: VD_ACT_A/B pin output fixed at low.
bit 3	DVALIDLA/B	DVALID Low_A/B	R/W	[0] : Normal output [1]: DVALID_A/B pin output fixed at low.
bit 4	NLA/B	NSIG Low_A/B	R/W	[0] : Normal output [1] : NSIG_A/B pin output fixed at low
bit 5	HDACTLA/B	HD/HACT Low_A/B	R/W	[0] : Normal output [1]: HD_ACT_A/B pin output fixed at low.
bit 6	FLA/B	FIELD_A/B	R/W	[0] : Normal output [1] : FIELD_A/B pin output fixed at low
bit 7	Reserved	Reserved	R/W	Reserved

Note: Output control via pins OE_A, OE_B, PDN, RSTN and AINSEL[4:0] (Non-decode) takes priority, regardless of the above settings.

Output Pin Control 1 A Register (R/W) [Sub Address 0x11] (A block register)
Output Pin Control 1 B Register (R/W) [Sub Address 0x29] (B block register)

A block output pin status setting register.

Sub Address 0x11, 0x29 Default Value : 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	HDACTSELA HDACTSELB	VDACTSELA VDACTSELB	FIELDA FIELDB	DVALIDA DVALIDB	VDACTA VDACTB	HDACTA HDACTB
Default Value							
0	0	0	0	0	0	0	0

Output Control 1 A/B Register Definition

Bit	Register Name		R/W	Definition
bit 0	HDACTA/B	HD_ACT_A/B Pin Polarity	R/W	HD_ACT_A/B pin output polarity setting. [0] : Active Low [1] : Active High
bit 1	VDACTA/B	VD_ACT_A/B Pin Polarity	R/W	VD_ACT_A/B pin output polarity setting. [0]: Active Low [1]: Active High
bit 2	DVALIDA/B	DVALID_A/B Pin Polarity	R/W	DVALID_A/B pin output polarity setting. [0]: Active Low [1]: Active High
bit 3	FIELDA/B	FIELD_A/B Pin Polarity	R/W	FIELD_A/B pin output polarity setting. [0]: Active Low [1]: Active High
bit 4	VDACTSELA/B	VD/ VACT Select_A/B	R/W	VD_ACT_A/B pin output signal selection : [0] : VD signal is output. [1] : VACT signal is output.
bit 5	HDACTSELA/B	HD/ HACT Select_A/B	R/W	HD_ACT_A/B pin output signal selection : [0] : HD signal is output. [1] : HACT signal is output.
bit 6 ~ bit 7	Reserved	Reserved	R/W	Reserved

Note: Output control via pins OE_A, OE_B, PDN and RSTN takes priority, regardless of the above settings.

AGC & ACC A Control Register (R/W) [Sub Address 0x12] (A block register)
AGC & ACC B Control Register (R/W) [Sub Address 0x2A] (B block register)

AGC and ACC setting register.

Sub Address 0x12, 0x2A Default Value : 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ACCFRZA ACCFRZB	ACCA1 ACCB1	ACCA0 ACCB0	AGCFRZA AGCFRZB	AGCCA1 AGCCB1	AGCCA0 AGCCB0	AGCTA1 AGCTB1	AGCTA0 AGCTB0
Default Value							
0	0	0	0	0	0	0	0

AGC & ACC A/B Control Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 1	AGCTA/B 0 ~ AGCTA/B 1	AGC Time Constant_A/B	R/W	AGC time constant (T) setting* (if disabled, PGA can be set manually) [AGCT1 : AGCT0] [00] : Disable [01] : Fast [T = 1Field] [10] : Middle [T =7Fields] [11] : Slow [T = 29Fields]
bit 2 ~ bit 3	AGCCA/B 0 ~ AGCCA/B 1	AGC Coring Control_A/B	R/W	AGC non-sensing bandwidth (LSB) setting [AGCC1 : AGCC0] [00] : ±2LSB [01] : ±3LSB [10] : ±4LSB [11] : No non-sensing band
bit 4	AGCFRZA/B	AGC Freeze_A/B	R/W	AGC freeze function (ON/OFF) setting (AGC set values are saved during freeze) [0] : Non-frozen [1] : Frozen
bit 5 ~ bit 6	ACCTA/B 0 ~ ACCTA/B 1	ACC Time Constant_A/B	R/W	ACC time constant (T) setting [ACCT1 : ACCT0] [00] : Disable [01] : Fast [T = 2Fields] [10] : Middle [T =8Fields] [11] : Slow [T = 30Fields]
bit 7	ACCFRZA/B	ACC Freeze_A/B	R/W	ACC freeze function (ON/OFF) setting (ACC set values are saved during freeze) [0] : Non-frozen [1] : Frozen

Control 0 A Register (R/W) [Sub Address 0x13] (A block register)
Control 0 B Register (R/W) [Sub Address 0x2B] (B block register)

Sub Address 0x13, 0x2B Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	NSIGMDA1 NSIGMDB1	NSIGMDA0 NSIGMDB0	C443FILA1 C443FILB1	C443FILA0 C443FILB0	C358FILA1 C358FILB1	C358FILA0 C358FILB0	AGCTLA AGCTLB
Default Value							
0	0	0	0	0	0	0	0

Control 0 A/B Register Definition

Bit	Register Name		R/W	Definition
bit 0	AGCTLA/B	AGC Transition Level_A/B	R/W	Transition speed setting, between peak AGC and sync AGC [0] : Quick [1] : Slow
bit 1 ~ bit 2	C358FILA/B 0 ~ C358FILA/B 1	C Filter_358 Select_A/B	R/W	C-filter bandwidth setting, for 3.58 MHz subcarrier system signal [C358FILA/B 1 : C358FILA/B 0] [00] : 3.58 Narrow [01] : 3.58 Medium [10] : 3.58 Wide [11] : Reserved
bit 3 ~ bit 4	C443FILA/B 0 ~ C443FILA/B 1	C Filter_443 Select_A/B	R/W	C-filter bandwidth setting, for 4.43 MHz subcarrier system signal [C443FILA/B 1 : C443FILA/B 0] [00] : 4.43 Narrow [01] : 4.43 Medium [10] : 4.43 Wide [11] : Reserved
bit 5 ~ bit 6	NSIGMDA/B 0 ~ NSIGMDA/B 1	No Signal Output Mode_A/B	R/W	Setting for output on no-signal detection * [NSIGMDA/B 1 : NSIGMDA/B 0] [00] : Black-level output [01] : Blue-level (Blueback) output [10] : Input status (sandstorm) output [11] : Reserved
bit 7	Reserved	Reserved	R/W	Reserved

* DOA/B[1:0] register of Sub-address"0x01/0x28" takes priority regardless to no-signal detection setting adjustment above when the DOA/B[1:0] register value is set other than [00].

Contrast Control A Register (R/W) [Sub Address 0x14] (A block register)
Contrast Control B Register (R/W) [Sub Address 0x2C] (B block register)

Contrast adjustment setting register.

Sub Address 0x14, 0x2C Default Value: 0x80

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CONTA7 CONTB7	CONTA6 CONTB6	CONTA5 CONTB5	CONTA4 CONTB4	CONTA3 CONTB3	CONTA2 CONTB2	CONTA1 CONTB1	CONTA0 CONTB0
Default Value							
1	0	0	0	0	0	0	0

Contrast Control A/B Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 7	CONTA/B 0 ~ CONTA/B 7	Contrast Control_A/B	R/W	Register for contrast adjustment in steps of 1/128 in range 1~255/128 from default value of 0x80

Brightness Control A Register (R/W) [Sub Address 0x15] (A block register)
Brightness Control B Register (R/W) [Sub Address 0x2D] (B block register)

Brightness adjustment setting register

Sub Address 0x15, 0x2D Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BRA7 BRB7	BRA6 BRB6	BRA5 BRB5	BRA4 BRB4	BRA3 BRB3	BRA2 BRB2	BRA1 BRB1	BRA0 BRB0
Default Value							
0	0	0	0	0	0	0	0

Brightness Control A/B Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 7	BRA/B0 ~ BRA/B7	Brightness Control_A/B	R/W	Register for brightness adjustment in steps of 1 by 8-bit code setting in 2's complement

Saturation Control A Register (R/W) [Sub Address 0x16] (A block register)
Saturation Control B Register (R/W) [Sub Address 0x2E] (B block register)

Saturation adjustment setting register

Sub Address 0x16, 0x2E Default Value: 0x80

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SATA7 SATB7	SATA6 SATB6	SATA5 SATB5	SATA4 SATB4	SATA3 SATB3	SATA2 SATB2	SATA1 SATB1	SATA0 SATB0
Default Value							
1	0	0	0	0	0	0	0

Saturation Control A/B Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 7	SATA/B0 ~ SATA/B7	Saturation Control_A/B	R/W	Register for saturation level adjustment in steps of 1/128 in range 1~255/128 from default value of 0x80 (CVBS or S-video input)

HUE Control A Register (R/W) [Sub Address 0x17] (A block register)
HUE Control B Register (R/W) [Sub Address 0x2F] (B block register)

HUE adjustment setting register.

Sub Address 0x17, 0x2F Default Value : 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HUEA7 HUEB7	HUEA6 HUEB6	HUEA5 HUEB5	HUEA4 HUEB4	HUEA3 HUEB3	HUEA2 HUEB2	HUEA1 HUEB1	HUEA0 HUEB0
Default Value							
0	0	0	0	0	0	0	0

HUE Control A/B Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 7	HUEA/B0 ~ HUEA/B7	HUE Control_A/B	R/W	Register for hue adjustment in steps of 1/256 in range ±45° in 2's complement

Request VBI Infomation A Register (R/W) [Sub Address 0x18] (A block register)
Request VBI Infomation B Register (R/W) [Sub Address 0x30] (B block register)

Data decode request during VBI interval setting register.

Sub Address 0x18, 0x30 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	WSSRQA WSSRQB	VBIDRQA VBIDRQB	EXTRQA EXTRQB	CCRQA CCRQB
Default Value							
0	0	0	0	0	0	0	0

Request VBI Infomation A/B Register Definition

Bit	Register Name		R/W	Definition
bit 0	CCRQA/B	Closed Caption Decode Request_A/B	R/W	Setting (ON/OFF) for closed caption decode request [0] : No request (OFF) [1] : Request (ON)
bit 1	EXTRQA/B	Extended Data Decode Request_A/B	R/W	Setting (ON/OFF) for Extended Data decode request [0] : No request (OFF) [1] : Request (ON)
bit 2	VBIDRQA/B	VBID Decode Request_A/B	R/W	Setting (ON/OFF) for VBID decode request [0] : No request (OFF) [1] : Request (ON)
bit 3	WSSRQA/B	WSS Decode Request_A/B	R/W	Setting (ON/OFF) for WSS decode request [0] : No request (OFF) [1] : Request (ON)
bit 4 ~ bit 7	Reserved	Reserved	R/W	Reserved

Status 1 A Register (R) [Sub Address 0x19] (A block register)
Status 1 B Register (R) [Sub Address 0x31] (B block register)

Sub Address 0x19, 0x31

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OVCOLA OVCOLB	PKWHITEA PKWHITEB	Reserved Reserved	CPLLA CPLLB	COLKILONA COLKILONB	FRMSTDA FRMSTDB	VLOCKA VLOCKB	NOSIGA NOSIGB

Status 1 A/B Register Definition

Bit	Register Name		R/W	Definition
bit 0	NOSIGA/B	No Signal_A/B	R	Input signal indicator [0] : Input signal present [1] : Input signal absent
bit 1	VLOCKA/B	Video Locked_A/B	R	Input signal VLOCK synchronization status indicator [0]: Input signal synchronized [1]: Input signal non-synchronized
bit 2	FRMSTDA/B	Frame Standard_A/B	R	Input signal interlace status indicator [0]: Input signal 525/625 interlaced [1]: Input signal not 525/625 interlaced
bit 3	COLKILONA/B	Color Killer_A/B	R	Color killer status indicator *1 [0]: Color killer not operation [1]: Color killer operation
bit 4	CPLLA/B	Color PLL Lock_A/B		PLL clock locked status indicator [0]: No locked [1]: Locked
bit 5	Reserved	Reserved	R	Reserved
bit 6	PKWHITEA/B	Peak White Detection_A/B	R	Luminance decode result flow status indicator,after passage through AGC block [0]: Normal [1]: Overflow
bit 7	OVCOLA/B	Over Color Level_A/B	R	Color decode result flow status indicator, after passage through ACC block*2 [0]: Normal [1]: Overflow (excessive color signal input)

Status 2 A Register (R) [Sub Address 0x1A] (A block register)
Status 2 B Register (R) [Sub Address 0x32] (B block register)

Sub Address 0x1A, 0x32

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	AGCSTSA AGCSTSB	REALFLDA REALFLDB	WSSDETA WSSDETB	VBIDDETA VBIDDETB	EXTDETA EXTDETB	CCDETA CCDETB

Status 2 A/B Register Definition

Bit	Register Name		R/W	Definition
bit 0	CCDETA/B	Closed Caption Detect_A/B	R	Indicator for presence of decoded data in Closed Caption 1 2 Register [0]: No closed caption data present [1]: Closed caption Data present
bit 1	EXTDETA/B	Extended Data Detect_A/B	R	Indicator for presence of decoded data in Extended Data 1,2 Register 0]: No extended data present [1]: Extended data present
bit 2	VBIDDETA/B	VBID Data Detect_A/B	R	Indicator for presence of decoded data in VBID 1,2 Register [0]: No VBID data present [1]: VBID data present
bit 3	WSSDETA/B	WSS Data Detect_A/B	R	Indicator for presence of decoded data in WSS 1,2 Register [0]: No WSS data present [1]: WSS data present
bit 4	REALFLDA/B	Real Field_A/B	R	Input signal field status (even/odd) indicator [0] : EVEN field [1] : ODD field
bit 5	AGCSTSA/B	AGC Status_A/B	R	[0] : Sync AGC active [1] : Peak AGC active *
bit 6 ~ bit 7	Reserved	Reserved	R	Reserved

Input Video Status A Register (R) [Sub Address 0x1C] (A block register)
Input Video Status B Register (R) [Sub Address 0x34] (B block register)

Sub Address 0x1C, 0x34

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FIXEDA	UNDEFA	ST_B/WA	ST_VLFA	ST_VCENA1	ST_VCENA0	ST_VSFA1	ST_VSFA0
FIXEDB	UNDEFB	ST_B/WB	ST_VLFB	ST_VCENB1	ST_VCENB0	ST_VSFB1	ST_VSFB0

Input Video Status A/B Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	ST_VSFA/B 0 ~ ST_VSFA/B 1	Status of Video Sub-Carrier Frequency_A/B	R	Input video signal subcarrier frequency indicator [ST_VSFA/B 1 : ST_VSFA/B 0] (MHz) [00] : 3.57954545 (NTSC-M,J) [01] : 3.57561149 (PAL-M) [10] : 3.58205625 (PAL-Nc) [11] : 4.43361875 (PAL-B,D,G,H,I,N,60, NTSC-4.43, SECAM*)
bit 2 ~ bit 3	ST_VCENA/B 0 ~ ST_VCENA/B 1	Status of Video Color Encode_A/B	R	Input signal color encode format indicator [ST_VCEN1 : ST_VCEN0] [00] : NTSC [01] : PAL [10] : SECAM [11] : Reserved
bit 4	ST_VLFA/B	Status of Video Line Frequency_A/B	R	Input signal line number indicator [0] : 525 line (NTSC-M,J , NTSC-4.43 , PAL-M,60) [1] : 625 line (PAL-B,D,G,H,I,N,Nc, SECAM)
bit 5	ST_BWA/B	Status of B/W Signal_A/B	R	Input signal monochrome indicator [0]: Not monochrome [1]: Monochrome
bit 6	UNDEFA/B	Un_define_A/B	R	Input signal detection indicator [0]: Input signal detected [1]: Input signal not detected
bit 7	FIXEDA/B	Input Video Standard fixed_A/B	R	Input signal detection process status [0]: Detection process in progress [1]: Detection process completed

*If SECAM input signal is detected, ST_VSCF[1:0] goes to [11].

Closed Caption 1 A Register (R) [Sub Address 0x1D] (A block register)
Closed Caption 1 B Register (R) [Sub Address 0x35] (B block register)

Closed Caption data storage register

Sub Address 0x1D, 0x35

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CCA7 CCB7	CCA6 CCB6	CCA5 CCB5	CCA4 CCB4	CCA3 CCB3	CCA2 CCB2	CCA1 CCB1	CCA0 CCB0

Closed Caption 2 A Register (R) [Sub Address 0x1E] (A block register)
Closed Caption 2 B Register (R) [Sub Address 0x36] (B block register)

Closed Caption data storage register

Sub Address 0x1E, 0x36

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CCA15 CCB15	CCA14 CCB14	CCA13 CCB13	CCA12 CCB12	CCA11 CCB11	CCA10 CCB10	CCA CCB	CCA8 CCB8

WSS 1 A Register (R) [Sub Address 0x1F] (A block register)
WSS 1 B Register (R) [Sub Address 0x37] (B block register)

WSS data storage register
Sub Address 0x1F, 0x37

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
GA2-7	GA2-6	GA2-5	GA2-4	GA1-3	GA1-2	GA1-1	GA1-0
GB2-7	GB2-6	GB2-5	GB2-4	GB1-3	GB1-2	GB1-1	GB1-0

WSS 2 A Register (R) [Sub Address 0x20] (A block register)
WSS 2 B Register (R) [Sub Address 0x38] (B block register)

WSS data storage register
Sub Address 0x20, 0x38

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	GA4-13 GB4-13	GA4-12 GB4-12	GA4-11 GB4-11	GA3-10 GB3-10	GA3-9 GB3-9	GA3-8 GB3-8

Extended Data 1 A Register (R) [Sub Address 0x21] (A block register)
Extended Data 1 B Register (R) [Sub Address 0x39] (B block register)

Closed Caption Extended data storage register
Sub Address 0x21, 0x39

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXTA7 EXTB7	EXTA6 EXTB6	EXTA5 EXTB5	EXTA4 EXTB4	EXTA3 EXTB3	EXTA2 EXTB2	EXTA1 EXTB1	EXTA0 EXTB0

Extended Data 2 A Register (R) [Sub Address 0x22] (A block register)
Extended Data 2 B Register (R) [Sub Address 0x3A] (B block register)

Closed Caption Extended data storage register
Sub Address 0x22, 0x3A

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXTA15 EXTB15	EXTA14 EXTB14	EXTA13 EXTB13	EXTA12 EXTB12	EXTA11 EXTB11	EXTA10 EXTB10	EXTA9 EXTB9	EXTA8 EXTB8

VBID 1 A Register (R) [Sub Address 0x23] (A block register)
VBID 1 B Register (R) [Sub Address 0x3B] (B block register)

VBID data storage register
Sub Address 0x23, 0x3B

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	VBIDA1 VBIDB1	VBIDA2 VBIDB2	VBIDA3 VBIDB3	VBIDA4 VBIDB4	VBIDA5 VBIDB5	VBIDA6 VBIDB6

VBID 2 A Register (R) [Sub Address 0x24] (A block register)
VBID 2 B Register (R) [Sub Address 0x3C] (B block register)

VBID data storage register
Sub Address 0x24, 0x3C

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBIDA7 VBIDB7	VBIDA8 VBIDB8	VBIDA9 VBIDB9	VBIDA10 VBIDB10	VBIDA11 VBIDB11	VBIDA12 VBIDB12	VBIDA13 VBIDB13	VBIDA14 VBIDB14

Device and Revision ID Register (R) [Sub Address 0x3D]

Device ID and Revision indicator

Device ID: [0x39]

Revision ID: Initially 0x00; revision number changes only when control software should be modified.

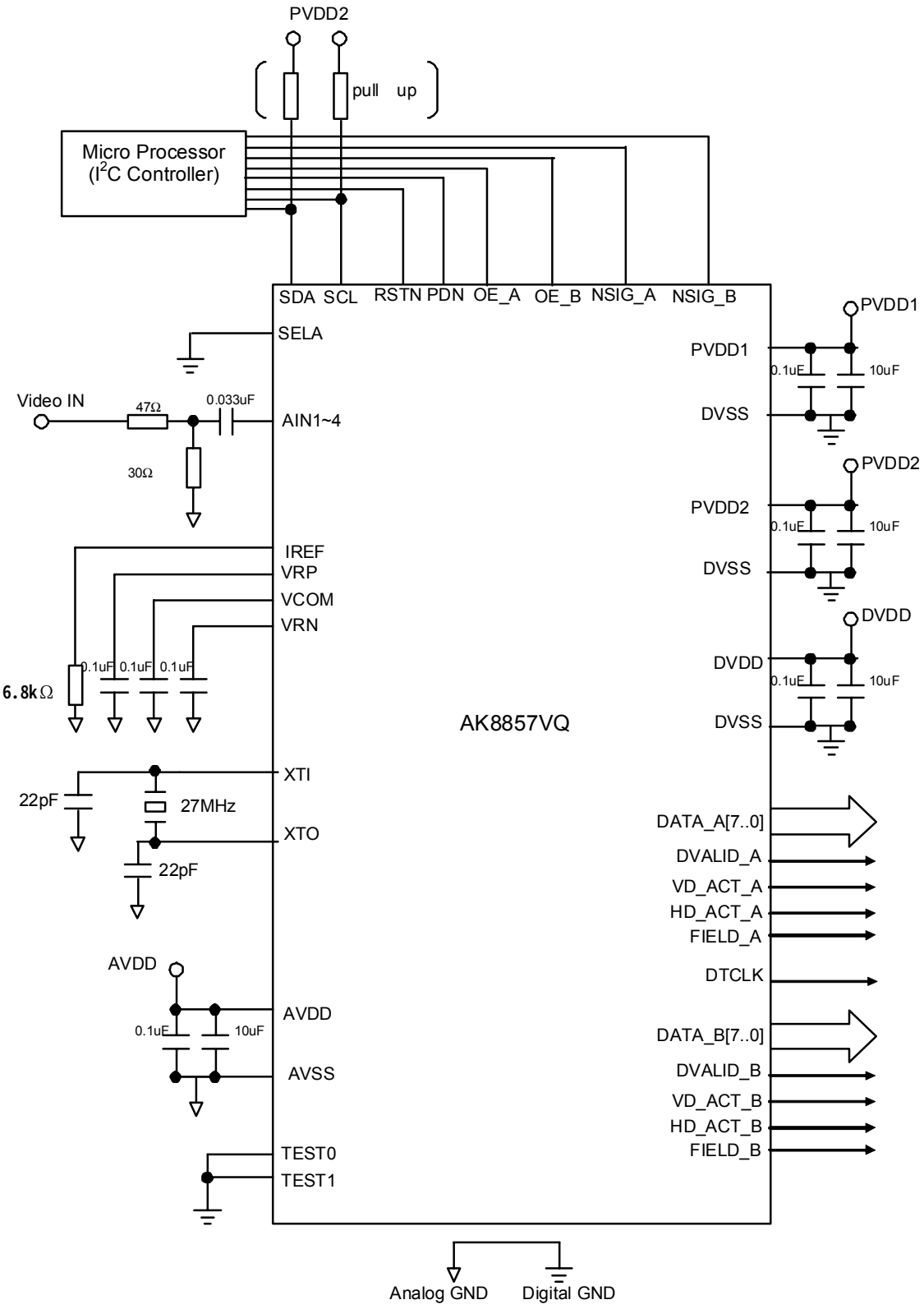
Sub Address 0x3D

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
REV1	REV0	DID5	DID4	DID3	DID2	DID1	DID0
Default Value							
0	0	1	1	1	0	0	1

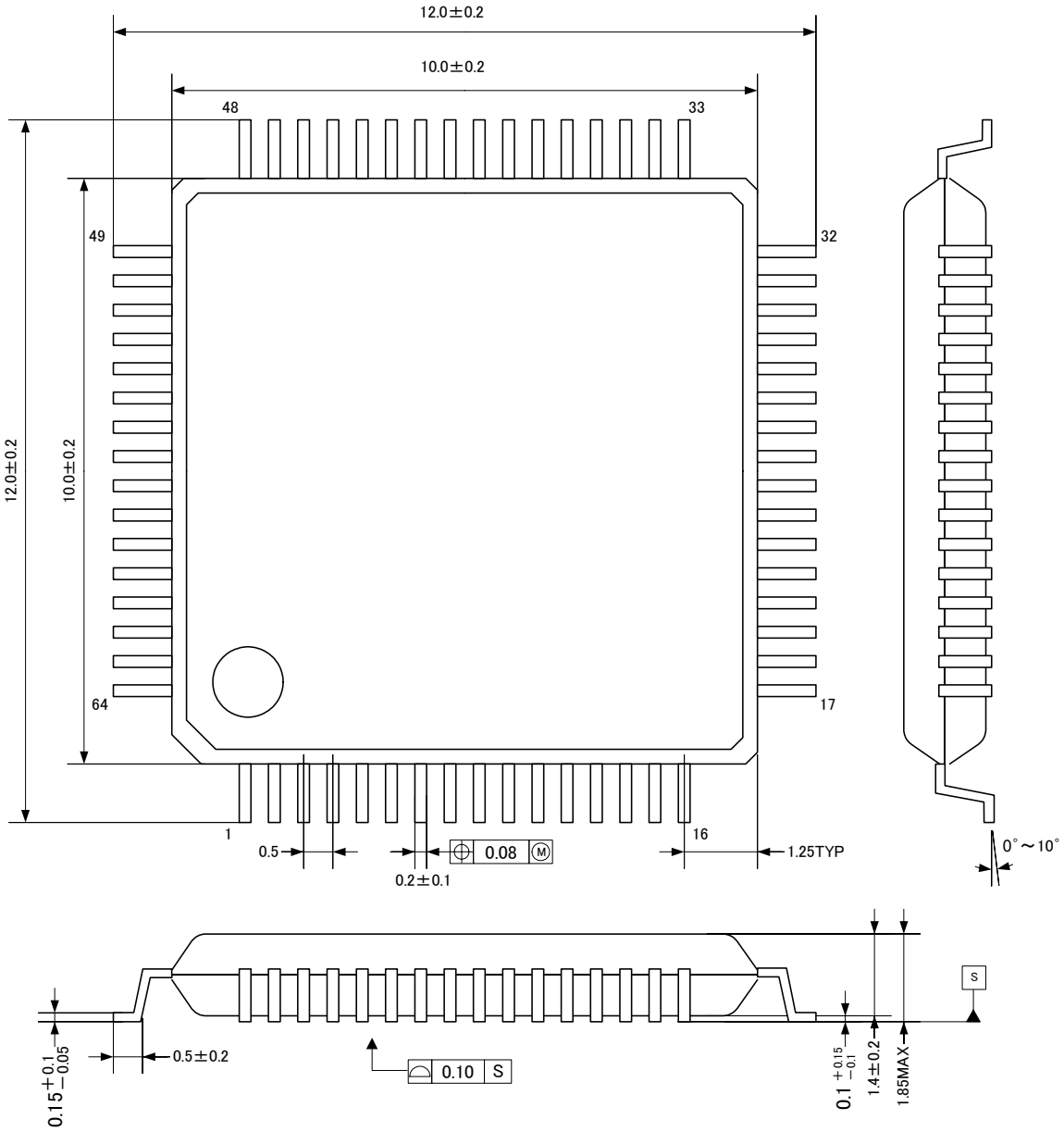
Device and Revision ID Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 5	DID0 ~ DID5	Device ID	R	Device ID indicator (0x39)
bit 6 ~ bit 7	REV0 ~ REV1	Revision ID	R	Revision ID indicator (initially 0x00)

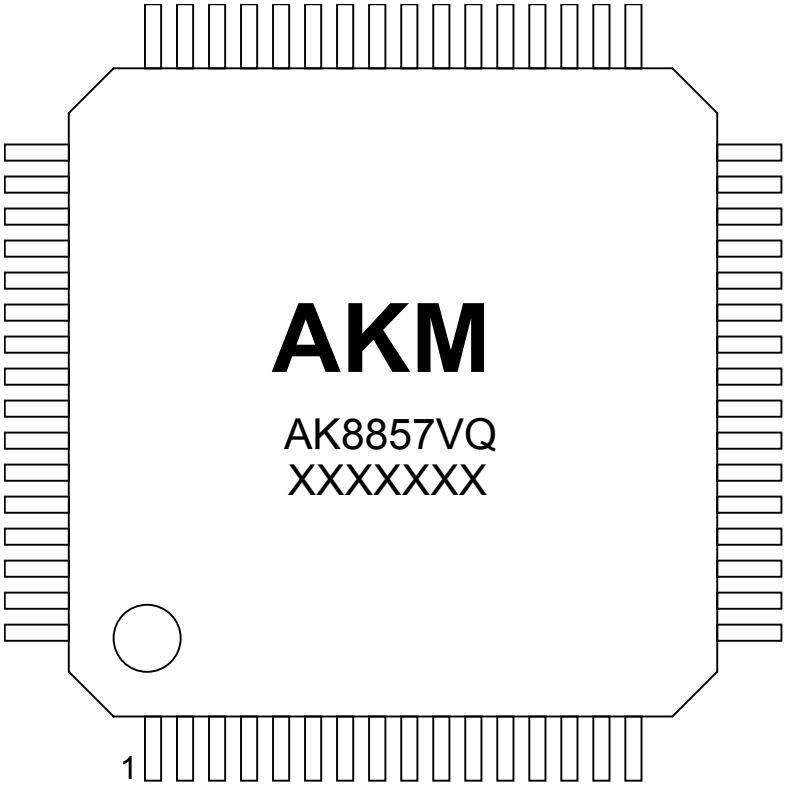
10. System connection example



11. Package


12.0±0.2
10.0±0.2
48
33
49
32
64
17
1
16
12.0±0.2
10.0±0.2
0.5
0.08 M
0.2±0.1
1.25TYP
0°～10°
S
0.5±0.2
0.10 S
0.15 +0.1 −0.05
0.1 +0.15 −0.1
1.4±0.2
1.85MAX

12. Marking



AKM: AKM Logo
AK8857VQ: Marketing Code
XXXXXXX (7 digits): Date Code

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