

MC74HC14A

Hex Schmitt-Trigger Inverter

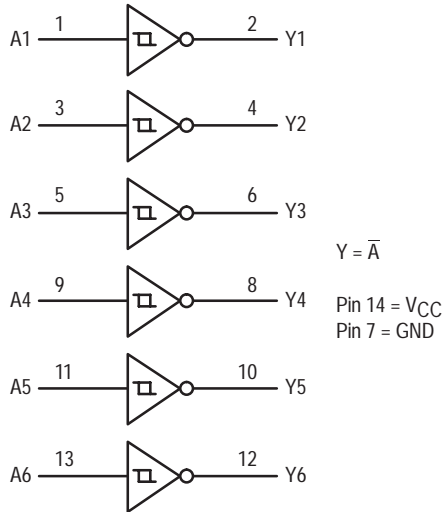
High-Performance Silicon-Gate CMOS

The MC74HC14A is identical in pinout to the LS14, LS04 and the HC04. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

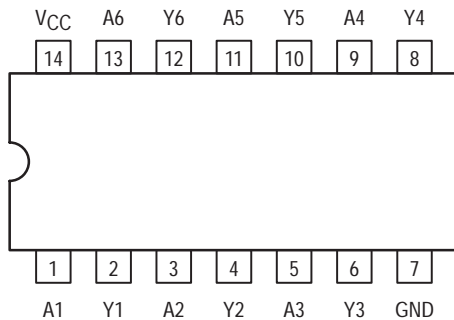
The HC14A is useful to “square up” slow input rise and fall times. Due to hysteresis voltage of the Schmitt trigger, the HC14A finds applications in noisy environments.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2 to 6V
- Low Input Current: 1µA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 60 FETs or 15 Equivalent Gates

LOGIC DIAGRAM



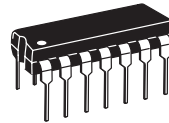
Pinout: 14-Lead Packages (Top View)



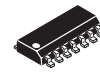
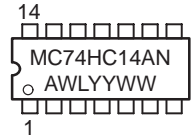
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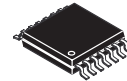
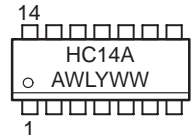
MARKING DIAGRAMS



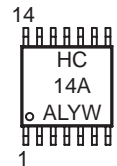
PDIP-14
N SUFFIX
CASE 646



SOIC-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

FUNCTION TABLE

| Inputs | Outputs |
|--------|---------|
| A | Y |
| L | H |
| H | L |

ORDERING INFORMATION

| Device | Package | Shipping |
|---------------|----------|-------------|
| MC74HC14AN | PDIP-14 | 2000 / Box |
| MC74HC14AD | SOIC-14 | 55 / Rail |
| MC74HC14ADR2 | SOIC-14 | 2500 / Reel |
| MC74HC14ADT | TSSOP-14 | 96 / Rail |
| MC74HC14ADTR2 | TSSOP-14 | 2500 / Reel |

MC74HC14A

MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|------------------|---|--------------------------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | - 0.5 to + 7.0 | V |
| V _{in} | DC Input Voltage (Referenced to GND) | - 0.5 to V _{CC} + 0.5 | V |
| V _{out} | DC Output Voltage (Referenced to GND) | - 0.5 to V _{CC} + 0.5 | V |
| I _{in} | DC Input Current, per Pin | ± 20 | mA |
| I _{out} | DC Output Current, per Pin | ± 25 | mA |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | ± 50 | mA |
| P _D | Power Dissipation in Still Air, Plastic DIP† | 750 | mW |
| | SOIC Package† | 500 | |
| | TSSOP Package† | 450 | |
| T _{stg} | Storage Temperature Range | - 65 to + 150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package | 260 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125° C
SOIC Package: - 7 mW/°C from 65° to 125° C
TSSOP Package: - 6.1 mW/°C from 65° to 125° C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit | |
|------------------------------------|--|-------------------------|-----------------|-----------|----|
| V _{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V | |
| V _{in} , V _{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V _{CC} | V | |
| T _A | Operating Temperature Range, All Package Types | - 55 | + 125 | °C | |
| t _r , t _f | Input Rise/Fall Time (Figure 1) | V _{CC} = 2.0 V | 0 | No Limit* | ns |
| | | V _{CC} = 4.5 V | 0 | No Limit* | |
| | | V _{CC} = 6.0 V | 0 | No Limit* | |

*When V_{in} = 50% V_{CC}, I_{CC} > 1mA

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DC CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Condition | V _{CC} V | Guaranteed Limit | | | Unit |
|------------------------------|---|---|--|------------------|-------|--------|------|
| | | | | -55 to 25°C | ≤85°C | ≤125°C | |
| V _{T+} max | Maximum Positive-Going Input Threshold Voltage (Figure 3) | V _{out} = 0.1V I _{out} ≤ 20μA | 2.0 | 1.50 | 1.50 | 1.50 | V |
| | | | 3.0 | 2.15 | 2.15 | 2.15 | |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.20 | 4.20 | 4.20 | |
| V _{T+} min | Minimum Positive-Going Input Threshold Voltage (Figure 3) | V _{out} = 0.1V I _{out} ≤ 20μA | 2.0 | 1.0 | 0.95 | 0.95 | V |
| | | | 3.0 | 1.5 | 1.45 | 1.45 | |
| | | | 4.5 | 2.3 | 2.25 | 2.25 | |
| | | | 6.0 | 3.0 | 2.95 | 2.95 | |
| V _{T-} max | Maximum Negative-Going Input Threshold Voltage (Figure 3) | V _{out} = V _{CC} - 0.1V I _{out} ≤ 20μA | 2.0 | 0.9 | 0.95 | 0.95 | V |
| | | | 3.0 | 1.4 | 1.45 | 1.45 | |
| | | | 4.5 | 2.0 | 2.05 | 2.05 | |
| | | | 6.0 | 2.6 | 2.65 | 2.65 | |
| V _{T-} min | Minimum Negative-Going Input Threshold Voltage (Figure 3) | V _{out} = V _{CC} - 0.1V I _{out} ≤ 20μA | 2.0 | 0.3 | 0.3 | 0.3 | V |
| | | | 3.0 | 0.5 | 0.5 | 0.5 | |
| | | | 4.5 | 0.9 | 0.9 | 0.9 | |
| | | | 6.0 | 1.2 | 1.2 | 1.2 | |
| V _H max Note 2 | Maximum Hysteresis Voltage (Figure 3) | V _{out} = 0.1V or V _{CC} - 0.1V I _{out} ≤ 20μA | 2.0 | 1.20 | 1.20 | 1.20 | V |
| | | | 3.0 | 1.65 | 1.65 | 1.65 | |
| | | | 4.5 | 2.25 | 2.25 | 2.25 | |
| | | | 6.0 | 3.00 | 3.00 | 3.00 | |
| V _H min Note 2 | Minimum Hysteresis Voltage (Figure 3) | V _{out} = 0.1V or V _{CC} - 0.1V I _{out} ≤ 20μA | 2.0 | 0.20 | 0.20 | 0.20 | V |
| | | | 3.0 | 0.25 | 0.25 | 0.25 | |
| | | | 4.5 | 0.40 | 0.40 | 0.40 | |
| | | | 6.0 | 0.50 | 0.50 | 0.50 | |
| V _{OH} | Minimum High-Level Output Voltage | V _{in} ≤ V _{T-} min I _{out} ≤ 20μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | | V _{in} ≤ V _{T-} min I _{out} ≤ 2.4mA | 3.0 | 2.48 | 2.34 | |
| I _{out} ≤ 4.0mA | 4.5 | 3.98 | 3.84 | 3.70 | | | |
| I _{out} ≤ 5.2mA | 6.0 | 5.48 | 5.34 | 5.20 | | | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{in} ≥ V _{T+} max I _{out} ≤ 20μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | | V _{in} ≥ V _{T+} max I _{out} ≤ 2.4mA | 3.0 | 0.26 | 0.33 | |
| I _{out} ≤ 4.0mA | 4.5 | 0.26 | 0.33 | 0.40 | | | |
| I _{out} ≤ 5.2mA | 6.0 | 0.26 | 0.33 | 0.40 | | | |
| I _{in} | Maximum Input Leakage Current | V _{in} = V _{CC} or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND I _{out} = 0μA | 6.0 | 1.0 | 10 | 40 | μA |

1. Information on typical parametric values along with frequency or heavy load considerations can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

2. V_Hmin > (V_{T+} min) - (V_{T-} max); V_Hmax = (V_{T+} max) - (V_{T-} min).

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AC CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

| Symbol | Parameter | VCC V | Guaranteed Limit | | | Unit |
|--|--|----------|------------------|-------|--------|------|
| | | | -55 to 25°C | ≤85°C | ≤125°C | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2) | 2.0 | 75 | 95 | 110 | ns |
| | | 3.0 | 30 | 40 | 55 | |
| | | 4.5 | 15 | 19 | 22 | |
| | | 6.0 | 13 | 16 | 19 | |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figures 1 and 2) | 2.0 | 75 | 95 | 110 | ns |
| | | 3.0 | 27 | 32 | 36 | |
| | | 4.5 | 15 | 19 | 22 | |
| | | 6.0 | 13 | 16 | 19 | |
| C _{in} | Maximum Input Capacitance | | 10 | 10 | 10 | pF |

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

| C _{PD} | Power Dissipation Capacitance (Per Inverter)* | Typical @ 25°C, VCC = 5.0 V | | pF |
|-----------------|---|-----------------------------|--|----|
| | | 22 | | |
| | | | | |

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

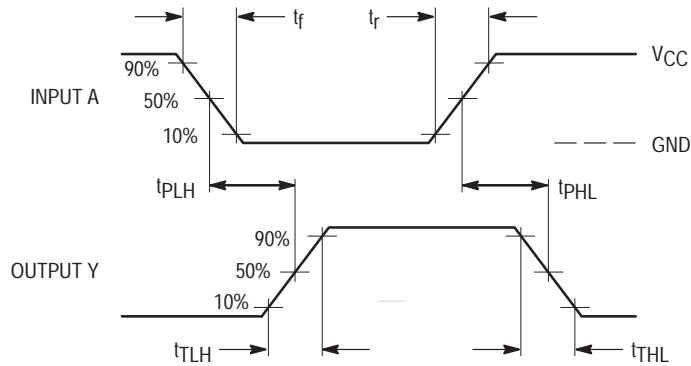
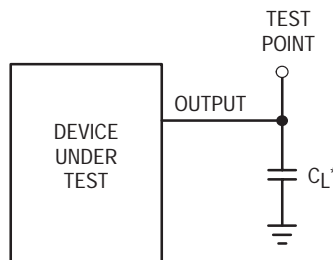


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

MC74HC14A

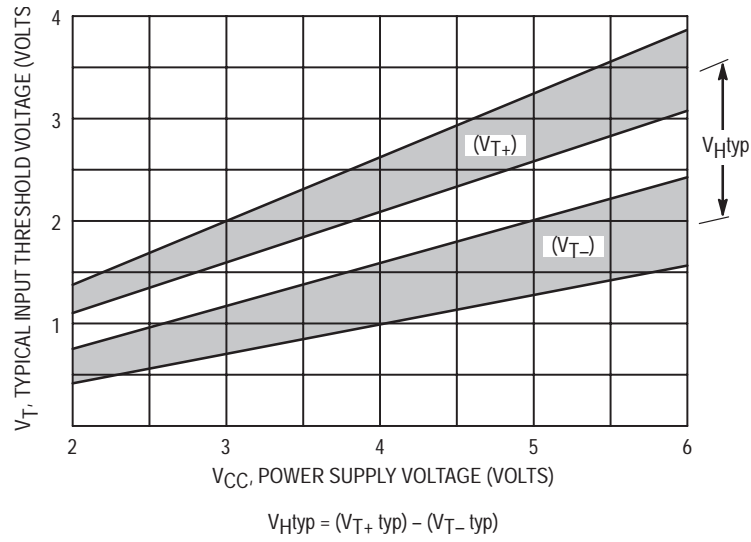
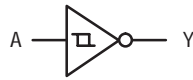
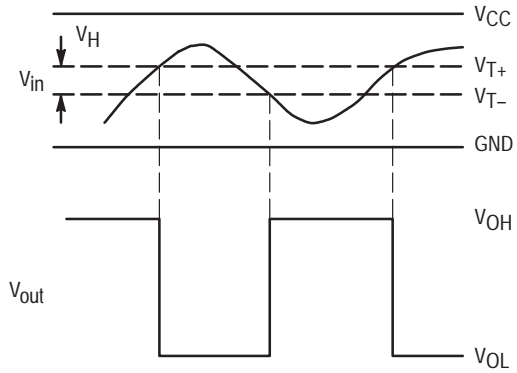


Figure 3. Typical Input Threshold, V_{T+} , V_{T-} versus Power Supply Voltage



(a) A Schmitt-Trigger Squares Up Inputs With Slow Rise and Fall Times



(b) A Schmitt-Trigger Offers Maximum Noise Immunity

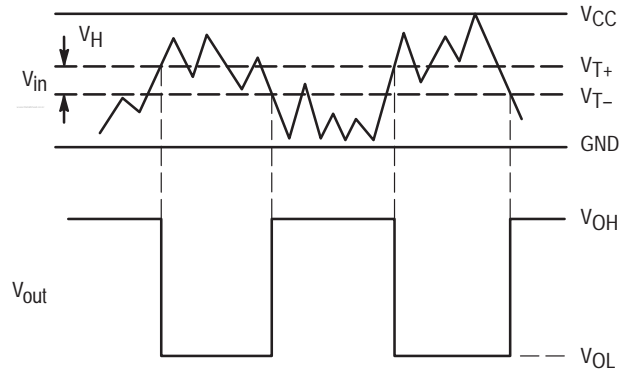
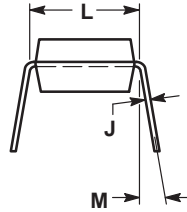
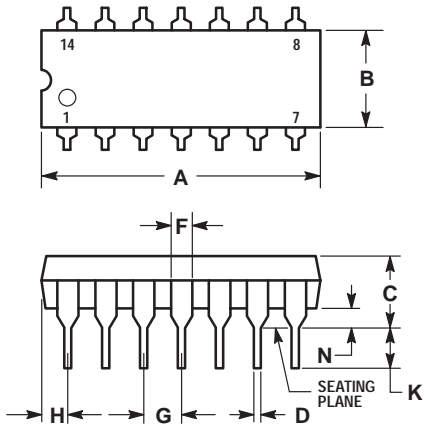


Figure 4. Typical Schmitt-Trigger Applications

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PACKAGE DIMENSIONS

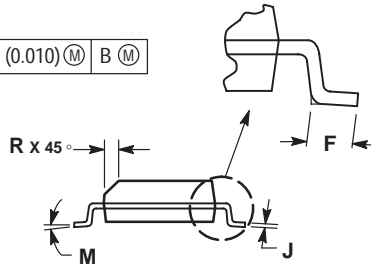
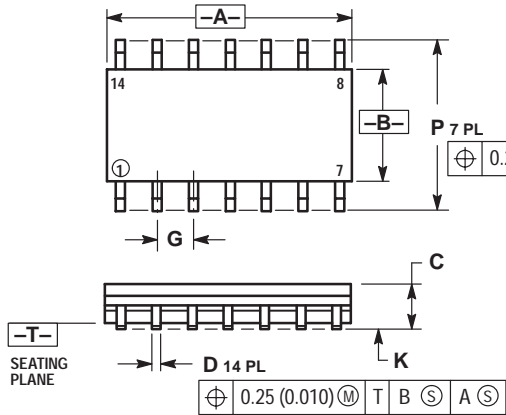
**PDIP-14
N SUFFIX
CASE 646-06
ISSUE L**



- NOTES:
- LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 - DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 - DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 - ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.715 | 0.770 | 18.16 | 19.56 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.145 | 0.185 | 3.69 | 4.69 |
| D | 0.015 | 0.021 | 0.38 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.78 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.052 | 0.095 | 1.32 | 2.41 |
| J | 0.008 | 0.015 | 0.20 | 0.38 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 10° | 0° | 10° |
| N | 0.015 | 0.039 | 0.39 | 1.01 |

**SOIC-14
D SUFFIX
CASE 751A-03
ISSUE F**



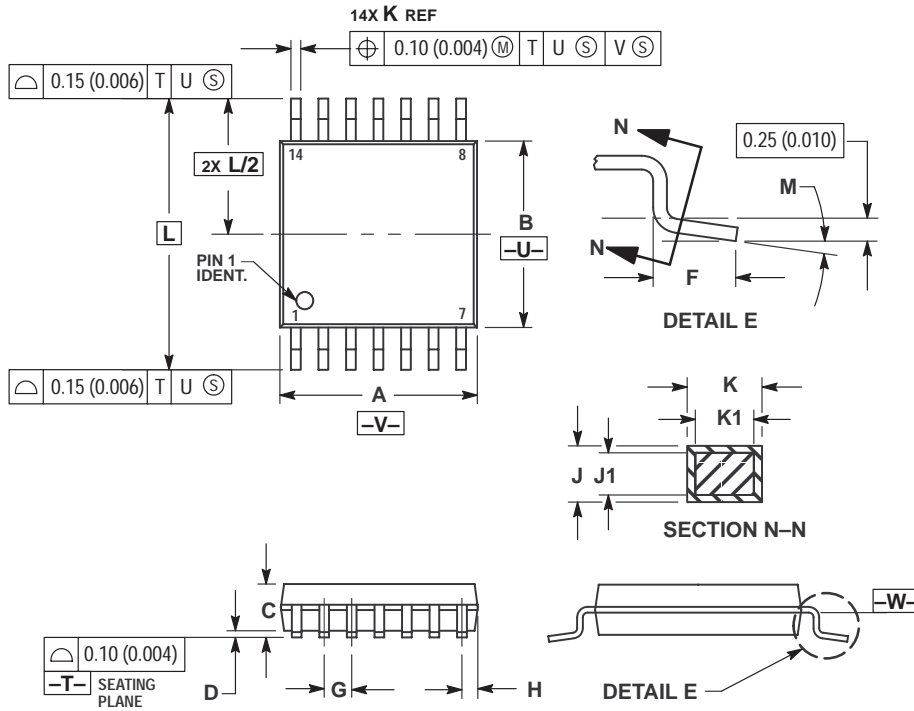
- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: MILLIMETER.
 - DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 - MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 - DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.228 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

MC74HC14A

PACKAGE DIMENSIONS

TSSOP-14
DT SUFFIX
CASE 948G-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -V-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

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