MC33201, MC33202, MC33204, NCV33202, NCV33204

Low Voltage, Rail-to-Rail Operational Amplifiers

The MC33201/2/4 family of operational amplifiers provide rail−to−rail operation on both the input and output. The inputs can be driven as high as 200 mV beyond the supply rails without phase reversal on the outputs, and the output can swing within 50 mV of each rail. This rail−to−rail operation enables the user to make full use of the supply voltage range available. It is designed to work at very low supply voltages (± 0.9 V) yet can operate with a supply of up to +12 V and ground. Output current boosting techniques provide a high output current capability while keeping the drain current of the amplifier to a minimum. Also, the combination of low noise and distortion with a high slew rate and drive capability make this an ideal amplifier for audio applications.

- Low Voltage, Single Supply Operation (+1.8 V and Ground to +12 V and Ground)
- Input Voltage Range Includes both Supply Rails
- Output Voltage Swings within 50 mV of both Rails
- No Phase Reversal on the Output for Over−driven Input Signals
- High Output Current (I_{SC} = 80 mA, Typ)
- Low Supply Current (I_D = 0.9 mA, Typ)
- 600 Ω Output Drive Capability
- Extended Operating Temperature Ranges (−40° to +105°C and −55° to +125°C)
- Typical Gain Bandwidth Product = 2.2 MHz
- Pb−Free Packages are Available

ON Semiconductor®

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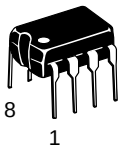
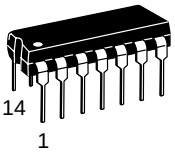


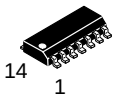
PDIP−8
P, VP SUFFIX
CASE 626

SOIC−8
D, VD SUFFIX
CASE 751

Micro8™
DM SUFFIX
CASE 846A



PDIP−14
P, VP SUFFIX
CASE 646



SOIC−14
D, VD SUFFIX
CASE 751A

TSSOP−14
DTB SUFFIX
CASE 948G

ORDERING INFORMATION

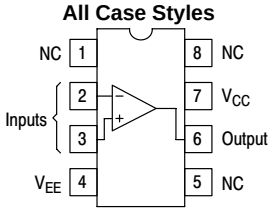
See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 11 of this data sheet.

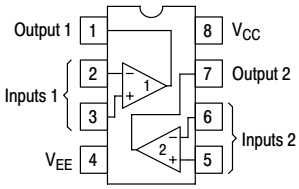
PIN CONNECTIONS

MC33201
All Case Styles



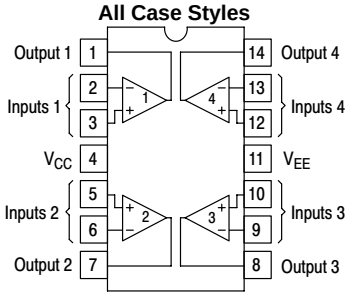
(Top View)

MC33202
All Case Styles

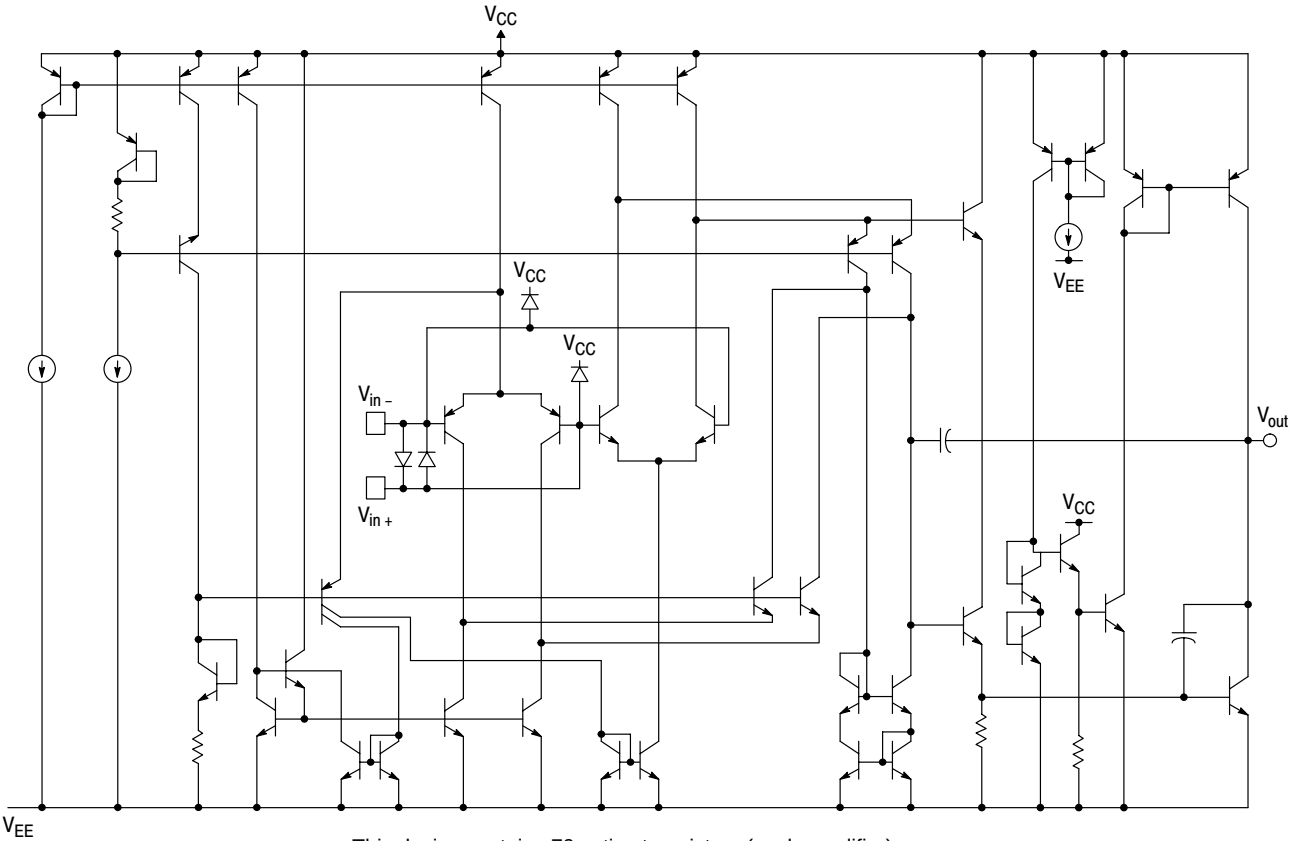


(Top View)

MC33204
All Case Styles



(Top View)



This device contains 70 active transistors (each amplifier).

Figure 1. Circuit Schematic
(Each Amplifier)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+13	V
Input Differential Voltage Range	V_{IDR}	Note 1	V
Common Mode Input Voltage Range (Note 2)	V_{CM}	V_{CC} + 0.5 V to V_{EE} − 0.5 V	V
Output Short Circuit Duration	t_s	Note 3	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	− 65 to +150	°C
Maximum Power Dissipation	P_D	Note 3	mW

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	V_{CC} = 2.0 V	V_{CC} = 3.3 V	V_{CC} = 5.0 V	Unit
Input Offset Voltage $V_{IO\ (max)}$ MC33201 MC33202, NCV33202 MC33204	 ± 8.0 ±10 ±12	 ± 8.0 ±10 ±12	 ± 6.0 ± 8.0 ±10	mV
Output Voltage Swing V_{OH} (R_L = 10 kΩ) V_{OL} (R_L = 10 kΩ)	 1.9 0.10	 3.15 0.15	 4.85 0.15	 V_{min} V_{max}
Power Supply Current per Amplifier (I_D)	 1.125	 1.125	 1.125	mA

Specifications at V_{CC} = 3.3 V are guaranteed by the 2.0 V and 5.0 V tests. V_{EE} = GND.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = + 5.0 V, V_{EE} = Ground, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{CM} 0 V to 0.5 V, V_{CM} 1.0 V to 5.0 V)	3	$\lvert V_{IO} \rvert$				mV
MC33201: T_A = + 25°C			−	−	6.0	
MC33201: T_A = − 40° to +105°C			−	−	9.0	
MC33201V: T_A = − 55° to +125°C			−	−	13	
MC33202: T_A = + 25°C			−	−	8.0	
MC33202: T_A = − 40° to +105°C			−	−	11	
MC33202V: T_A = − 55° to +125°C			−	−	14	
NCV33202V: T_A = − 55° to +125°C (Note 4)			−	−	14	
MC33204: T_A = + 25°C			−	−	10	
MC33204: T_A = − 40° to +105°C			−	−	13	
MC33204V: T_A = − 55° to +125°C			−		17	
Input Offset Voltage Temperature Coefficient (R_S = 50 Ω)	4	$\Delta V_{IO}/\Delta T$				μV/°C
T_A = − 40° to +105°C			−	2.0	−	
T_A = − 55° to +125°C			−	2.0	−	
Input Bias Current (V_{CM} = 0 V to 0.5 V, V_{CM} = 1.0 V to 5.0 V)	5, 6	$\lvert I_{IB} \rvert$				nA
T_A = + 25°C			−	80	200	
T_A = − 40° to +105°C			−	100	250	
T_A = − 55° to +125°C			−	−	500	
Input Offset Current (V_{CM} = 0 V to 0.5 V, V_{CM} = 1.0 V to 5.0 V)	−	$\lvert I_{IO} \rvert$				nA
T_A = + 25°C			−	5.0	50	
T_A = − 40° to +105°C			−	10	100	
T_A = − 55° to +125°C			−	−	200	
Common Mode Input Voltage Range	−	V_{ICR}	V_{EE}	−	V_{CC}	V

1. The differential input voltage of each amplifier is limited by two internal parallel back−to−back diodes. For additional differential input voltage range, use current limiting resistors in series with the input pins.
2. The input common mode voltage range is limited by internal diodes connected from the inputs to both supply rails. Therefore, the voltage on either input must not exceed either supply rail by more than 500 mV.
3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See Figure 2)
4. *NCV33202 and NCV33204 are qualified for automotive use.*

DC ELECTRICAL CHARACTERISTICS (cont.) (V_{CC} = + 5.0 V, V_{EE} = Ground, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Large Signal Voltage Gain (V_{CC} = + 5.0 V, V_{EE} = − 5.0 V) R_L = 10 kΩ R_L = 600 Ω	7	A_{VOL}	 50 25	 300 250	 − −	kV/V
Output Voltage Swing (V_{ID} = ± 0.2 V) R_L = 10 kΩ R_L = 10 kΩ R_L = 600 Ω R_L = 600 Ω	8, 9, 10	 V_{OH} V_{OL} V_{OH} V_{OL}	 4.85 − 4.75 −	 4.95 0.05 4.85 0.15	 − 0.15 − 0.25	V
Common Mode Rejection (V_{in} = 0 V to 5.0 V)	11	CMR	60	90	−	dB
Power Supply Rejection Ratio V_{CC}/V_{EE} = 5.0 V/GND to 3.0 V/GND	12	PSRR	 500	 25	 −	μV/V
Output Short Circuit Current (Source and Sink)	13, 14	I_{SC}	50	80	−	mA
Power Supply Current per Amplifier (V_O = 0 V) T_A = − 40° to +105°C T_A = − 55° to +125°C	15	I_D	 − −	 0.9 0.9	 1.125 1.125	mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = + 5.0 V, V_{EE} = Ground, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_S = ± 2.5 V, V_O = − 2.0 V to + 2.0 V, R_L = 2.0 kΩ, A_V = +1.0)	16, 26	SR	 0.5	 1.0	 −	V/μs
Gain Bandwidth Product (f = 100 kHz)	17	GBW	−	2.2	−	MHz
Gain Margin (R_L = 600 Ω, C_L = 0 pF)	20, 21, 22	A_M	−	12	−	dB
Phase Margin (R_L = 600 Ω, C_L = 0 pF)	20, 21, 22	ϕ_M	−	65	−	Deg
Channel Separation (f = 1.0 Hz to 20 kHz, A_V = 100)	23	CS	−	90	−	dB
Power Bandwidth (V_O = 4.0 V_{pp}, R_L = 600 Ω, THD ≤ 1 %)		BW_P	−	28	−	kHz
Total Harmonic Distortion (R_L = 600 Ω, V_O = 1.0 V_{pp}, A_V = 1.0) f = 1.0 kHz f = 10 kHz	24	THD	 − −	 0.002 0.008	 − −	%
Open Loop Output Impedance (V_O = 0 V, f = 2.0 MHz, A_V = 10)		$\lvert Z_O \rvert$	 −	 100	 −	Ω
Differential Input Resistance (V_{CM} = 0 V)		R_{in}	−	200	−	kΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{in}	−	8.0	−	pF
Equivalent Input Noise Voltage (R_S = 100 Ω) f = 10 Hz f = 1.0 kHz	25	e_n	 − −	 25 20	 − −	$\frac{nV}{\sqrt{Hz}}$
Equivalent Input Noise Current f = 10 Hz f = 1.0 kHz	25	i_n	 − −	 0.8 0.2	 − −	$\frac{pA}{\sqrt{Hz}}$

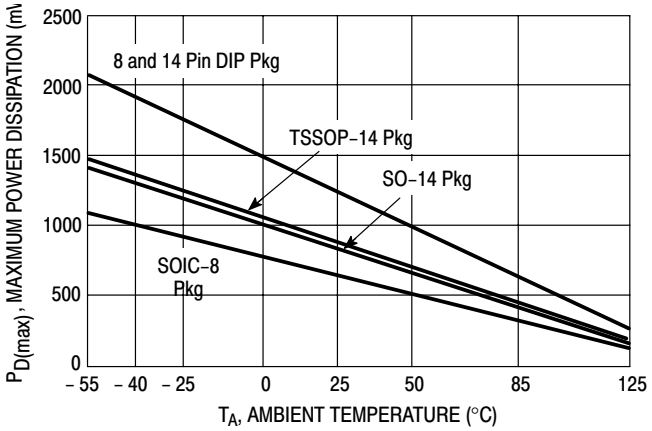


Figure 2. Maximum Power Dissipation versus Temperature

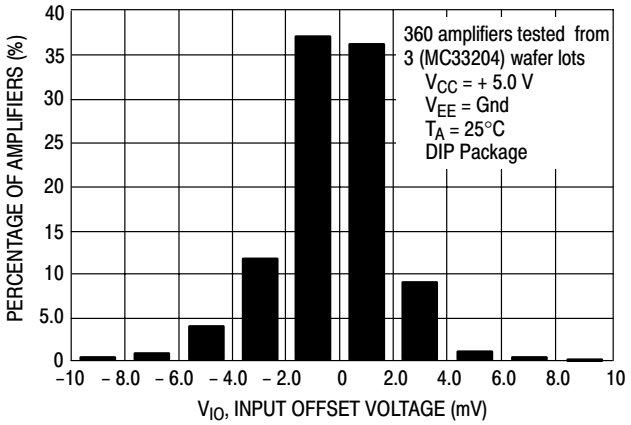


Figure 3. Input Offset Voltage Distribution

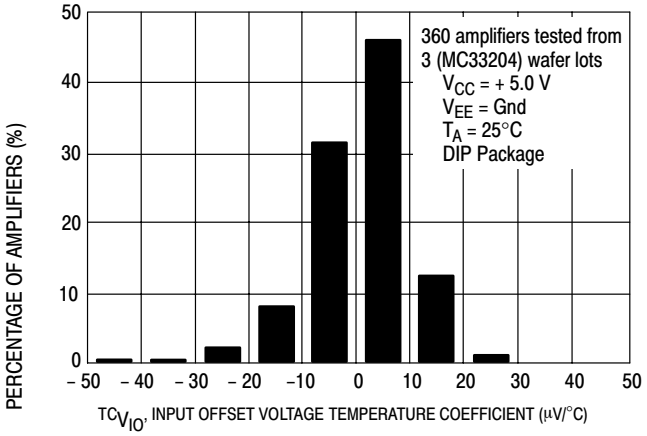


Figure 4. Input Offset Voltage Temperature Coefficient Distribution

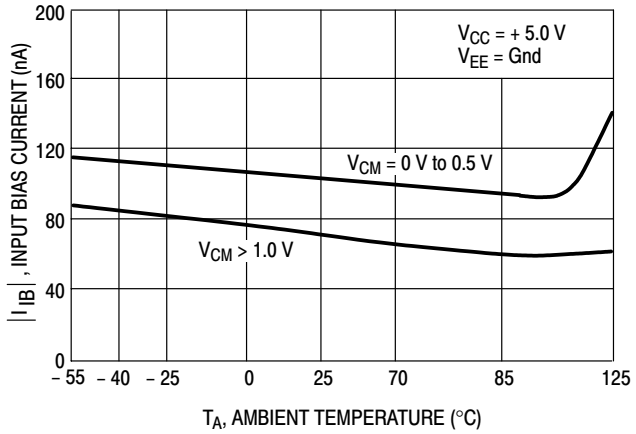


Figure 5. Input Bias Current versus Temperature

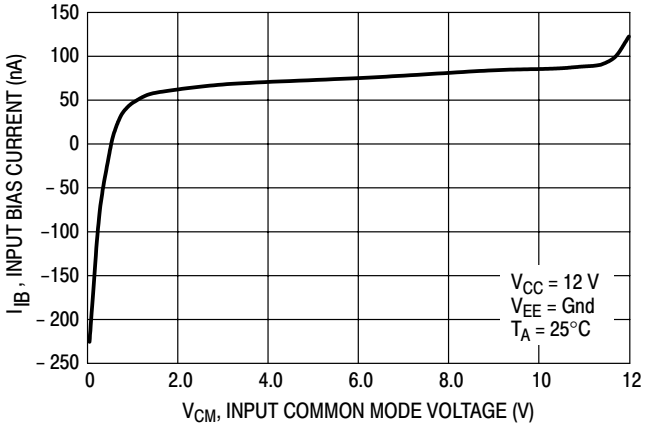


Figure 6. Input Bias Current versus Common Mode Voltage

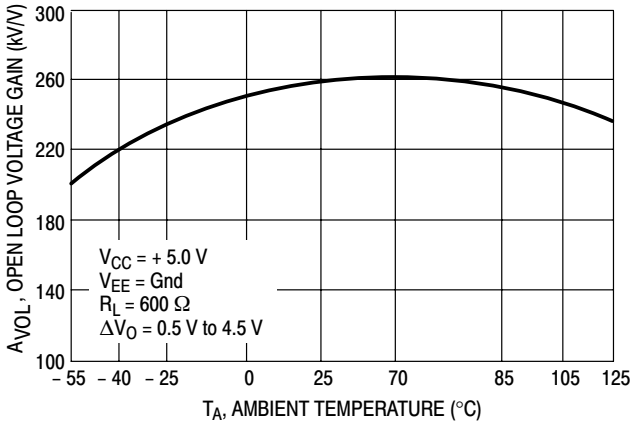


Figure 7. Open Loop Voltage Gain versus Temperature

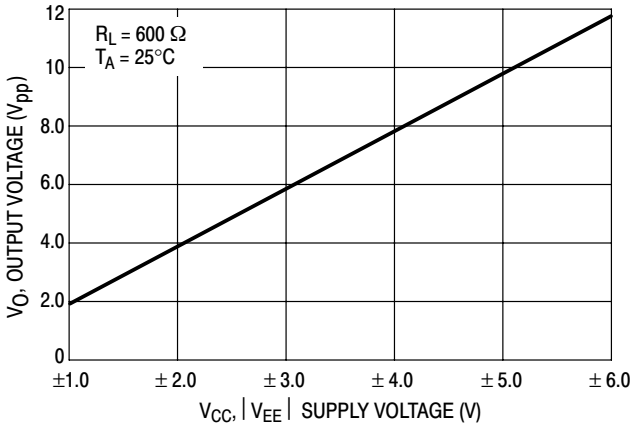


Figure 8. Output Voltage Swing versus Supply Voltage

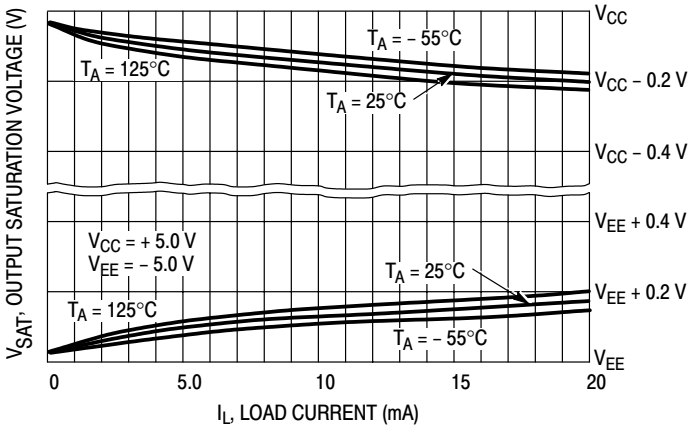


Figure 9. Output Saturation Voltage versus Load Current

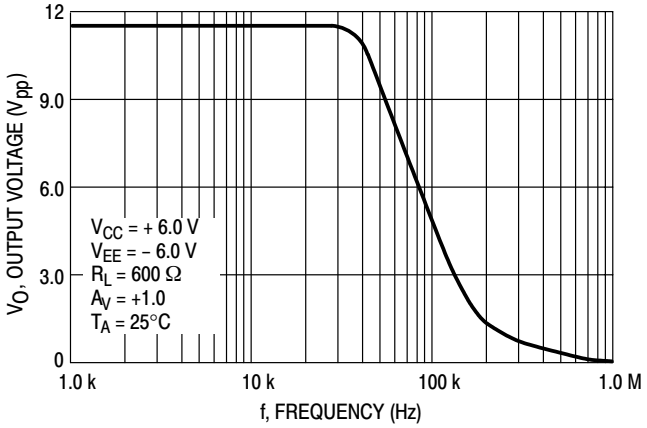


Figure 10. Output Voltage versus Frequency

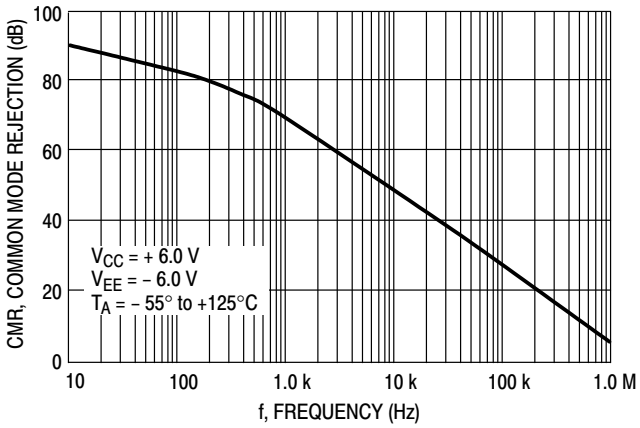


Figure 11. Common Mode Rejection versus Frequency

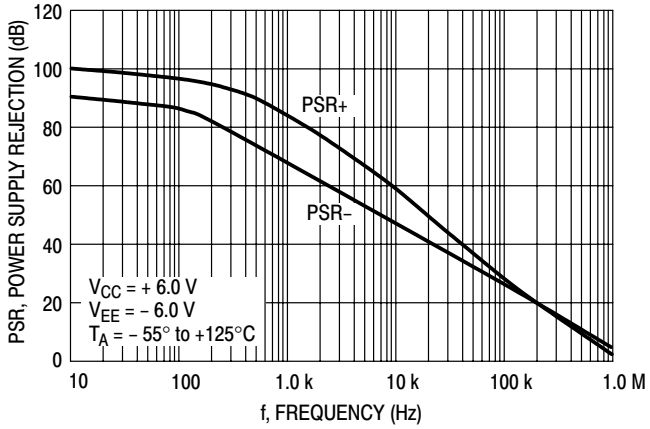


Figure 12. Power Supply Rejection versus Frequency

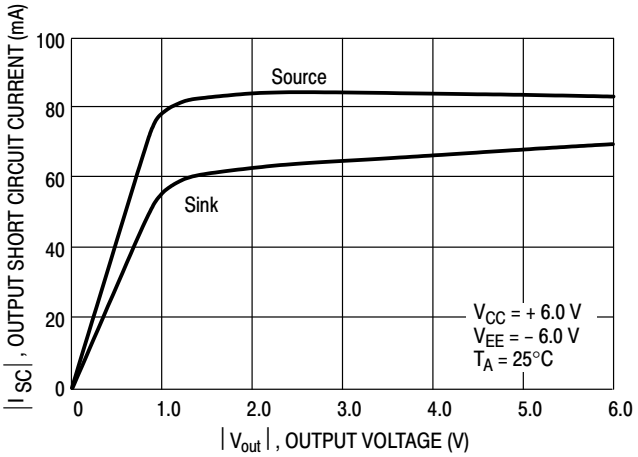


Figure 13. Output Short Circuit Current versus Output Voltage

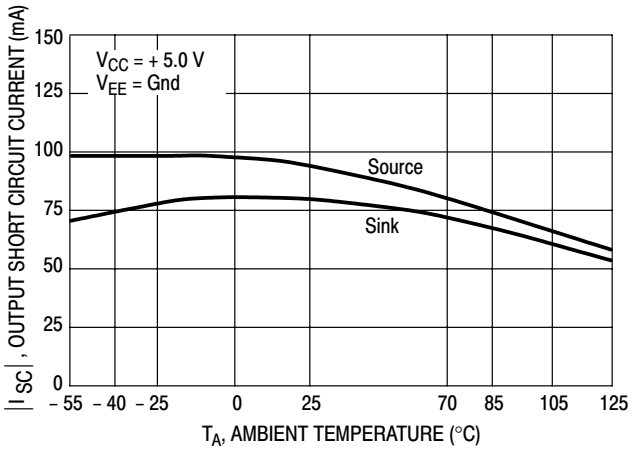


Figure 14. Output Short Circuit Current versus Temperature

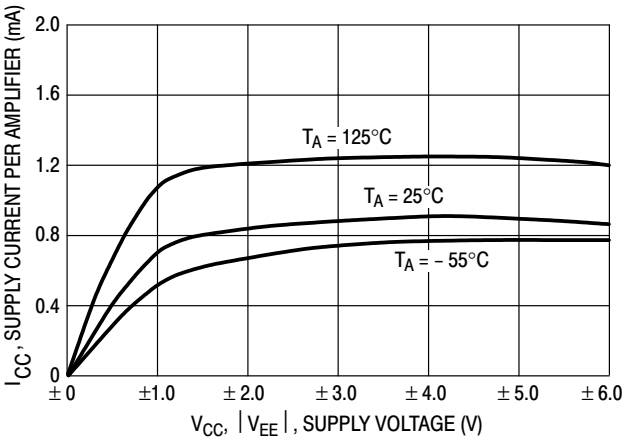


Figure 15. Supply Current per Amplifier versus Supply Voltage with No Load

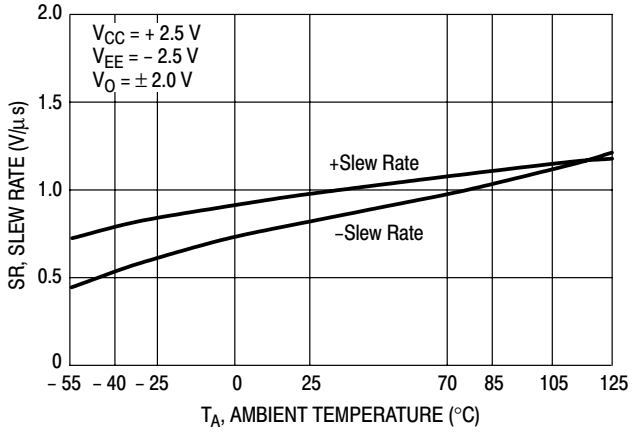


Figure 16. Slew Rate versus Temperature

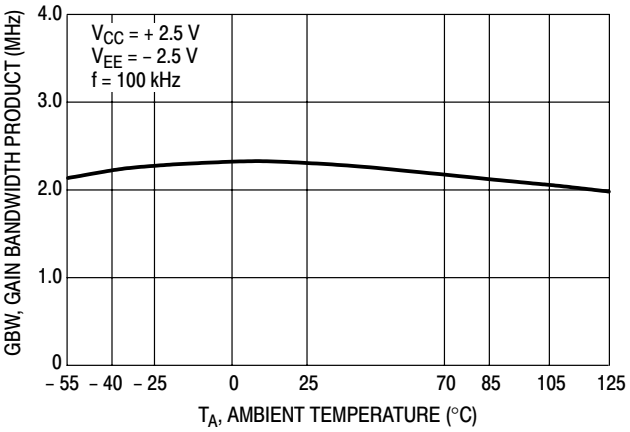


Figure 17. Gain Bandwidth Product versus Temperature

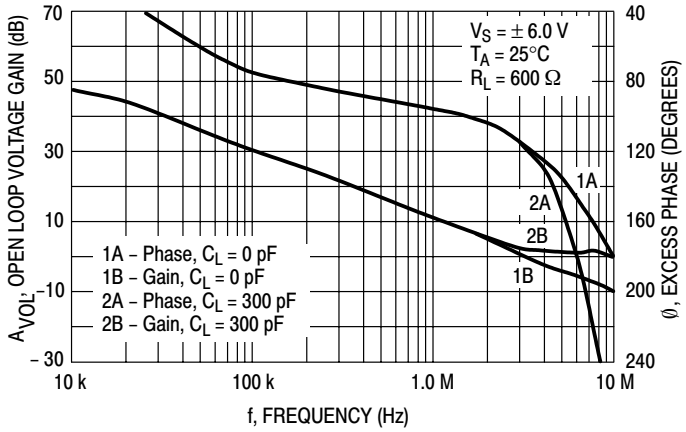


Figure 18. Voltage Gain and Phase versus Frequency

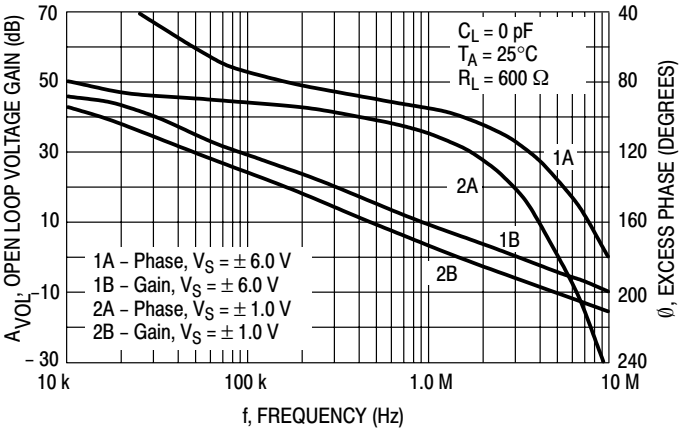


Figure 19. Voltage Gain and Phase versus Frequency

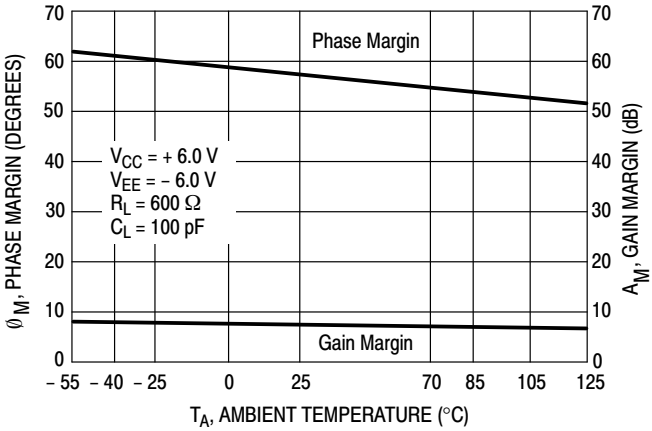


Figure 20. Gain and Phase Margin versus Temperature

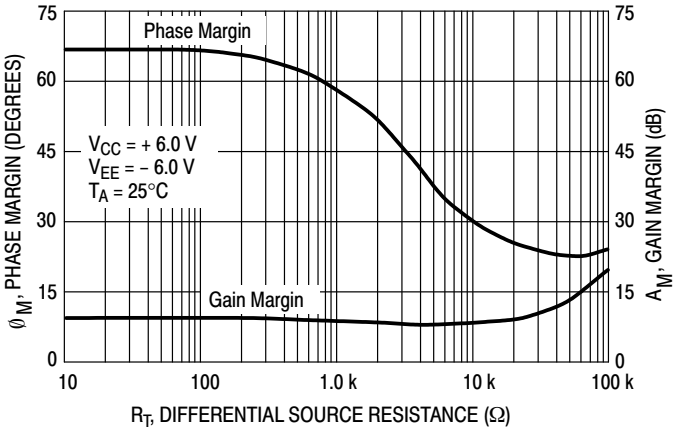


Figure 21. Gain and Phase Margin versus Differential Source Resistance

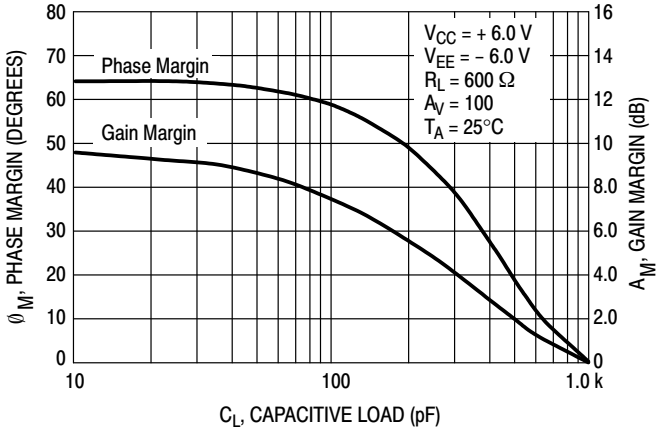


Figure 22. Gain and Phase Margin versus Capacitive Load

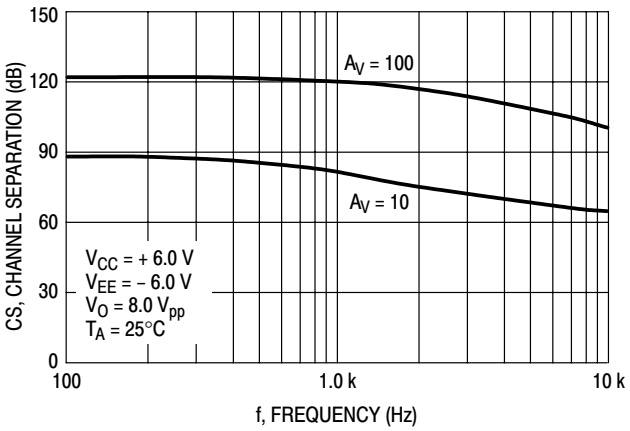


Figure 23. Channel Separation versus Frequency

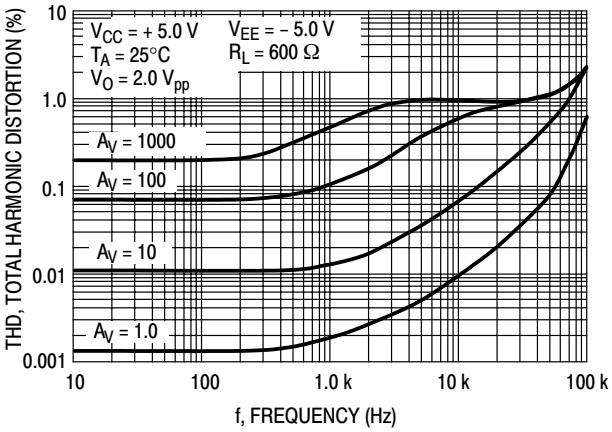


Figure 24. Total Harmonic Distortion versus Frequency

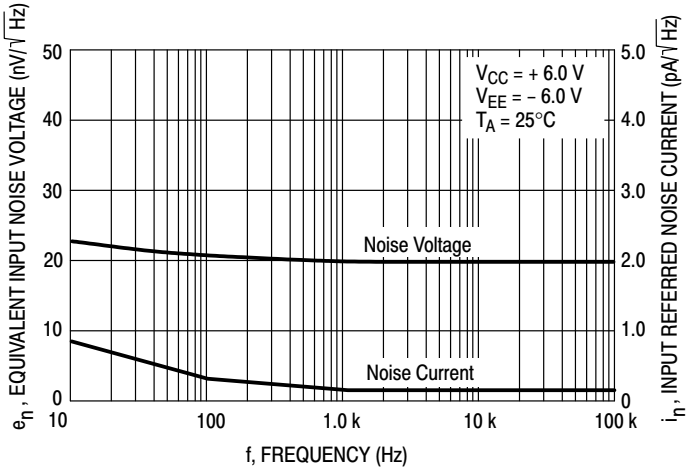


Figure 25. Equivalent Input Noise Voltage and Current versus Frequency

DETAILED OPERATING DESCRIPTION

General Information

The MC33201/2/4 family of operational amplifiers are unique in their ability to swing rail−to−rail on both the input and the output with a completely bipolar design. This offers low noise, high output current capability and a wide common mode input voltage range even with low supply voltages. Operation is guaranteed over an extended temperature range and at supply voltages of 2.0 V, 3.3 V and 5.0 V and ground.

Since the common mode input voltage range extends from V_{CC} to V_{EE}, it can be operated with either single or split voltage supplies. The MC33201/2/4 are guaranteed not to latch or phase reverse over the entire common mode range, however, the inputs should not be allowed to exceed maximum ratings.

Circuit Information

Rail−to−rail performance is achieved at the input of the amplifiers by using parallel NPN−PNP differential input stages. When the inputs are within 800 mV of the negative rail, the PNP stage is on. When the inputs are more than 800 mV greater than V_{EE}, the NPN stage is on. This switching of input pairs will cause a reversal of input bias currents (see Figure 6). Also, slight differences in offset voltage may be noted between the NPN and PNP pairs. Cross−coupling techniques have been used to keep this change to a minimum.

In addition to its rail−to−rail performance, the output stage is current boosted to provide 80 mA of output current, enabling the op amp to drive 600 Ω loads. Because of this high output current capability, care should be taken not to exceed the 150°C maximum junction temperature.

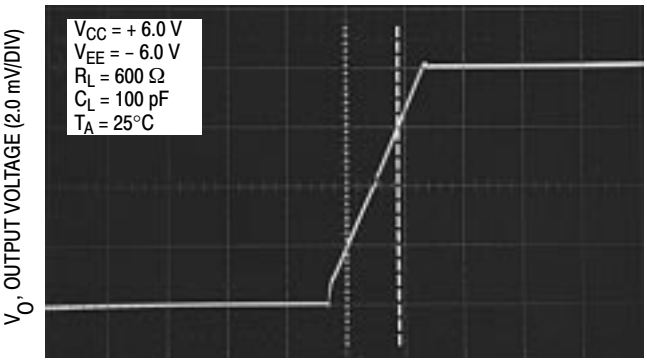


Figure 26. Noninverting Amplifier Slew Rate

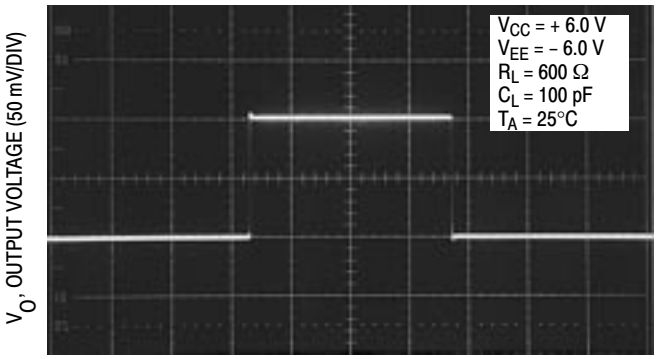


Figure 27. Small Signal Transient Response

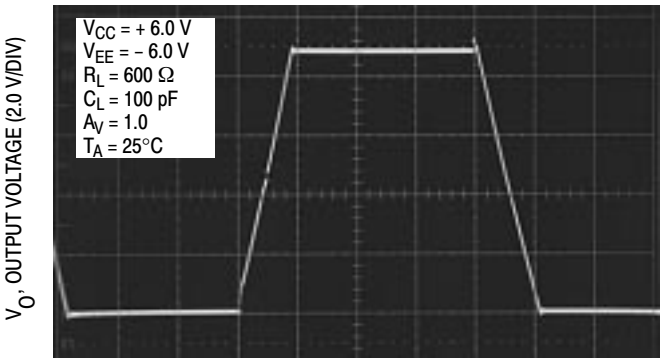


Figure 28. Large Signal Transient Response

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self−align when subjected to a solder reflow process.

ORDERING INFORMATION

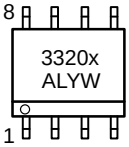
Operational Amplifier Function	Device	Operating Temperature Range	Package	Shipping†
Single	MC33201D	T_A= −40° to +105°C	SOIC−8	98 Units / Rail
	MC33201DR2		SOIC−8	2500 Units / Tape & Reel
	MC33201P		PDIP−8	50 Units / Rail
	MC33201VD	T_A = −55° to 125°C	SOIC−8	98 Units / Rail
Dual	MC33202D	T_A= −40 ° to +105°C	SOIC−8	98 Units / Rail
	MC33202DG		SOIC−8 (Pb−Free)	
	MC33202DR2		SOIC−8	2500 Units / Tape & Reel
	MC33202DR2G		SOIC−8 (Pb−Free)	
Dual	MC33202DMR2	T_A= −40 ° to +105°C	Micro−8	4000 Units / Tape & Reel
	MC33202P		PDIP−8	50 Units / Rail
	MC33202VD	T_A = −55° to 125°C	SOIC−8	98 Units / Rail
	MC33202VDR2		SOIC−8	2500 Units / Tape & Reel
	NCV33202VDR2*		SOIC−8	2500 Units / Tape & Reel
	MC33202VP		PDIP−8	50 Units / Rail
Quad	MC33204D	T_A= −40 ° to +105°C	SO−14	55 Units / Rail
	MC33204DR2		SO−14	2500 Units / Tape & Reel
	MC33204DTB		TSSOP−14	96 Units / Rail
	MC33204DTBR2		TSSOP−14	2500 Units / Tape & Reel
	MC33204P		PDIP−14	25 Units / Rail
	MC33204VD	T_A = −55° to 125°C	SO−14	55 Units / Rail
	MC33204VDR2		SO−14	2500 Units / Tape & Reel
	NCV33204DR2*		SO−14	2500 Units / Tape & Reel
	NCV33204DTBR2*		TSSOP−14	2500 Units / Tape & Reel
	MC33204VP		PDIP−14	25 Units / Rail

*NCV33202 and NCV33204 are qualified for automotive use.

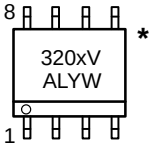
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS

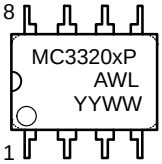
SOIC−8
D SUFFIX
CASE 751



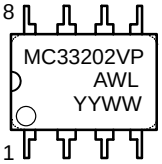
SOIC−8
VD SUFFIX
CASE 751



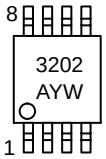
PDIP−8
P SUFFIX
CASE 626



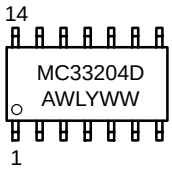
PDIP−8
VP SUFFIX
CASE 626



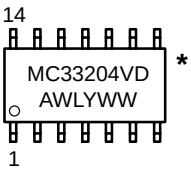
Micro−8
DM SUFFIX
CASE 846A



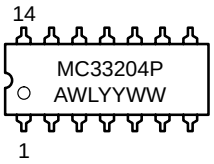
SO−14
D SUFFIX
CASE 751A



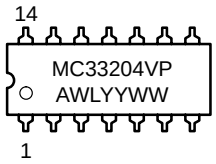
SO−14
VD SUFFIX
CASE 751A



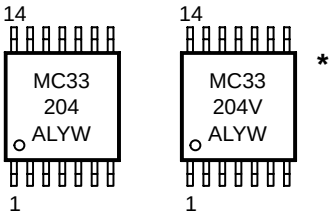
PDIP−14
P SUFFIX
CASE 646



PDIP−14
VP SUFFIX
CASE 646



TSSOP−14
DTB SUFFIX
CASE 948G

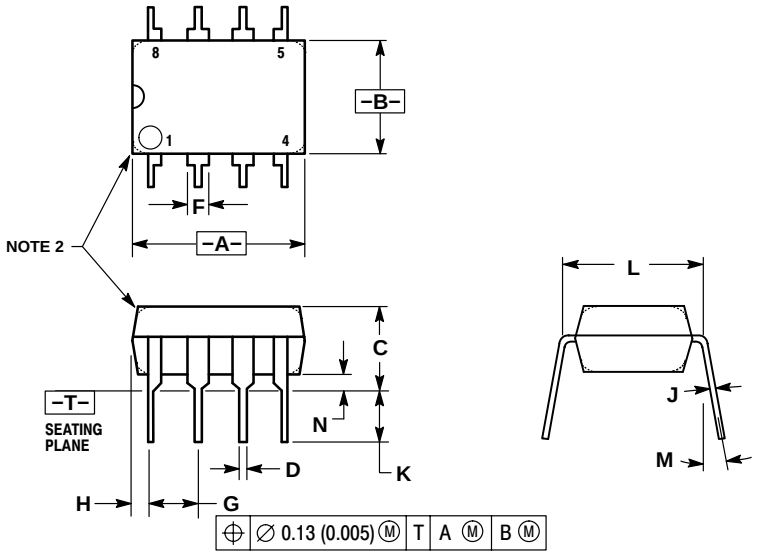


x = 1 or 2
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

*This marking diagram applies to NCV3320x

PACKAGE DIMENSIONS

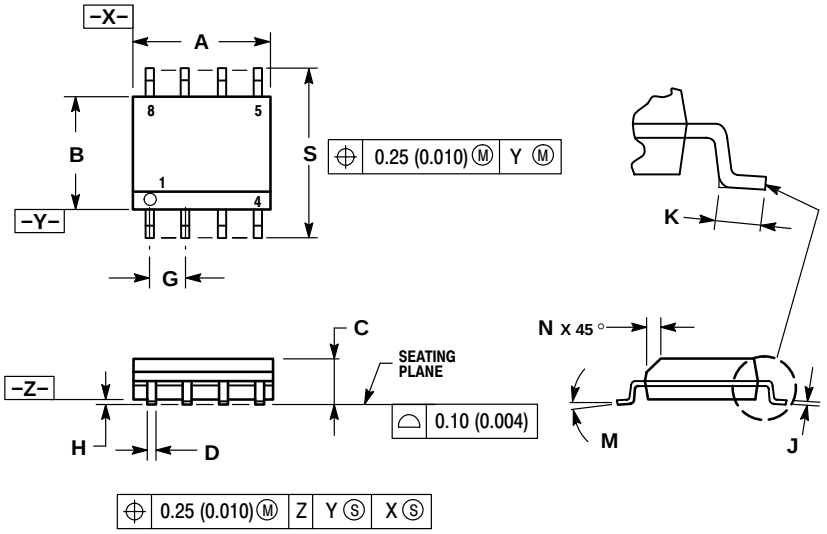
PDIP−8
P, VP SUFFIX
CASE 626−05
ISSUE L



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

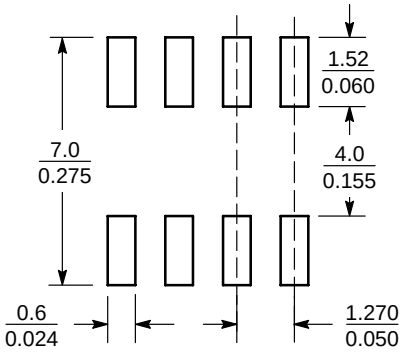
SOIC−8
D, VD SUFFIX
CASE 751−07
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDAARD IS 751−07

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



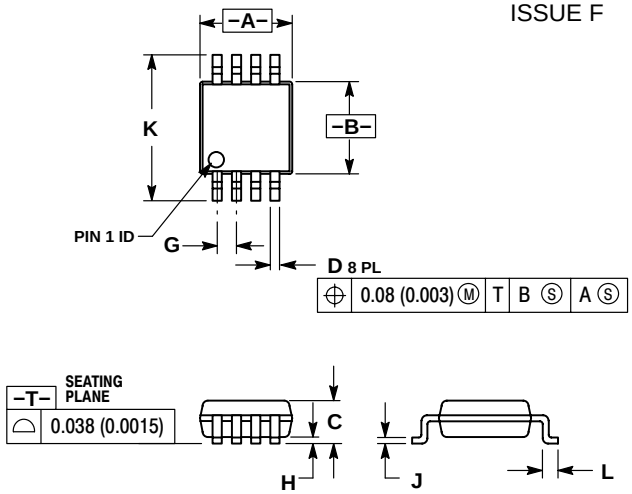
SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

SOIC−8

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

Micro8
DM SUFFIX
CASE 846A−02
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A−01 OBSOLETE, NEW STANDARD 846A−02.

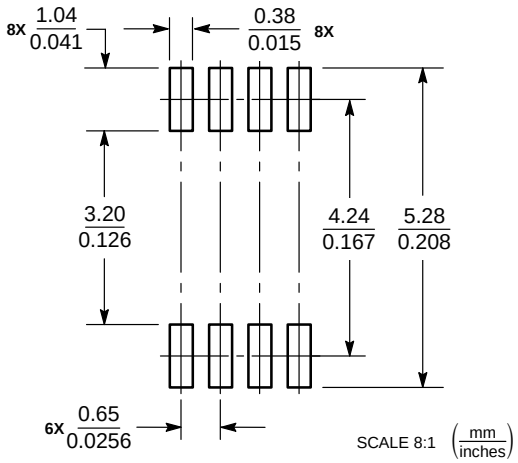
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	---	1.10	---	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

SOLDERING FOOTPRINT*

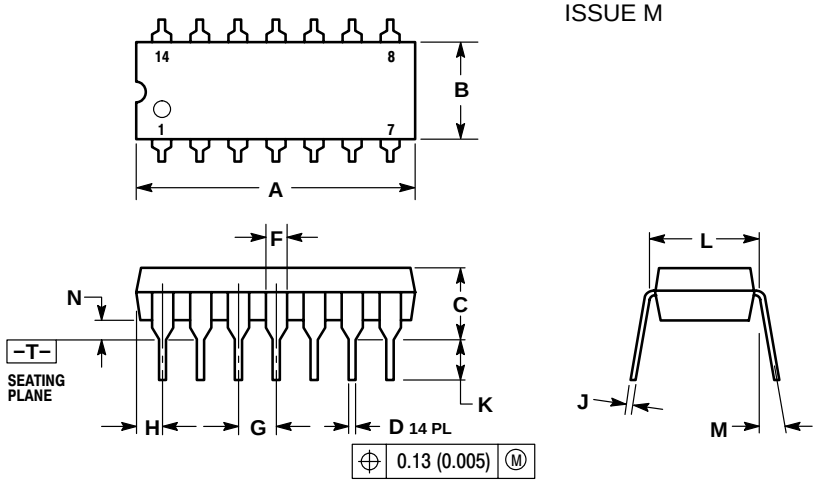


Micro8™

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

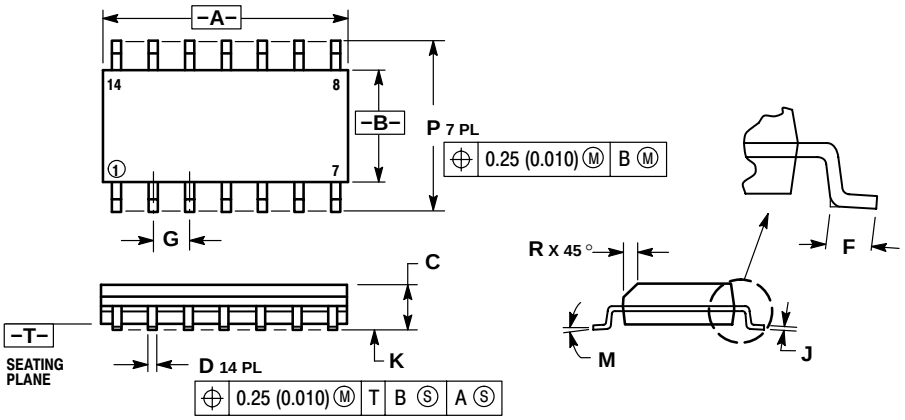
PDIP−14
P, VP SUFFIX
CASE 646−06
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

SOIC−14
D, VD SUFFIX
CASE 751A−03
ISSUE F

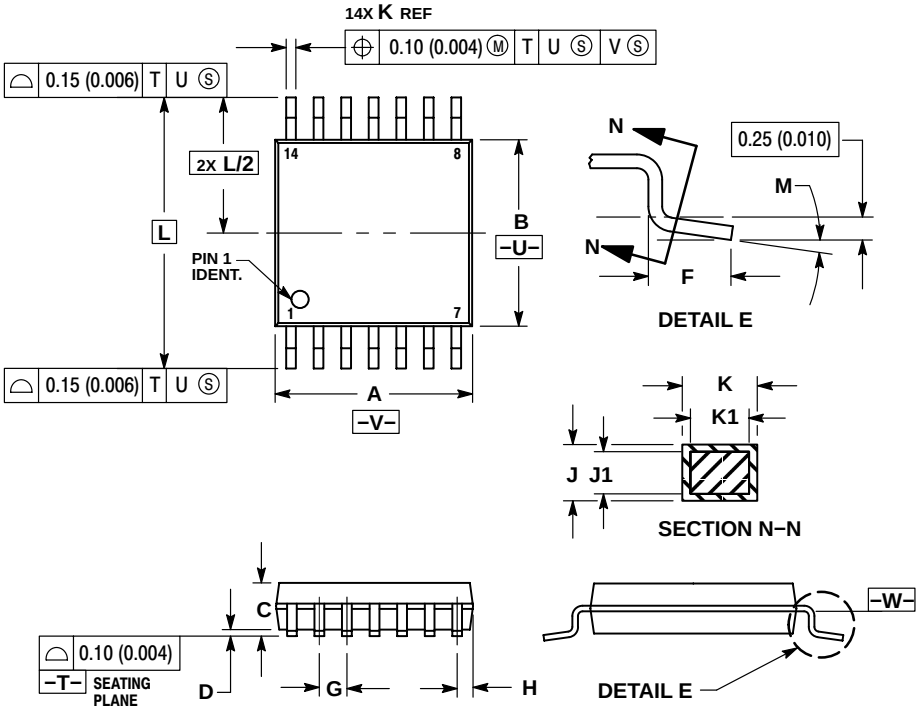


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

TSSOP−14
DTB SUFFIX
CASE 948G−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

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