LINEAR SYSTEMS

LS3N165
P-CHANNEL MOSFET

micross

The LS3N165 is a monolithic dual enhancement mode P-Channel Mosfet

The LS3N165 is a dual enhancement mode P-Channel Mosfet and is ideal for space constrained applications and those requiring tight electrical matching.

The hermetically sealed TO-78 package is well suited for high reliability and harsh environment applications.

(See Packaging Information).

LS3N165 Features:

- Very high Input Impedance
- Low Capacitance
- High Gain
- High Gate Breakdown Voltage
- Low Threshold Voltage

FEATURES	
DIRECT REPLACEMENT FOR INTERSIL LS3N165	
ABSOLUTE MAXIMUM RATINGS[1] @ 25°C (unless otherwise noted)	
Maximum Temperatures	
Storage Temperature	-65°C to +200°C
Operating Junction Temperature	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Maximum Power Dissipation	
Continuous Power Dissipation (one side)	300mW
Total Derating above 25°C	4.2 mW/°C
MAXIMUM CURRENT	
Drain Current	50mA
MAXIMUM VOLTAGES	
Drain to Gate or Drain to Source[2]	-40V
Peak Gate to Source[3]	±125V
Gate-Gate Voltage	±80V

LS3N165 ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN	TYP.	MAX	UNITS	CONDITIONS
I_{GSSR}	Gate Reverse Leakage Current	--	--	10	pA	V_{GS} = -0V
I_{GSSF}	Gate Forward Current	--	--	-10		V_{GS} = -40V
	T_A = +125°C	--	--	-25		
I_{DSS}	Drain to Source Leakage Current	--	--	-200		V_{DS} = -20V
I_{SDS}	Source to Drain Leakage Current	--	--	-400		V_{SD} = -20V V_{DB} = 0
$I_{D(on)}$	Drain Current "On"	-5.0	--	-30	mA	V_{DS} = -15V, V_{GS} = -10V
$V_{GS(th)}$	Gate to Source Threshold Voltage	-2.0	--	-5.0	V	V_{DS} = -15V, I_D = -10µA
		-2.0	--	-5.0		V_{DS} = V_{GS}, I_D = -10µA
$r_{DS(on)}$	Drain to Source "On" Resistance	--	--	300	Ω	V_{GS} = -20V, I_D = -100µA
g_{fs}	Forward Transconductance	1500	--	3000	µS	V_{DS} = -15V, I_D = -10mA, f = 1kHz
g_{os}	Output Admittance	--	--	300		
C_{iss}	Input Capacitance	--	--	3	pF	V_{DS} = -15V, I_D = -10mA, f = 1MHz[4]
C_{rss}	Reverse Transfer Capacitance	--	--	0.7		
C_{oss}	Output Capacitance	--	--	3.0		
$R_E(Y_{fs})$	Common Source Forward Transconductance	1200	--	--	µS	V_{DS} = -15V, I_D = -10mA, f = 100MHz[4]

MATCHING CHARACTERISTICS LS3N165

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS MAX	UNITS	CONDITIONS
Y_{fs1}/Y_{fs2}	Forward Transconductance Ratio	0.90	1.0	ns	V_{DS} = -15V, I_D = -500µA, f = MHz[4]
V_{GS1-2}	Gate Source Threshold Voltage Differential	--	100	mV	V_{DS} = -15V, I_D = -500µA
$\Delta V_{GS1-2}/\Delta T$	Gate Source Threshold Voltage Differential Change with Temperature	--	100	µV/°C	V_{DS} = -15V, I_D = -500µA T_A = -55°C to = +25°C

Note 1 - Absolute maximum ratings are limiting values above which LS3N165 serviceability may be impaired.
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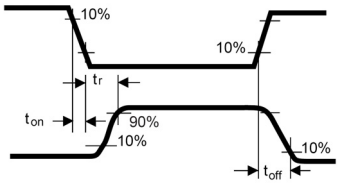
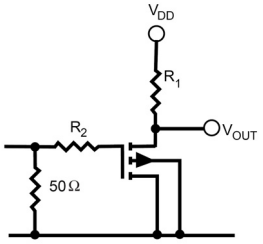
Note 2 – Per Transistor
Note 3 – Device must not be tested at ±125V more than once or longer than 300ms.

SWITCHING WAVEFORM & TEST CIRCUIT



INPUT PULSE
Rise Time≤2ns
Pulse Width≥200ns

SAMPLING SCOPE
T_r≤0.2ns
C_{IN}≤2pF
R_{IN}≥10M

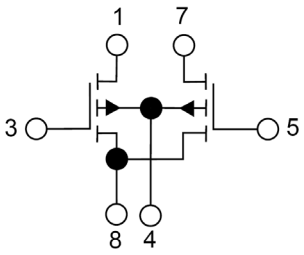


Available Packages:

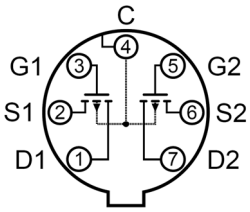
LS3N165 in TO-72
LS3N165 in bare die.

Please contact Micross for full package and die dimensions

Device Schematic



TO-78 (Bottom View)



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Tel: +44 1603 788967
Email: chipcomponents@micross.com
Web: http://www.micross.com/distribution

*To avoid possible damage to the device while wiring, testing, or in actual operation, follow these procedures: To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used. Avoid unnecessary handling. Pick up devices by the case instead of the leads. Do not insert or remove devices from circuits with the power on, as transient voltages may cause permanant damage to the devices.