

Silicon NPN Power Transistors

2SD905

DESCRIPTION

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- With TO-3 package
- High voltage ,high speed

APPLICATIONS

- For high voltage power switching TV horizontal deflection output applications

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

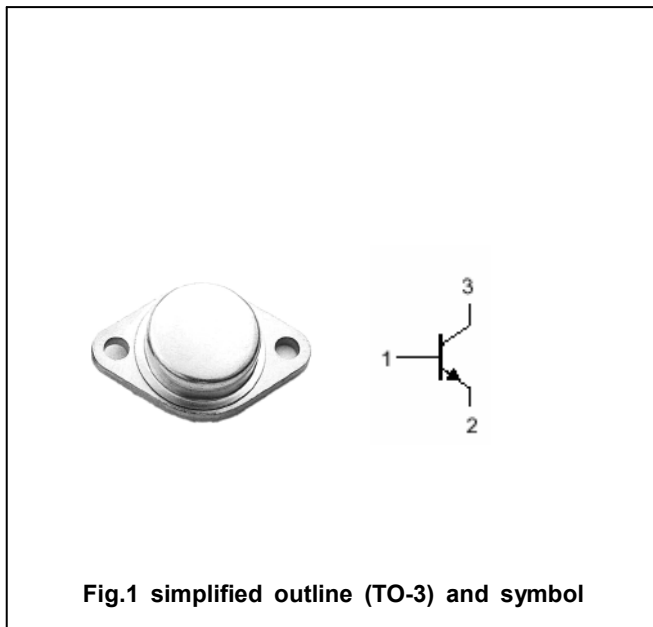


Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings(Ta=□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CBO}	Collector-base voltage	Open emitter	1400	V
V _{CEO}	Collector-emitter voltage	Open base	650	V
V _{EBO}	Emitter-base voltage	Open collector	5	V
I _C	Collector current		8	A
I _{CM}	Collector current-peak		10	A
P _C	Collector power dissipation	T _C =25□	50	W
T _j	Junction temperature		150	□
T _{stg}	Storage temperature		-45~150	□

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CHARACTERISTICS

T_j=25°C unless otherwise specified

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =10mA ; R _{BE} =∞	650			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =10mA ; I _C =0	5			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =8A; I _B =1.5A			10	V
V _{BEsat}	Base-emitter saturation voltage	I _C =8A; I _B =1.5A			1.5	V
I _{CES}	Collector cut-off current	V _{CE} =1400V ; R _{BE} =0			0.5	mA
I _{EBO}	Emitter cut-off current	V _{EB} =5V; I _C =0			0.5	mA
h _{FE}	DC current gain	I _C =1A ; V _{CE} =5V	8		36	
t _f	Fall time	I _C =6.8A; I _{B1} =1.1A; L _B =0			1.0	μs

PACKAGE OUTLINE

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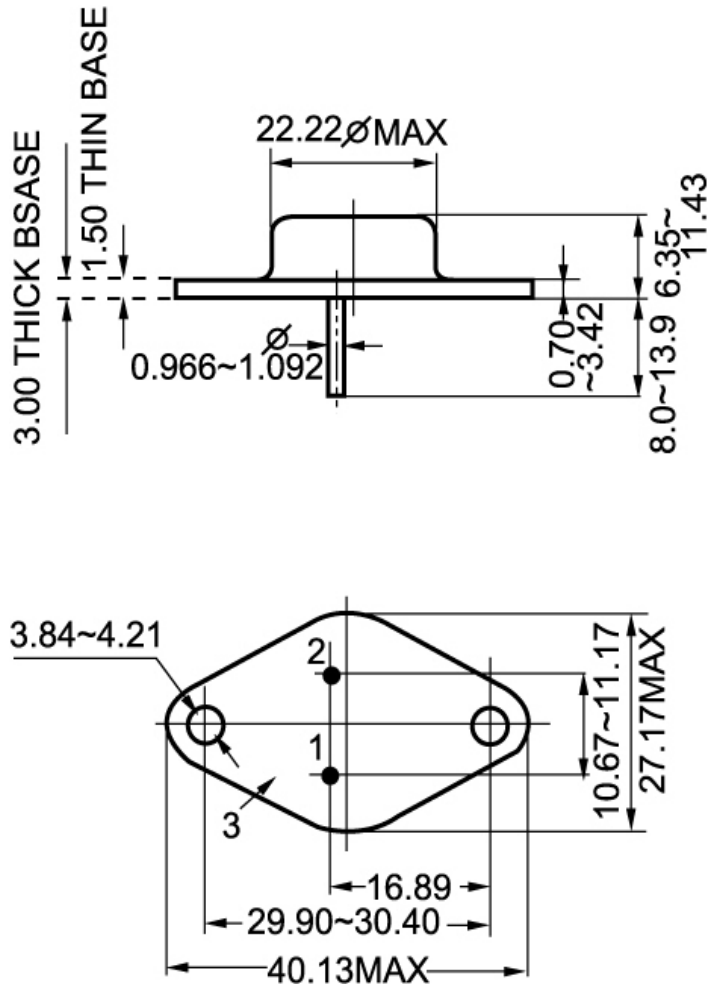


Fig.2 outline dimensions (unindicated tolerance:±0.1mm)