

128Mbit GDDR SDRAM

***2M x 16Bit x 4 Banks
Graphic Double Data Rate
Synchronous DRAM***

Revision 1.2

November 2006

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Revision History

Revision	Month	Year	History
0.0	March	2005	- <i>Target Spec</i> - Defined target specification
0.1	May	2005	- Corrected typo. - Added CL2 feature in AC Characteristics.
1.0	August	2005	- Finalized SPEC - Deleted CL2.5 option
1.1	January	2006	- Corrected typo.
1.2	November	2006	- Corrected typo.

2M x 16Bit x 4 Banks Double Data Rate Synchronous DRAM with Bi-directional Data Strobe and DLL

1.0 FEATURES

- 2.5V \pm 5% power supply for device operation
- 2.5V \pm 5% power supply for I/O interface
- SSTL_2 compatible inputs/outputs
- 4 banks operation
- MRS cycle with address key programs
 - Read latency 2,3(clock)
 - Burst length (2, 4 and 8)
 - Burst type (sequential & interleave)
- All inputs except data & DM are sampled at the positive going edge of the system clock
- Differential clock input
- Write-Interrupted by Read Function
- 2 DQS's (1DQS / Byte)
- Data I/O transactions on both edges of Data strobe
- DLL aligns DQ and DQS transitions with Clock transition
- Edge aligned data & data strobe output
- Center aligned data & data strobe input
- DM for write masking only
- Auto & Self refresh
- 32ms refresh period (4K cycle)
- Lead free 66pin TSOP-II (RoHS compliant)
- Maximum clock frequency up to 250MHz
- Maximum data rate up to 500Mbps/pin

2.0 ORDERING INFORMATION

Part NO.	Max Freq.	Max Data Rate	Interface	Package
K4D261638I-LC40	250MHz	500Mbps/pin	SSTL_2	66pin TSOP-II
K4D261638I-LC50	200MHz	400Mbps/pin		

* K4D261638I-TC is the Leaded package part number.

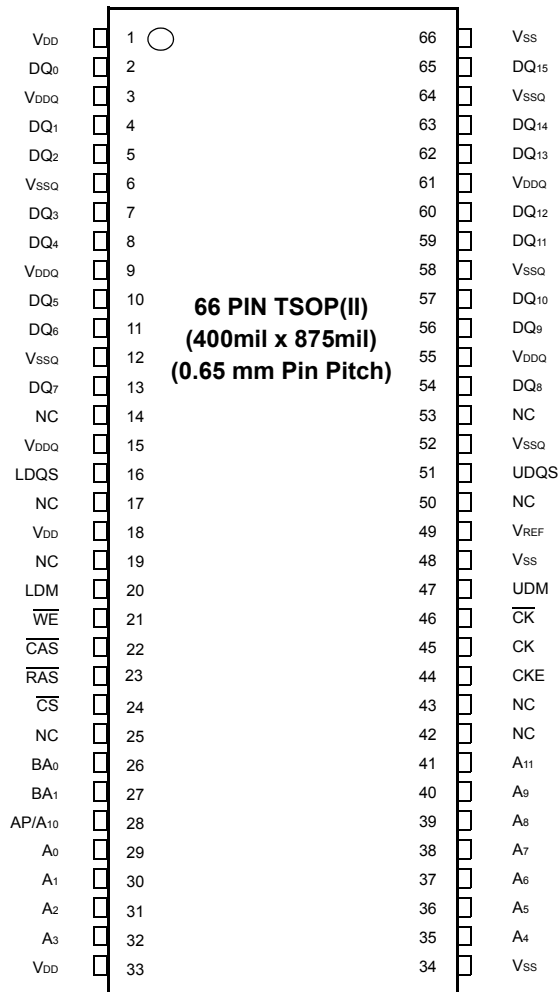
* For K4D261638I-LC50, VDD & VDDQ = 2.375V to 2.7V.

3.0 GENERAL DESCRIPTION

FOR 2M x 16Bit x 4 Bank DDR SDRAM

The K4D261638I is 134,217,728 bits of hyper synchronous data rate Dynamic RAM organized as 4 x 2,097,152 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 1GB/s/chip. I/O transactions are possible on both edges of the clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

4.0 PIN CONFIGURATION (Top View)



PIN DESCRIPTION

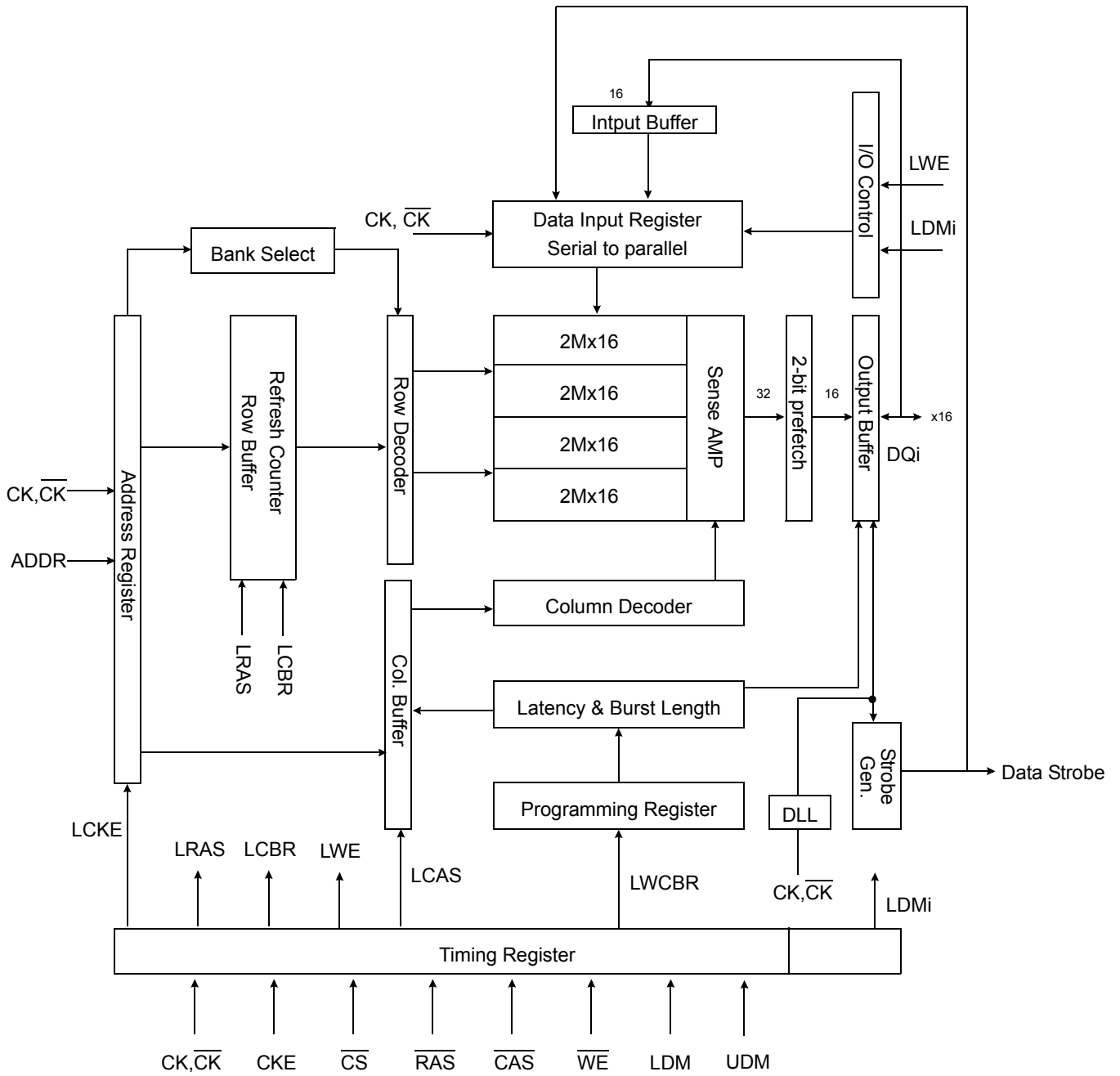
CK, \overline{CK}	Differential Clock Input	BA0, BA1	Bank Select Address
CKE	Clock Enable	A0 ~A11	Address Input
\overline{CS}	Chip Select	DQ0 ~ DQ15	Data Input/Output
\overline{RAS}	Row Address Strobe	V _{DD}	Power
\overline{CAS}	Column Address Strobe	V _{SS}	Ground
\overline{WE}	Write Enable	V _{DDQ}	Power for DQ's
L(U)DQS	Data Strobe	V _{SSQ}	Ground for DQ's
L(U)DM	Data Mask	NC	No Connection
RFU	Reserved for Future Use		

5.0 INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	Function
CK, \overline{CK}^{*1}	Input	The differential system clock Input. All of the inputs are sampled on the rising edge of the clock except DQ's and DM's that are sampled on both edges of the DQS.
CKE	Input	Activates the CK signal when high and deactivates the \overline{CK} signal when low. By deactivating the clock, CKE low indicates the Power down mode or Self refresh mode.
\overline{CS}	Input	\overline{CS} enables the command decoder when low and disabled the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
\overline{RAS}	Input	Latches row addresses on the positive going edge of the CK with \overline{RAS} low. Enables row access & precharge.
\overline{CAS}	Input	Latches column addresses on the positive going edge of the CK with \overline{CAS} low. Enables column access.
\overline{WE}	Input	Enables write operation and row precharge. Latches data in starting from \overline{CAS} , \overline{WE} active.
LDQS, UDQS	Input/Output	Data input and output are synchronized with both edge of DQS. For the x16, LDQS corresponds to the data on DQ0-DQ7 ; UDQS corresponds to the data on DQ8-DQ15.
LDM, UDM	Input	Data in Mask. Data In is masked by DM Latency=0 when DM is high in burst write. For the x16, LDM corresponds to the data on DQ0-DQ7 ; UDM corresponds to the data on DQ8-DQ15.
DQ0 ~ DQ15	Input/Output	Data inputs/Outputs are multiplexed on the same pins.
BA0, BA1	Input	Selects which bank is to be active.
A0 ~ A11	Input	Row/Column addresses are multiplexed on the same pins. Row addresses : RA0 ~ RA11, Column addresses : CA0 ~ CA8.
V_{DD}/V_{SS}	Power Supply	Power and ground for the input buffers and core logic.
V_{DDQ}/V_{SSQ}	Power Supply	Isolated power supply and ground for the output buffers to provide improved noise immunity.
V_{REF}	Power Supply	Reference voltage for inputs, used for SSTL interface.
NC/RFU	No connection/ Reserved for future use	This pin is recommended to be left "No connection" on the device

*1 : The timing reference point for the differential clocking is the cross point of CK and \overline{CK} .
For any applications using the single ended clocking, apply V_{REF} to \overline{CK} pin.

6.0 BLOCK DIAGRAM (2Mbit x 16I/O x 4 Bank)



7.0 FUNCTIONAL DESCRIPTION

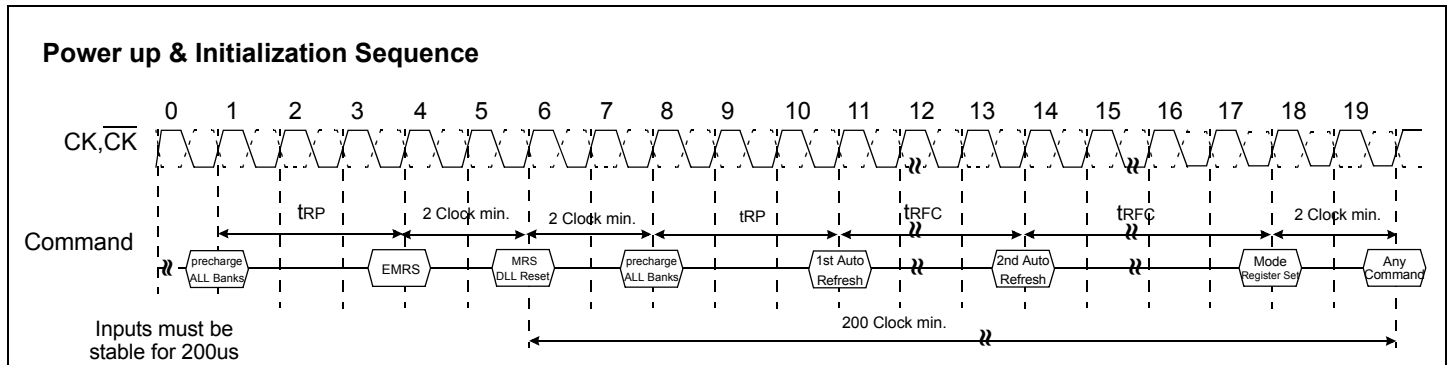
7.1 Power-Up Sequence

DDR SDRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

1. Apply power and keep CKE at low state (All other inputs may be undefined)
 - Apply V_{DD} before V_{DDQ} .
 - Apply V_{DDQ} before V_{REF} & V_{TT}
2. Start clock and maintain stable condition for minimum 200us.
3. The minimum of 200us after stable power and clock(CK, \overline{CK}), apply NOP and take CKE to be high .
4. Issue precharge command for all banks of the device.
5. Issue a EMRS command to enable DLL
- *1 6. Issue a MRS command to reset DLL. The additional 200 clock cycles are required to lock the DLL.
- *1,2 7. Issue precharge command for all banks of the device.
8. Issue at least 2 or more auto-refresh commands.
9. Issue a mode register set command with A8 to low to initialize the mode register.

*1 The additional 200cycles of clock input is required to lock the DLL after enabling DLL.

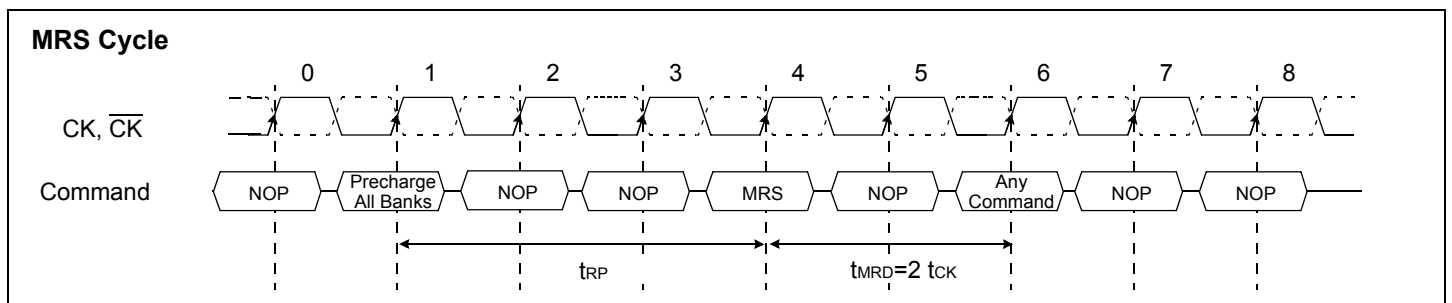
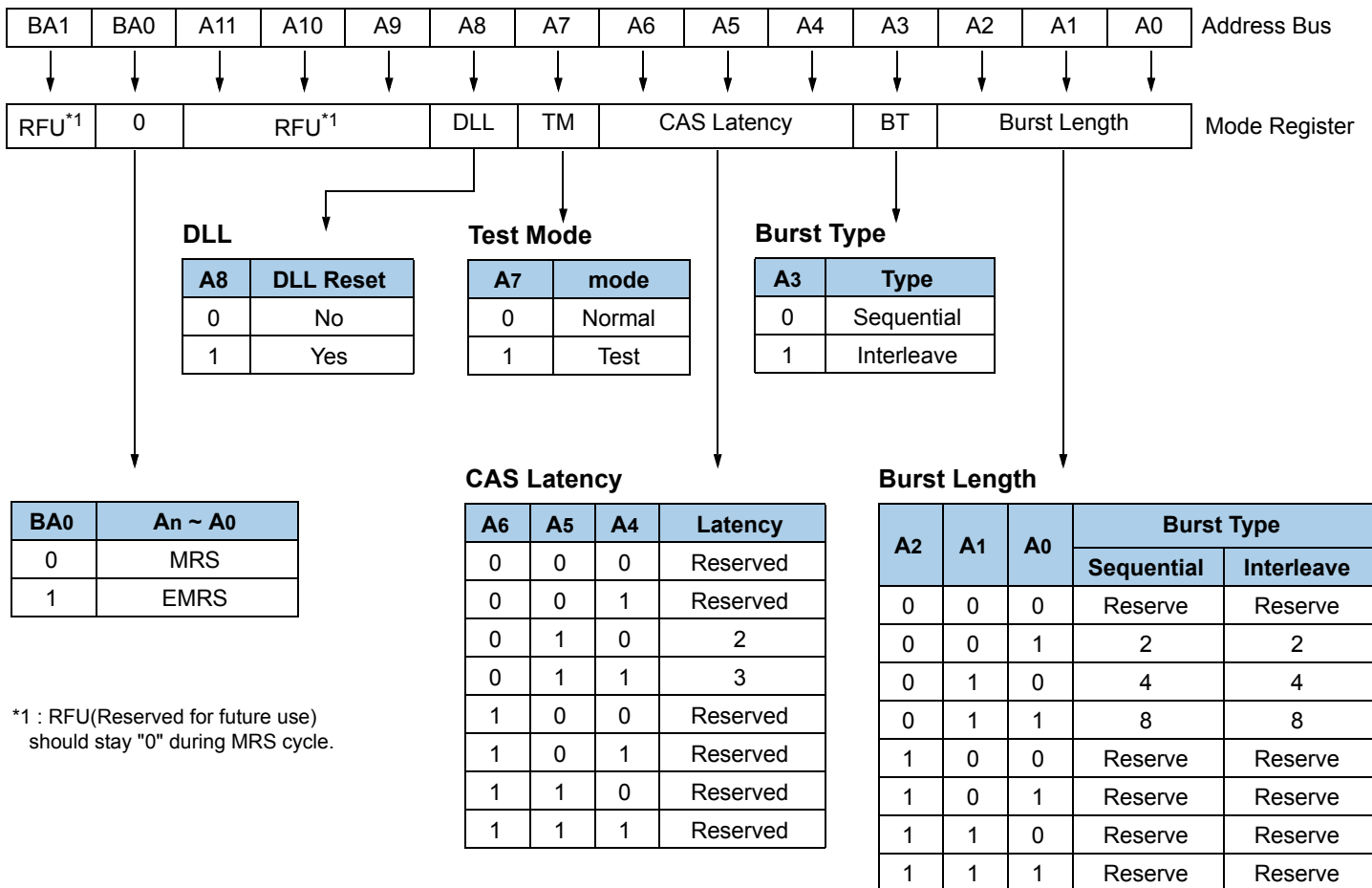
*2 Sequence of 6&7 is regardless of the order.



- * When the operating frequency is changed, DLL reset should be required again.
After DLL reset again, the minimum 200 cycles of clock input is needed to lock the DLL.

7.2 MODE REGISTER SET(MRS)

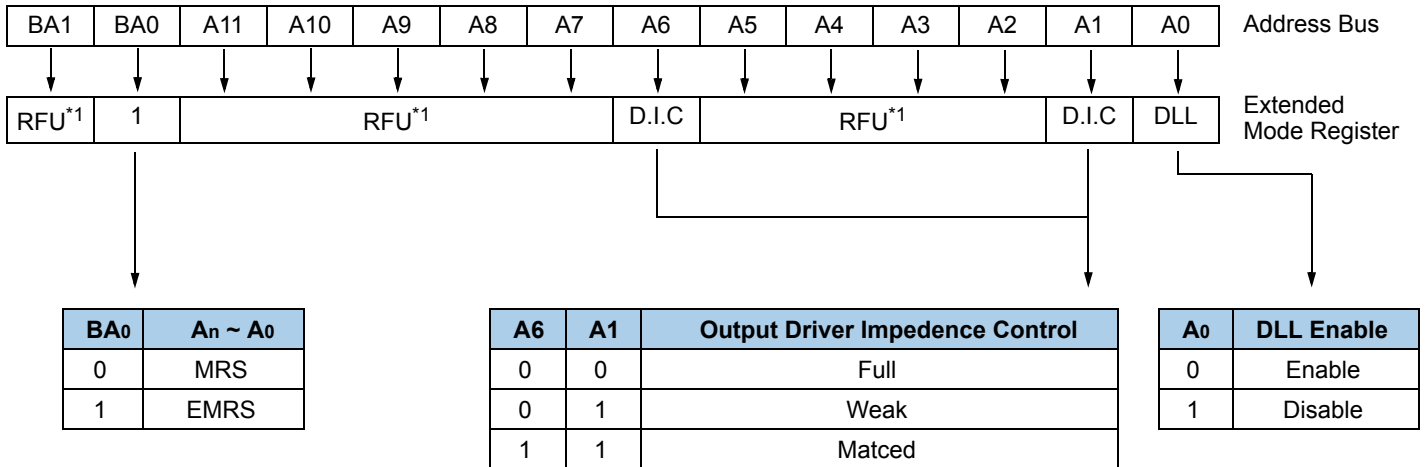
The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs CAS latency, addressing mode, burst length, test mode, DLL reset and various vendor specific options to make DDR SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for proper operation. The mode register is written by asserting low on CS, RAS, CAS and WE(The DDR SDRAM should be in active mode with CKE already high prior to writing into the mode register). The state of address pins A0 ~ A11 and BA0, BA1 in the same cycle as CS, RAS, CAS and WE going low is written in the mode register. Minimum two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0 ~ A2, addressing mode uses A3, CAS latency(read latency from column address) uses A4 ~ A6. A7 is used for test mode. A8 is used for DLL reset. A7,A8, BA0 and BA1 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and CAS latencies.



*1 : MRS can be issued only at all banks precharge state.
 *2 : Minimum tRP is required to issue MRS command.

7.3 EXTENDED MODE REGISTER SET(EMRS)

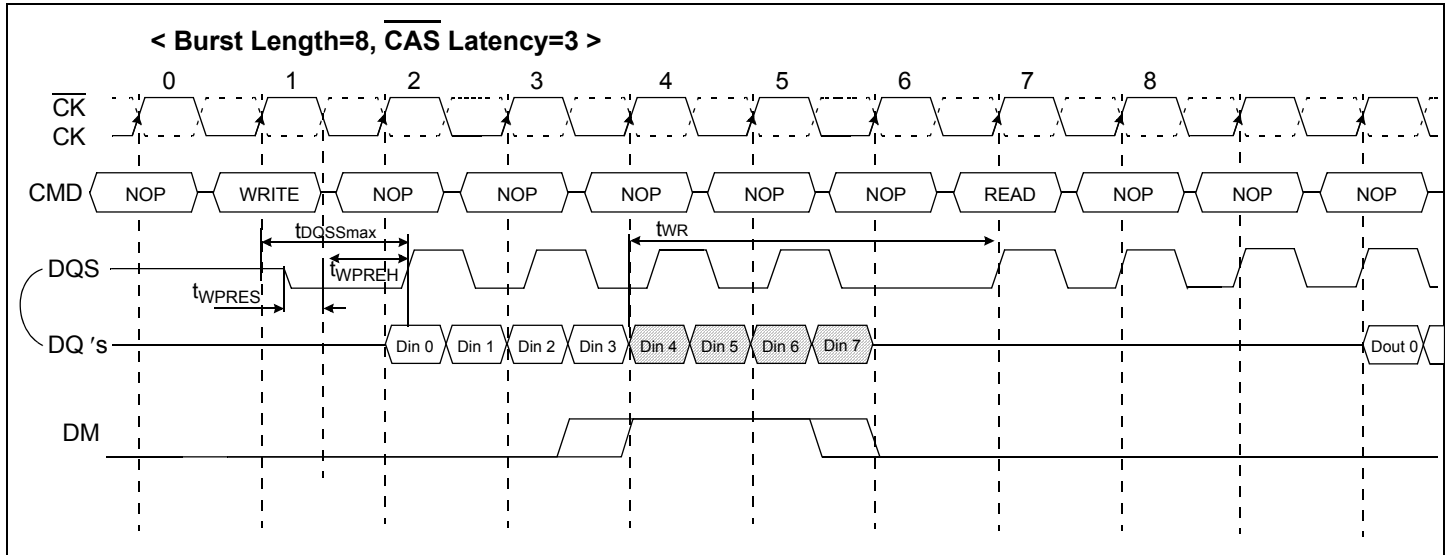
The extended mode register stores the data for enabling or disabling DLL and selecting output driver strength. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on CS, RAS, CAS, WE and high on BA0(The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0, A2 ~ A5, A7 ~ A11 and BA1 in the same cycle as CS, RAS, CAS and WE going low are written in the extended mode register. A1 and A6 are used for setting driver strength to normal, weak or matched impedance. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. "High" on BA0 is used for EMRS. All the other address pins except A0,A1,A6 and BA0 must be set to low for proper EMRS operation. Refer to the table for specific codes.



*1 : RFU(Reserved for future use) should stay "0" during EMRS cycle.

7.4 WRITE INTERRUPTED BY A READ

A burst write can be interrupted by a read command of any bank. The DQ's must be in the high impedance state at least one clock cycle before the interrupting read data appear on the outputs to avoid data contention. When the read command is registered, any residual data from the burst write cycle must be masked by DM. The delay from the last data to read command (tCDLR) is required to avoid the data contention DRAM inside. Data that are presented on the DQ pins before the read command is initiated will actually be written to the memory. Read command interrupting write can not be issued at the next clock edge of that of write command.



- The following function established how a Read command may interrupt a Write burst and which input data is not written into the memory.
1. For Read commands interrupting a Write burst, the minimum Write to Read command delay is 2 clock cycles. The case where the Write to Read delay is 1 clock cycle is disallowed
 2. For Read commands interrupting a Write burst, the DM pin must be used to mask the input data words which immediately precede the interrupting Read operation and the input data word which immediately follows the interrupting Read operation
 3. For all cases of a Read interrupting a Write, the DQ and DQS buses must be released by the driving chip (i.e., the memory controller) in time to allow the buses to turn around before the DDR SDRAM drives them during a read operation.
 4. If input Write data is masked by the Read command, the DQS input is ignored by the DDR SDRAM.
 5. Refer to "3.3.2 Burst write operation"

8.0 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 ~ 3.6	V
Voltage on VDD supply relative to Vss	V _{DD}	-1.0 ~ 3.6	V
Voltage on VDDQ supply relative to Vss	V _{DDQ}	-0.5 ~ 3.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	2.0	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

9.0 AC & DC OPERATING CONDITIONS

9.1 POWER & DC OPERATING CONDITIONS(SSTL_2 In/Out)

Recommended operating conditions(Voltage referenced to V_{SS}=0V, T_A=0 to 65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Device Supply voltage	V _{DD}	2.375	2.50	2.625	V	1, 7
Output Supply voltage	V _{DDQ}	2.375	2.50	2.625	V	1, 7
Reference voltage	V _{REF}	0.49*V _{DDQ}	-	0.51*V _{DDQ}	V	2
Termination voltage	V _{tt}	V _{REF} -0.04	V _{REF}	V _{REF} +0.04	V	3
Input logic high voltage	V _{IH}	V _{REF} +0.15	-	V _{DDQ} +0.30	V	4
Input logic low voltage	V _{IL}	-0.30	-	V _{REF} -0.15	V	5
Output logic high voltage	V _{OH}	V _{tt} +0.76	-	-	V	I _{OH} =-15.2mA
Output logic low voltage	V _{OL}	-	-	V _{tt} -0.76	V	I _{OL} =+15.2mA
Input leakage current	I _{IL}	-5	-	5	uA	6
Output leakage current	I _{OL}	-5	-	5	uA	6

Note :

- Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
- V_{REF} is expected to equal 0.50*V_{DDQ} of the transmitting device and to track variations in the DC level of the same. Peak to peak noise on the V_{REF} may not exceed + 2% of the DC value. Thus, from 0.50*V_{DDQ}, V_{REF} is allowed + 25mV for DC error and an additional + 25mV for AC noise.
- V_{tt} of the transmitting device must track V_{REF} of the receiving device.
- V_{IH}(max.)= V_{DDQ} +1.5V for a pulse width and it can not be greater than 1/3 of the cycle rate.
- V_{IL}(min.)= -1.5V for a pulse width and it can not be greater than 1/3 of the cycle rate.
- For any pin under test input of 0V ≤ V_{IN} ≤ V_{DD} is acceptable. For all other pins that are not under test V_{IN}=0V.
- For K4D261638I-LC50, V_{DD} & V_{DDQ} = 2.375V to 2.7V.

9.2 DC CHARACTERISTICS

Recommended operating conditions Unless Otherwise Noted (T_A=0 to 65°C)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-40	-50		
Operating Current (One Bank Active)	I _{CC1}	Burst Lenth=2 t _{RC} ≥ t _{RC} (min) I _{OL} =0mA, t _{CC} = t _{CC} (min)	200	180	mA	1, 2
Precharge Standby Current in Power-down mode	I _{CC2P}	CKE ≤ V _{IL} (max), t _{CC} = t _{CC} (min)	45	40	mA	1, 2
Precharge Standby Current in Non Power-down mode	I _{CC2N}	CKE ≥ V _{IH} (min), $\overline{CS} \geq V_{IH}(\min)$, t _{CC} = t _{CC} (min).	70	60	mA	1, 2
Active Standby Current power-down mode	I _{CC3P}	CKE ≤ V _{IL} (max), t _{CC} = t _{CC} (min)	85	70	mA	1, 2
Active Standby Current in in Non Power-down mode	I _{CC3N}	CKE ≥ V _{IH} (min), $\overline{CS} \geq V_{IH}(\min)$, t _{CC} = t _{CC} (min) .	135	110	mA	1, 2
Operating Current (Burst Mode)	I _{CC4}	I _{OL} =0mA ,t _{CC} = t _{CC} (min), Page Burst, All Banks activated.	390	345	mA	1, 2
Refresh Current	I _{CC5}	t _{RC} ≥ t _{RFC} (min)	200	180	mA	1, 2,3
Self Refresh Current	I _{CC6}	CKE ≤ 0.2V	10	10	mA	1, 2

Note :

- Measured with output open.
- Current measured at V_{DD}(max).
- Refresh period is 32ms.

9.3 AC INPUT OPERATING CONDITIONS

Recommended operating conditions(Voltage referenced to V_{SS}=0V, V_{DD}=2.5V± 5%, V_{DDQ}=2.5V± 5%, T_A=0 to 65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Input High (Logic 1) Voltage; DQ	V _{IH}	V _{REF} +0.35	-	-	V	
Input Low (Logic 0) Voltage; DQ	V _{IL}	-	-	V _{REF} -0.35	V	
Clock Input Differential Voltage; CK and \overline{CK}	V _{ID}	0.7	-	V _{DDQ} +0.6	V	1
Clock Input Crossing Point Voltage; CK and \overline{CK}	V _{IX}	0.5*V _{DDQ} -0.2	-	0.5*V _{DDQ} +0.2	V	2

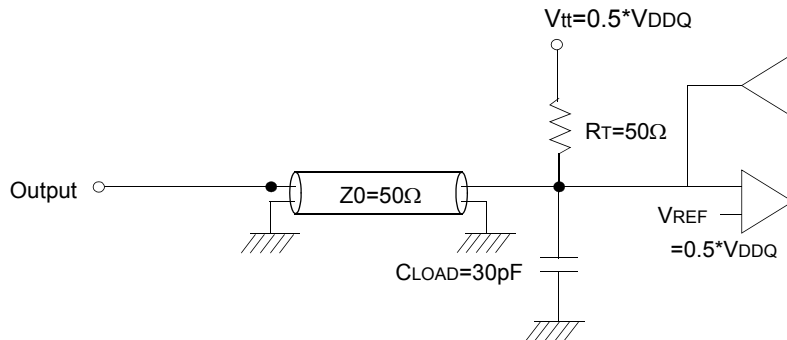
- Note :
1. V_{ID} is the magnitude of the difference between the input level on CK and the input level on \overline{CK} .
 2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.
 3. For K4D261638I-LC50, V_{DD} & V_{DDQ} = 2.375V to 2.7V.

9.4 AC OPERATING TEST CONDITIONS

(V_{DD}=2.5V± 5%^{*2}, T_A= 0 to 65°C)

Parameter	Value	Unit	Note
Input reference voltage for CK(for single ended)	0.50*V _{DDQ}	V	1
CK and \overline{CK} signal maximum peak swing	1.5	V	
CK signal minimum slew rate	1.0	V/ns	
Input Levels(V _{IH} /V _{IL})	V _{REF} +0.35/V _{REF} -0.35	V	
Input timing measurement reference level	V _{REF}	V	
Output timing measurement reference level	V _{tt}	V	
Output load condition	See Fig.1		

- Note :
1. In case of differential clocks(CK and \overline{CK}), input reference voltage for clock is a CK and \overline{CK} 's crossing point.
 2. For K4D261638I-LC50, V_{DD} & V_{DDQ} = 2.375V to 2.7V.



(Fig. 1) Output Load Circuit

9.5 CAPACITANCE

(VDD=2.5V, TA= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance(CK, \overline{CK})	CIN1	1.0	5.0	pF
Input capacitance(A0~A11, BA0~BA1)	CIN2	1.0	4.0	pF
Input capacitance(CKE, \overline{CS} , \overline{RAS} , \overline{CAS} , \overline{WE})	CIN3	1.0	4.0	pF
Data & DQS input/output capacitance(DQ0~DQ15)	COUT	1.0	6.5	pF
Input capacitance(DM0 ~ DM3)	CIN4	1.0	6.5	pF

DECOUPLING CAPACITANCE GUIDE LINE

Recommended decoupling capacitance added to power line at board.

Parameter	Symbol	Value	Unit
Decoupling Capacitance between VDD and VSS	CDC1	0.1 + 0.01	uF
Decoupling Capacitance between VDDQ and VSSQ	CDC2	0.1 + 0.01	uF

1. VDD and VDDQ pins are separated each other. All VDD pins are connected in chip. All VDDQ pins are connected in chip.
2. VSS and VSSQ pins are separated each other. All VSS pins are connected in chip. All VSSQ pins are connected in chip.

9.6 AC CHARACTERISTICS

Parameter	Symbol	-40		-50		Unit	Note	
		Min	Max	Min	Max			
CK cycle time	CL=2	tCK	7.5	10	7.5	10	ns	
	CL=3	tCK	4.0	10	5.0	10	ns	
CK high level width	tCH	0.45	0.55	0.45	0.55	tCK		
CK low level width	tCL	0.45	0.55	0.45	0.55	tCK		
DQS out access time from CK	tDQSCK	-0.6	0.6	-0.7	0.7	ns		
Output access time from CK	tAC	-0.6	0.6	-0.7	0.7	ns		
Data strobe edge to Dout edge	tDQSQ	-	0.4	-	0.45	ns	1	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK		
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK		
CK to valid DQS-in	tDQSS	0.85	1.15	0.8	1.2	tCK		
DQS-In setup time	tWPRES	0	-	0	-	ns		
DQS-in hold time	tWPREH	0.35	-	0.3	-	tCK		
DQS write postamble	tWPST	0.4	0.6	0.4	0.6	tCK		
DQS-In high level width	tDQSH	0.4	0.6	0.4	0.6	tCK		
DQS-In low level width	tDQSL	0.4	0.6	0.4	0.6	tCK		
Address and Control input setup	tIS	0.9	-	1.0	-	ns		
Address and Control input hold	tIH	0.9	-	1.0	-	ns		
DQ and DM setup time to DQS	tDS	0.4	-	0.45	-	ns		
DQ and DM hold time to DQS	tDH	0.4	-	0.45	-	ns		
Clock half period	tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	1	
Data output hold time from DQS	tQH	tHP-0.4	-	tHP-0.45	-	ns	1	

Note 1 :

- The JEDEC DDR specification currently defines the output data valid window(tDV) as the time period when the data strobe and all data associated with that data strobe are coincidentally valid.
- The previously used definition of tDV(=0.35tCK) artificially penalizes system timing budgets by assuming the worst case output valid window even then the clock duty cycle applied to the device is better than 45/55%
- A new AC timing term, tQH which stands for data output hold time from DQS is defined to account for clock duty cycle variation and replaces tDV
- tQHmin = tHP-X where
 - . tHP=Minimum half clock period for any given cycle and is defined by clock high or clock low time(tCH,tCL)
 - . X=A frequency dependent timing allowance account for tDQSQmax

AC CHARACTERISTICS (II)_Continued

Parameter	Symbol	-40		-50		Unit	Note
		Min	Max	Min	Max		
Row cycle time	tRC	52	-	55	-	ns	
Refresh row cycle time	tRFC	60	-	70		ns	
Row active time	tRAS	36	100K	40	100K	ns	
RAS to CAS delay for Read	tRCDRD	16	-	15	-	ns	
RAS to CAS delay for Write	tRCDWR	8	-	10	-	ns	2
Row precharge time	tRP	16	-	15	-	ns	
Row active to Row active	tRRD	12	-	10		ns	
Last data in to Row precharge @Normal Precharge	tWR	3	-	3	-	tCK	1
Last data in to Row precharge @Auto Precharge	tWR_A	3	-	3	-	tCK	1
Last data in to Read command	tCDLR	2	-	2	-	tCK	1
Col. address to Col. address	tCCD	1	-	1	-	tCK	
Mode register set cycle time	tMRD	2	-	2	-	tCK	
Auto precharge write recovery + Precharge	tDAL	7	-	6	-	tCK	
Exit self refresh to read command	tXSR	200	-	200	-	tCK	
Power down exit time	tPDEX	3tCK+tIS	-	3tCK+tIS	-	ns	
Refresh interval time	tREF	-	7.8	-	7.8	us	

Note :

1. For normal write operation, even numbers of Din are to be written inside DRAM.
2. tRCDWR should be always greater or equal to 2tCK.

AC CHARACTERISTICS (III)_Continued

(Unit : Number of Clock)

K4D261638F-LC40

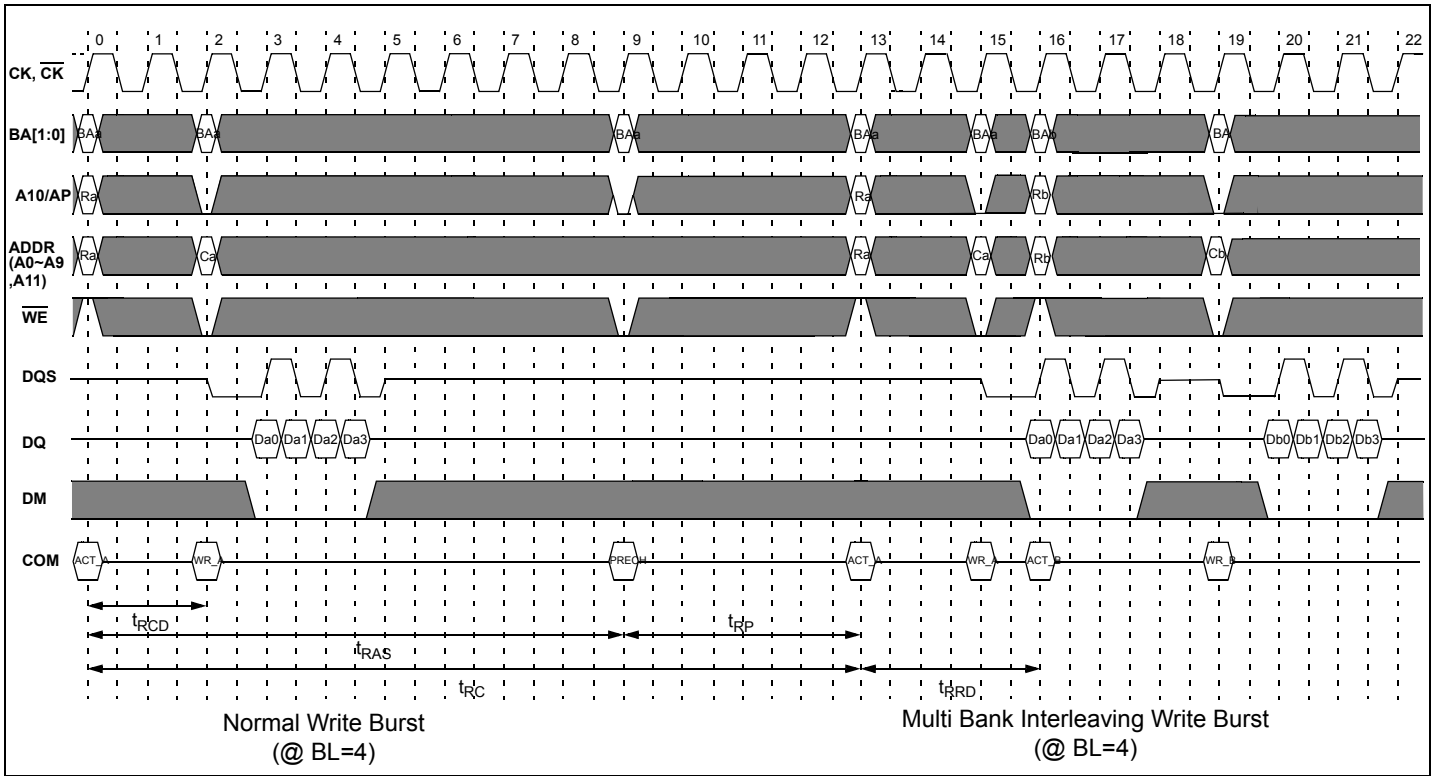
Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	tDAL	Unit
250MHz (4.0ns)	3	13	15	9	4	2	4	3	7	tCK
200MHz (5.0ns)	3	11	14	8	3	2	3	2	6	tCK
133MHz (7.5ns)	3 or 2	7	8	5	3	2	3	2	4	tCK

K4D261638F-LC50

Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	tDAL	Unit
200MHz (5.0ns)	3	11	14	8	3	2	3	2	6	tCK
133MHz (7.5ns)	3 or 2	8	10	6	2	2	2	2	4	tCK

10.0 SIMPLIFIED TIMING

Simplified Timing @ BL=4



11.0 IBIS : I/V Characteristics for Input and Output Buffers

(1) Full Strength Driver Characteristics

Voltage (V)	Pulldown Current (mA)		Pullup Current (mA)	
	Minimum	Maximum	Minimum	Maximum
0.0	0	0	0	0
0.1	1.368	1.716	-0.9	-0.924
0.2	4.968	6.996	-4.536	-6.424
0.3	8.46	12.32	-7.92	-11.572
0.4	11.808	17.512	-11.196	-16.588
0.5	14.904	22.616	-14.328	-21.472
0.6	17.892	27.544	-17.208	-26.136
0.7	20.376	32.12	-19.908	-30.756
0.8	22.716	36.564	-22.428	-35.024
0.9	24.624	40.612	-24.732	-39.204
1.0	26.208	44.176	-26.748	-42.988
1.1	27.432	47.388	-28.476	-46.508
1.2	28.224	50.028	-29.952	-49.808
1.3	28.836	52.184	-31.176	-52.668
1.4	29.268	53.812	-32.22	-55.22
1.5	29.592	55	-33.048	-57.464
1.6	29.808	55.88	-33.696	-59.356
1.7	29.988	56.54	-34.308	-60.896
1.8	30.168	56.98	-34.812	-62.172
1.9	30.348	57.332	-35.244	-63.272
2.0	30.456	57.64	-35.64	-64.24
2.1	30.564	57.86	-36	-65.032
2.2	30.708	58.08	-36.288	-65.736
2.3	30.78	58.256	-36.576	-66.352
2.4	30.807	58.388	-36.648	-66.924
2.5	30.879	58.52	-36.747	-67.452
2.6	30.924	58.652	-36.72	-67.936
2.7	30.969	58.784	-36.72	-68.332

11.0 IBIS : I/V Characteristics for Input and Output Buffers

(2) Weak Strength Driver Characteristics

Voltage (V)	Pulldown Current (mA)		Pullup Current (mA)	
	Minimum	Maximum	Minimum	Maximum
0.0	0	0	0	0
0.1	1.332	1.716	-1.08	-1.144
0.2	4.752	6.776	-4.212	-5.94
0.3	7.992	11.704	-2.272	-10.56
0.4	11.008	16.456	-10.152	-15.092
0.5	13.968	21.076	-12.96	-19.36
0.6	16.74	25.784	-15.48	-23.496
0.7	19.08	30.052	-17.856	-27.588
0.8	21.24	34.144	-20.052	-31.284
0.9	23.04	37.884	-21.996	-35.024
1.0	24.516	41.404	-23.832	-38.368
1.1	25.596	44.308	-25.308	-41.492
1.2	26.388	46.772	-26.64	-44.352
1.3	26.964	48.664	-27.684	-46.816
1.4	27.36	50.248	-28.548	-49.06
1.5	27.648	51.348	-29.232	-50.864
1.6	27.828	52.14	-29.844	-52.448
1.7	28.008	52.756	-30.312	-53.812
1.8	28.188	53.196	-30.78	-54.956
1.9	28.296	53.196	-31.14	-55.88
2.0	28.44	53.768	-31.464	-56.672
2.1	28.548	53.988	-31.752	-57.376
2.2	28.62	54.164	-32.04	-57.992
2.3	28.728	54.296	-32.157	-58.476
2.4	28.8	54.472	-32.328	-59.004
2.5	28.908	54.604	-32.418	-59.444
2.6	28.953	54.692	-32.472	-59.84
2.7	28.998	54.824	-32.508	-60.28

11.0 IBIS : I/V Characteristics for Input and Output Buffers

(3) Matched Strength Driver Characteristics

Voltage (V)	Pulldown Current (mA)		Pullup Current (mA)	
	Minimum	Maximum	Minimum	Maximum
0.0	0	0	0	0
0.1	1.152	1.452	-0.972	-1.276
0.2	2.988	4.312	-2.916	-4.224
0.3	4.788	7.084	-4.824	-7.04
0.4	6.48	9.724	-6.516	-9.768
0.5	8.028	12.232	-8.172	-12.364
0.6	9.396	14.74	-9.756	-14.872
0.7	10.692	16.984	-11.16	-17.292
0.8	11.7	19.184	-12.42	-19.624
0.9	12.564	21.164	-13.572	-21.736
1.0	13.248	22.792	-14.544	-23.672
1.1	13.716	24.2	-15.372	-25.476
1.2	14.04	25.256	-16.056	-27.06
1.3	14.292	26.136	-16.632	-28.468
1.4	14.472	26.752	-17.1	-29.656
1.5	14.616	27.148	-17.496	-30.668
1.6	14.724	27.544	-17.82	-31.504
1.7	14.796	27.764	-18.108	-32.208
1.8	14.868	27.984	-18.324	-32.78
1.9	14.94	28.116	-18.54	-33.264
2.0	14.976	28.204	-18.756	-33.66
2.1	15.048	28.336	-18.9	-34.056
2.2	15.12	28.38	-19.08	-34.408
2.3	15.192	28.512	-19.224	-34.716
2.4	15.228	28.6	-19.332	-34.716
2.5	15.264	28.644	-19.431	-35.2
2.6	15.3	28.732	-19.611	-35.42
2.7	15.372	28.776	-19.692	-35.64

12.0 PACKAGE DIMENSIONS (66pin TSOP-II)

