

J308 SERIES

N-Channel JFETs

The J308 Series is a popular, low-cost device which offers superb amplification characteristics. It features high-gain, low noise (typically $< 6\text{ nV}\sqrt{\text{Hz}}$) and low gate leakage (typically $< 2\text{ pA}$). Of special interest, however, is performance at high frequency. Even at 450 MHz the J308 Series offers high power gain and low noise. Like all TO-92 packages offered by Siliconix, tape and reel options are available to support automated assembly. (See Section 7.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
J308	-6.5	-25	8	60
J309	-4.0	-25	8	30
J310	-6.5	-25	8	60

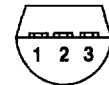
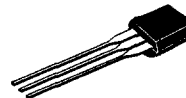
For additional design information and a closer look at high-frequency characteristics, please consult performance curves NZB.

SIMILAR PRODUCTS

- TO-52, See U309 Series
- SOT-23, See SST308 Series
- Dual, See U430 Series
- Chips, See NZB Series Die

TO-92 (TO-226AA)

BOTTOM VIEW



- 1 DRAIN
- 2 SOURCE
- 3 GATE

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	10	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/ $^\circ\text{C}$
Operating Junction Temperature Range	T_J	-55 to 135	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($1/16"$ from case for 10 sec.)	T_L	300	

SPECIFICATIONS ^a				LIMITS							
PARAMETER	SYMBOL	TEST CONDITIONS	TYP ^b	J308		J309		J310		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX		
STATIC											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = -1 \mu A, V_{DS} = 0 V$	-35	-25		-25		-25		V	
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	$V_{DS} = 10 V, I_D = 1 nA$		-1	-6.5	-1	-4	-2	-6.5		
Saturation Drain Current ^c	I_{DSS}	$V_{DS} = 10 V, V_{GS} = 0 V$		12	60	12	30	24	60	mA	
Gate Reverse Current	I_{GSS}	$V_{GS} = -15 V, V_{DS} = 0 V$ $T_A = 125^\circ C$	-0.002		-1		-1		-1	nA	
					-1		-1		-1	μA	
Gate Operating Current	I_G	$V_{DG} = 9 V, I_D = 10 mA$	-15							pA	
Drain Cutoff Current	$I_{DS(ON)}$	$V_{GS} = 0 V, I_D = 1 mA$	35							Ω	
Gate-Source Forward Voltage	$V_{GS(F)}$	$I_G = 1 mA, V_{DS} = 0 V$	0.7		1		1		1	V	
DYNAMIC											
Common-Source Forward Transconductance	g_{fs}	$V_{DS} = 10 V, I_D = 10 mA$ $f = 1 kHz$	14	8		10		8		mS	
Common-Source Output Conductance	g_{os}			110		250		250		250	μS
Common-Source Input Capacitance	C_{iss}	$V_{DS} = 10 V, V_{GS} = -10 V$ $f = 1 MHz$	4		5		5		5	pF	
Common-Source Reverse Transfer Capacitance	C_{rss}			1.9		2.5		2.5			2.5
Equivalent Input Noise Voltage	\bar{e}_n	$V_{DS} = 10 V, I_D = 10 mA$ $f = 100 Hz$	6							nV/\sqrt{Hz}	
HIGH FREQUENCY											
Common-Gate Forward Transconductance	g_{fg}	$V_{DS} = 10 V$ $I_D = 10 mA$	$f = 105 MHz$	15						mS	
			$f = 450 MHz$	13							
Common-Gate Output Conductance	g_{og}		$f = 105 MHz$	0.16							dB
			$f = 450 MHz$	0.55							
Common-Gate Power Gain ^d	G_{pg}		$f = 105 MHz$	16							
			$f = 450 MHz$	11.5							
Noise Figure	NF		$f = 105 MHz$	1.5							
			$f = 450 MHz$	2.7							

NOTES:

- a. $T_A = 25^\circ C$ unless otherwise noted.
- b. For design aid only, not subject to production testing.
- c. Pulse test; $PW = 300 \mu S$, duty cycle $\leq 3\%$.
- d. Gain (G_{pg}) measured at optimum input noise match.