XRD4461/XRD44L61
XRD4462/XRD44L62

CCD Image Digitizer with Programmable Gain & Stand-by Mode

EXAR

FEATURES

- 10-Bit resolution ADC
- 18 MHz Sampling Rate
- Correlated Double Sampler (CDS)
- Digital Black Level Auto-Calibration
- Programmable Gain from 6dB to 38dB (PGA)
- Single 5V or 3.0V Power Supply
- Low Power for Battery Powered Operation:

  250mW @ V_{DD}=5V (XRD4461/XRD4462)

  120mW @ V_{DD}=3V (XRD44L61/XRD44L62)
- Stand By Mode (less than 50μA)
- XRD4461 & XRD44L61 sample on falling edge of clocks
- XRD4462 & XRD44L62 sample on rising edge of clocks
- 3-State Digital Outputs
- ESD Protection to over 4000V
- 32 pin TQFP Package
- 3 Wire Serial Interface

APPLICATIONS

- Video Camcorder
- Digital Still Cameras
- PC Video Teleconferencing
- Digital Copiers
- Infrared Image Digitizers
- CCD/CIS Imager Interface

ALSO SEE

- XRD4460/XRD44L60: More Features
- XRD4461/62EVAL: Evaluation System User Manual

GENERAL DESCRIPTION

The XRD4461 and XRD4462 are complete CCD Image Digitizers for digital cameras. These products include a high bandwidth, differential Correlated Double Sampler (CDS), an 8-bit digitally Programmable Gain Amplifier (PGA), a 10-bit Analog-to-Digital Converter (ADC), and automatic black level calibration circuitry.

The Correlated Double Sampler (CDS) subtracts the CCD output black level from the video level. Common mode noise and power supply noise are rejected by the differential CDS input stage. The CDS inputs can be used either differentially or single ended.

The PGA is digitally controlled with 8-bit resolution on a linear dB scale, resulting in a gain range from 6dB to 38dB with 0.125dB per LSB of the Gain code.

The PGA and black level calibration are controlled through a simple 3-wire serial interface. The timing circuitry is designed to be compatible with a wide variety of available CCD image sensors.

The XRD4461/XRD44L61 and XRD4462/XRD44L62 are packaged in 32-lead surface mount TQFP to reduce space and weight, and are suitable for hand-held and portable applications.

ORDERING INFORMATION

Part No.	Power Supply	Package	Operating Temperature Range
XRD4461DIQ	5.0V	32-Lead TQFP (7 X 7 X 1.4mm)	-40°C to 85°C
XRD44L61DIQ	3.0V	32-Lead TQFP (7 X 7 X 1.4mm)	-40°C to 85°C
XRD4462DIQ	5.0V	32-Lead TQFP (7 X 7 X 1.4mm)	-40°C to 85°C
XRD44L62DIQ	3.0V	32-Lead TQFP (7 X 7 X 1.4mm)	-40°C to 85°C

BLOCK DIAGRAM

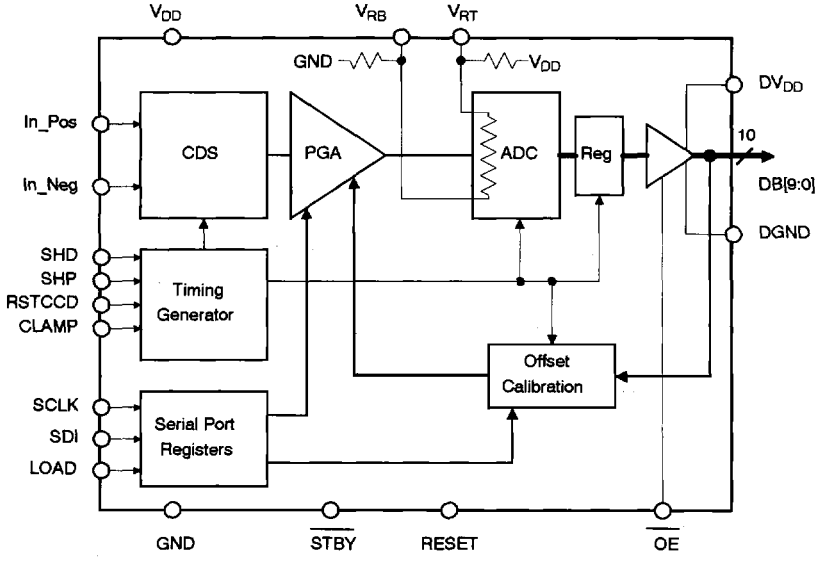

Figure 1. Simplified Block Diagram of the XRD4461 & XRD4462

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	DB2	Dout	**ADC Output.**
2	DB3	Dout	**ADC Output.**
3	DB4	Dout	**ADC Output.**
4	DGND	Ground	**Digital Output Ground.**
5	DV_{DD}	Power	**Digital Output Power Supply.**
6	DB5	Dout	**ADC Output.**
7	DB6	Dout	**ADC Output.**
8	DB7	Dout	**ADC Output.**
9	DB8	Dout	**ADC Output.**
10	DB9	Dout	**ADC Output (MSB).**
11	$\overline{OE}$	Din	**Digital Output 3-State Control.** Pull Low to enable digital output drivers
12	V_{DD}	Power	**Analog Power Supply.**
13	GND	Ground	**Analog Ground.**
14	$\overline{STBY}$	Din	**Stand By Control.** Pull Low to put chip in power down mode.
15	RESET	Din	**Chip Reset.** When reset goes high all internal control registers are set to power up default values. Gain register is set to code 00h (minimum gain). Offset code is set to 08h. Calibration circuit is cleared to uncalibrated state.
16	SCLK	Din	**Shift Clock for Serial Register.** Serial register latches SDI data on the rising edges of SCLK. When LOAD is high SCLK is internally disabled.
17	LOAD	Din	**Data Load.** Rising edge loads data from serial input register to gain or offset register. Load must be low to enable shift register to read data from SDI
18	SDI	Din	**Data Input for Serial Register.**
19	V_{RT}	Analog	**ADC Top Reference.** Internally set to $V_{DD}/1.3$.
20	V_{DD}	Power	**Analog Power Supply.**
21	In_Neg	Analog	**CDS Inverting Input.** Connect via capacitor to CCD video output.
22	In_Pos	Analog	**CDS Non-Inverting Input.** Connect via capacitor to CCD ground or black reference.
23	GND	Ground	**Analog Ground.**
24	V_{RB}	Analog	**ADC Bottom Reference.** Internally set to $V_{DD}/10$.
25	CLAMP	Din	**Black Level Clamp Control.** XRD4461 & XRD44L61 Active High. XRD4462 & XRD44L62 Active low.
26	SHD	Din	**Pixel Video Level Clock.** XRD4461 & XRD44L61 Samples on Falling Edge. XRD4462 & XRD44L62 Samples on rising edge.
27	SHP	Din	**Pixel Black Level Clock.** XRD4461 & XRD44L61 Samples on Falling Edge. XRD4462 & XRD44L62 Samples on rising edge.
28	RSTCCD	Din	**CCD Reset Pulse** . Used to decouple CDS during the reset pulse for noise reduction.
29	GND	Ground	**Analog Ground.**
30	V_{DD}	Power	**Analog Power Supply.**
31	DB0	Dout	**ADC Output (LSB).**
32	DB1	Dout	**ADC Output.**

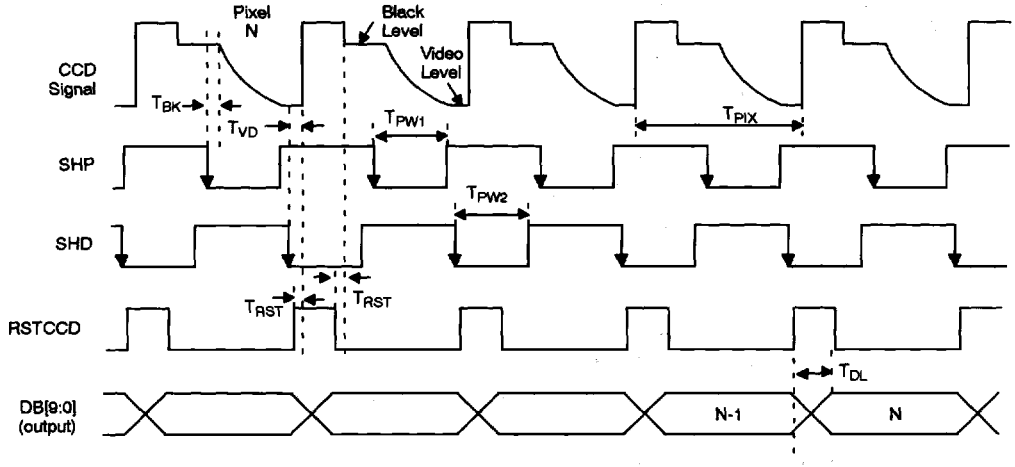

Figure 2. Conversion Timing Diagram for XRD4461 & XRD44L61.

Event	Action
↑RSTCCD	Disconnect CDS Inputs from Reset Noise
↓RSTCCD	Connect CDS Inputs and Track Black Level
↓SHP	Hold Black Level and Track Video Level
↓SHD	Hold Video Level
↑SHP/SHD	No Action
CLAMP High	Force ADC Output Code to Equal Offset Code

Table 1. Timing Event Description for XRD4461 & XRD44L61

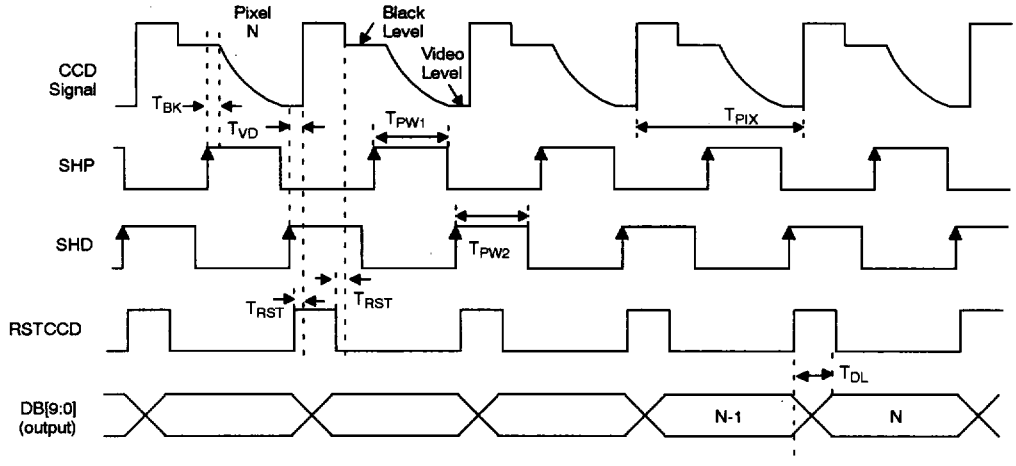

Figure 3. Conversion Timing Diagram for XRD4462 & XRD44L62.

Event	Action
↑RSTCCD	Disconnect CDS Inputs from Reset Noise
↓RSTCCD	Connect CDS Inputs and Track Black Level
↑SHP	Hold Black Level and Track Video Level
↑SHD	Hold Video Level
↓SHP/SHD	No Action
CLAMP Low	Force ADC Output Code to Equal Offset Code

Table 2. Timing Event Description for XRD4462 & XRD44L62

DC ELECTRICAL CHARACTERISTICS - XRD4461 & XRD4462
Test Conditions: Unless otherwise specified: $DV_{DD} = V_{DD} = 5.0V$, Pixel Rate = 16MSPS, $V_{RT} = 3.8V$, $V_{RB} = 0.5V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CDS Performance						
$CDSV_{IN}$	Input Range		200	800	mV_{PP}	Pixel (black level - video level).
BW	Small Signal Bandwidth (-3dB)		60		MHz	
SR	Slew Rate		40		V/µs	400mV step input.
FT	Feed-through (Hold Mode)		-60		dB	
PGA Parameters						
AV_{MIN}	Minimum Gain		6		dB	
AV_{MAX}	Maximum Gain		38		dB	
PGA n	Resolution		8		bits	Transfer function is linear steps in dB (1LSB = 0.125dB).
GE	Gain Error		5		% FS	At maximum or minimum gain setting.
ADC Parameters (Measured Through TESTVIN)						
ADC n	Resolution	10			bits	
f_s	Max Sample Rate	16			MSPS	
V_{RB}	Self Bias V_{RB} $\left(V_{RB} = \frac{V_{DD}}{10}\right)$		0.5		V	
V_{RT}	Self Bias V_{RT} $\left(V_{RT} = \frac{V_{DD}}{1.30}\right)$		3.8		V	
System Specifications						
DNL_{SMIN}	DNL @ Minimum Gain		0.75		LSB	
DNL_{SMAX}	DNL @ Maximum Gain		0.75		LSB	
INL_{SMIN}	INL @ Minimum Gain		2		LSB	INL error is dominated by CDS/ PGA linearity.
INL_{SMAX}	INL @ Maximum Gain		2		LSB	INL error is dominated by CDS/ PGA linearity.
$V_{OS\ MINAV}$	Offset (Input Referred) @ Minimum Gain		5		mV	Offset is defined as the input pixel value-0.5 LSB required to cause the ADC output to switch from "Zero scale" to "Zero scale + 1LSB". Offset is measured after calibration.
$V_{OS\ MAXAV}$	Offset (Input Referred) @ Maximum Gain		1		mV	Zero scale is the code in the offset register. Offset depends on PGA gain code.

DC ELECTRICAL CHARACTERISTICS - XRD4461 & XRD4462 (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
System Specifications (Cont'd)						
en_{MAXAV}	Input Referred Noise @ Maximum Gain		0.2		mV_{rms}	Noise depends upon gain setting of the PGA.
en_{MINAV}	Input Referred Noise @ Minimum Gain		3.5		mV_{rms}	Noise depends upon gain setting of the PGA.
Digital Inputs						
V_{IH}	Digital Input High Voltage	3.5			V	
V_{IL}	Digital Input Low Voltage			1.5	V	
I_L	DC Leakage Current		5		µA	Input between GND and V_{DD}.
C_{IN}	Input Capacitance		5		pF	
Digital Outputs						
V_{OH}	Digital Output High Voltage	V_{DD}-0.5			V	While sourcing 2mA.
V_{OL}	Digital Output Low Voltage			0.5	V	While sinking 2mA.
I_{OZ}	High-Z Leakage	-10		10	µA	$\overline{OE}$=1 or $\overline{STBY}$= 0. Output between GND & DV_{DD}.
Digital I/O Timing						
T_{DL}	Data Valid Delay		20	25	ns	
T_{PW1}	Pulse Width of SHD	15			ns	
T_{PW2}	Pulse Width of SHD	15			ns	
T_{PIX}	Pixel Period	62			ns	
T_{BK}	Sample Black Aperture Delay		4	6	ns	V_{DD} = 4.5V to 5.5V, Temperature -40°C to 85°C range
T_{VD}	Sample Video Aperture Delay		3	5	ns	V_{DD} = 4.5V to 5.5V, Temperature -40°C to 85°C range
T_{RST}	RSTCCD Switch Delay	0		4	ns	V_{DD} = 4.5V to 5.5V, Temperature -40°C to 85°C range
T_{SC}	Shift Clock Period	40	70		ns	
T_{SET}	Shift Register Setup Time	10			ns	
Power Supplies						
V_{DD}	Analog Supply Voltage	4.5	5.0	5.5	V	
DV_{DD}	Digital Output Supply Voltage	2.7	5.0	5.5	V	$DV_{DD} \leq V_{DD}$ always
I_{DD}	Supply Current		50	70	mA	$DV_{DD} = V_{DD}$ = 5.0V
I_{DDPD}	Power Down Supply Current		50	100	µA	$\overline{STBY}$ = 0

DC ELECTRICAL CHARACTERISTICS - XRD44L61 & XRD44L62
Test Conditions: Unless otherwise specified: $DV_{DD} = V_{DD} = 2.7V$, Pixel Rate = 16MSPS, $V_{RT} = 2.07V$, $V_{RB} = 0.27V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CDS Performance						
$CDSV_{IN}$	Input Range		200	800	mV_{PP}	Pixel (black level - video level).
BW	Small Signal Bandwidth (-3dB)		60		MHz	
SR	Slew Rate		40		V/µs	400mV step input.
FT	Feed-through (Hold Mode)		-60		dB	
PGA Parameters						
AV_{MIN}	Minimum Gain		6		dB	
AV_{MAX}	Maximum Gain		38		dB	
PGA n	Resolution		8		bits	Transfer function is linear steps in dB (1LSB = 0.125dB).
GE	Gain Error		5		% FS	At maximum or minimum gain setting.
ADC Parameters (Measured Through TESTVIN)						
ADC n	Resolution	10			bits	
f_s	Max Sample Rate	16			MSPS	
V_{RB}	Self Bias V_{RB} $\left(V_{RB} = \frac{V_{DD}}{10}\right)$		0.27		V	
V_{RT}	Self Bias V_{RT} $\left(V_{RT} = \frac{V_{DD}}{1.30}\right)$		2.07		V	
System Specifications						
DNL_{SMIN}	DNL @ Minimum Gain		0.75		LSB	
DNL_{SMAX}	DNL @ Maximum Gain		0.75		LSB	
INL_{SMIN}	INL @ Minimum Gain		2		LSB	INL error is dominated by CDS/ PGA linearity.
INL_{SMAX}	INL @ Maximum Gain		2		LSB	INL error is dominated by CDS/ PGA linearity.
$V_{OS\ MINAV}$	Offset (Input Referred) @ Minimum Gain		5		mV	Offset is defined as the input pixel value-0.5 LSB required to cause the ADC output to switch from "Zero scale" to "Zero scale + 1LSB". Offset is measured after calibration.
$V_{OS\ MAXAV}$	Offset (Input Referred) @ Maximum Gain		1		mV	Zero scale is the code in the offset register. Offset depends on PGA gain code.
$en_{\ MAXAV}$	Input Referred Noise @ Maximum Gain		0.2		mV_{rms}	Noise depends upon gain setting of the PGA.

DC ELECTRICAL CHARACTERISTICS - XRD44L61 & XRD44L62 (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
System Specifications (Con't)						
en_{MINAV}	Input Referred Noise @ Minimum Gain		3.5		mV_{rms}	Noise depends upon gain setting of the PGA.
Digital Inputs						
V_{IH}	Digital Input High Voltage	2.0			V	
V_{IL}	Digital Input Low Voltage			0.8	V	
I_L	DC Leakage Current		5		µA	Input between GND and V_{DD}.
C_{IN}	Input Capacitance		5		pF	
Digital Outputs						
V_{OH}	Digital Output High Voltage	V_{DD}-0.5			V	While sourcing 2mA.
V_{OL}	Digital Output Low Voltage			0.5	V	While sinking 2mA.
I_{OZ}	High-Z Leakage	-10		10	µA	$\overline{OE}$=1 or $\overline{STBY}$ = 0. Output between GND & DV_{DD}.
Digital I/O Timing						
T_{DL}	Data Valid Delay		28	35	ns	
T_{PW1}	Pulse Width of SHD	15			ns	
T_{PW2}	Pulse Width of SHD	15			ns	
T_{PIX}	Pixel Period	62			ns	
T_{BK}	Sample Black Aperture Delay		5	7	ns	V_{DD} = 4.5V to 5.5V, Temperature -40°C to 85°C range
T_{VD}	Sample Video Aperture Delay		4	6	ns	V_{DD} = 4.5V to 5.5V, Temperature -40°C to 85°C range
T_{RST}	RSTCCD Switch Delay	0		5	ns	V_{DD} = 4.5V to 5.5V, Temperature -40°C to 85°C range
T_{SC}	Shift Clock Period	40	70		ns	
T_{SET}	Shift Register Setup Time	10			ns	
Power Supplies						
V_{DD}	Analog Supply Voltage	2.7	3.0	3.6	V	
DV_{DD}	Digital Output Supply Voltage	2.7	3.0	3.6	V	$DV_{DD} \leq V_{DD}$ always
I_{DD}	Supply Current		40	50	mA	$DV_{DD} = V_{DD}$ = 3.0 V
I_{DDPD}	Power Down Supply Current		50	100	µA	$\overline{STBY}$ = 0

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND	+7.0V
V_{RT} & V_{RB}	V_{DD} +0.5 to GND -0.5V
V_{IN}	V_{DD} +0.5 to GND -0.5V
All Inputs	V_{DD} +0.5 to GND -0.5V
All Outputs	V_{DD} +0.5 to GND -0.5V
Storage Temperature	-65°C to 150°C
Lead Temperature (Soldering 10 seconds)	300°C
Maximum Junction Temperature	150°C
Package Power Dissipation Ratings (T_A= +70°C)	
TQFP	θ_{JA} = 54°C/W
ESD	4000V

Notes:

1 *Stresses above those listed as "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.*

2 *Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.*

3 *V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.*

SYSTEM DESCRIPTION

Correlated Double Sample/Hold (CDS) & Programmable Gain Amplifier (PGA)

The function of the CDS block, shown in *Figure 4*, is to sense the voltage difference between the black level and the video level of each pixel. CCD2 (IN_POS) would typically be considered the "common" voltage of the CCD which may be ground or the CCD black reference. CCD1 (IN_NEG) would be the actual CCD video output signal. The internal bias voltage, V_{BIAS}, sets the DC voltage of the input pins In_Pos & In_Neg. The DC voltage is updated every line using the CLAMP control input. The clock signals SHP & SHD are used to generate the internal signals SDRK and SPIX. SDRK samples the pixel black level by clamping the PGA inputs to V_{DD} when the CCD outputs the pixel black level. When SDRK goes low, the pixel value is transmitted through the internal capacitors and converted into a fully differential signal ***va*** by differential amplifier PGA1 which also provides programmable gains of 2.5, 1, and 0.4. The gain is controlled by the two most significant bits of the 8-bit gain control code. SPIX is used to sample/hold the pixel value ***va*** so that the required bandwidth of the following circuit is reduced. In each coarse gain segment set by PGA1, the second programmable amplifier PGA2 provides fine gain control (each LSB adds 0.125dB). The combined gain of the two PGA blocks is controlled by the digital code in the gain register. The gain register is programmed through the serial port.

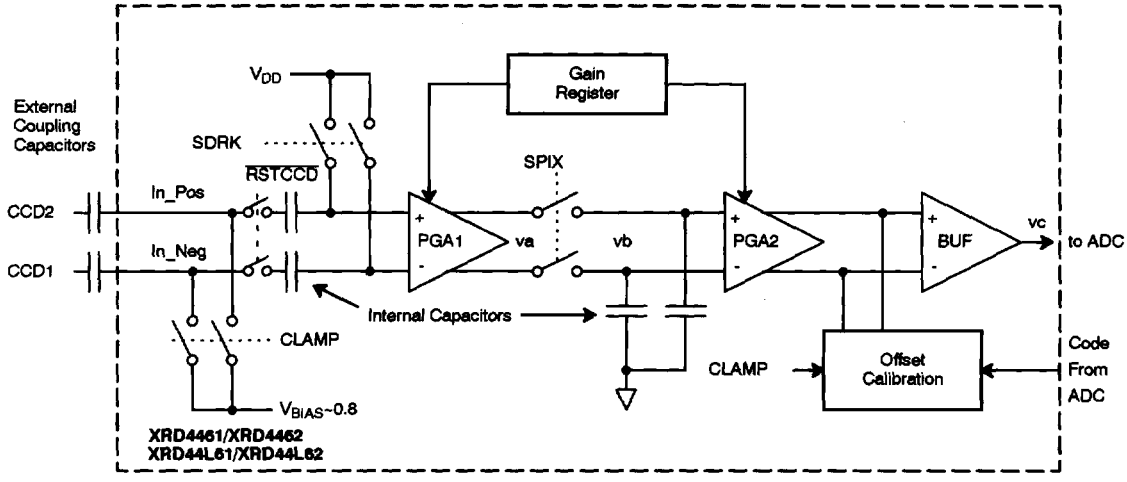

Figure 4. Block Diagram of the CDS

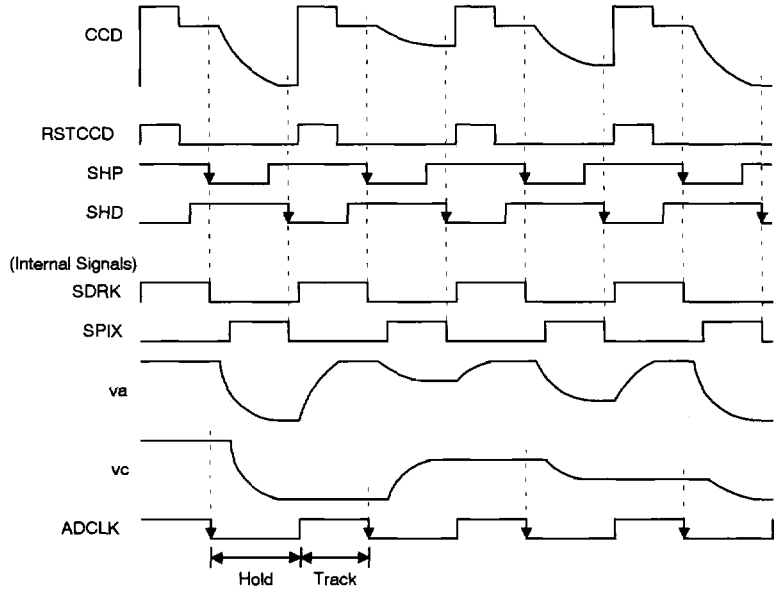

Figure 5. Timing Diagram of the CDS Clocks and Internal Signals (Shown with XRD4461/XRD44L61 Timing)

Figure 5 shows the wave forms of the control clocks and the output voltages at various nodes in the block diagram. On the XRD4461 & XRD44L61 the falling edge of SHP samples the black level while the falling edge of SHD samples the pixel value. On the XRD4462 & XRD44L62 the rising edge of SHP samples the black level while the rising edge of SHD samples the pixel value. The ADC samples the output ***vc*** before the rising edge of SPIX. Note that ***vb*** and ***vc*** will have the same waveform shape, but ***vc*** will be delayed relative to ***vb***, and will have a different amplitude depending upon the gain setting.

Figure 6 shows PGA gain vs. gain register code. The PGA provides a programmable gain range of 32dB. The minimum gain (code 00h) is 6dB $\pm$ 1dB. The maximum gain (code FFh) is 38dB $\pm$1dB. Ideally, the gain can be expressed by the following equation.

$$Gain[dB] = 6 + \left(32 \cdot \frac{code}{256}\right)$$

where code is between 0 and 255.

The gain is realized by two stages. The gain transfer function is split into three main segments. The first stage, PGA1, is controlled by two MSBs of the 8-bit gain code and selects one of the three gain segments. The second stage, PGA2, provides fine gain adjustment within each gain segment. One LSB of the gain code represents a 0.125dB gain step. The gain control may not be monotonic between the codes 63-64, and 127-128 because of device mismatch; the maximum error is within 0.25dB.

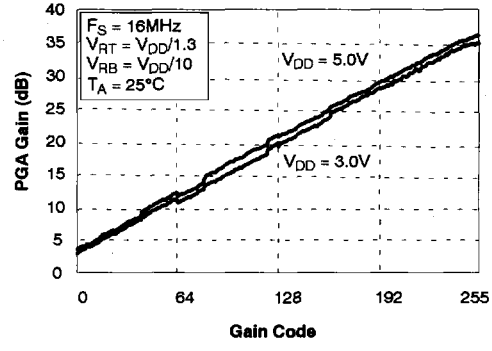

Figure 6. PGA Gain vs. Gain Code

Offset Calibration

To get maximum resolution in dark areas of an image the black level offset of the PGA must be equal to the bottom reference voltage of the ADC. The offset calibration logic operates during the interline black level clamping (CLAMP=active). The logic compares the ADC output code to the value stored in the offset register, and then increments or decrements the offset adjust DAC to make the ADC output equal to the code in the offset register. Each adjustment requires 6 cycles of the SHP/SHD clocks: 1 cycle for CDS, 3 cycles for A/D conversion, 1 cycle for logic, and 1 cycle for DAC update. Once the CLAMP signal is deactivated, the calibration process stops, and the black level calibration state is held. The offset register is 8-bits wide and is programmed through the serial port. The default value of this register at power up is 08h. Typical values for this register are between 02h and 20h. When the part is first powered up, the calibration may take several hundred clock cycles to converge to the proper offset. However, it requires only a few clock cycles subsequently to maintain the offset value (see *Figure 7*).

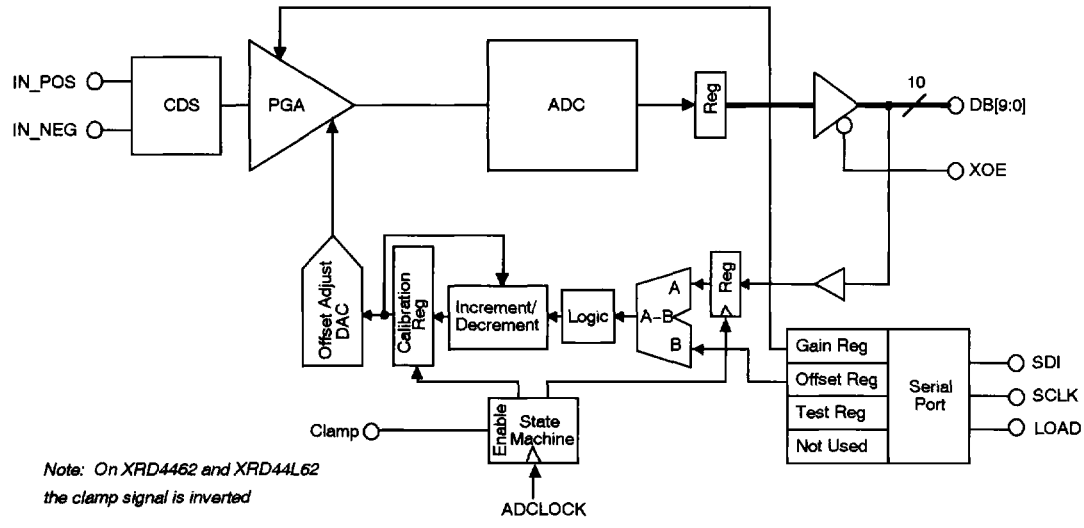

Figure 7. Offset Calibration Loop

Analog To Digital Converter

The analog-to-digital converter is based upon a two-step sub-ranging flash converter architecture with a built in track and hold input stage. The ADC conversion is controlled by an internally generated signal, ADCLK (see *Figure 5)*. The ADC tracks the output of the CDS/PGA while ADCLK is high and holds when ADCLK is low. This allows maximum time for the CDS/PGA output to settle to its final value before being sampled. The conversion is then performed and the parallel output is updated, after a 2.5 cycle pipeline delay, on the rising edge of RSTCCD. The pipeline delay of the entire chip is 4 clock cycles. The references of the ADC are generated internally. The internal reference values are set by a resistor divider between V_{DD} and GND. To maximize performance the internal references should be decoupled to GND. The ADC parallel output bus is equipped with a high impedance capability, controlled by $\overline{OE}$. The outputs are enabled when $\overline{OE}$ is low.

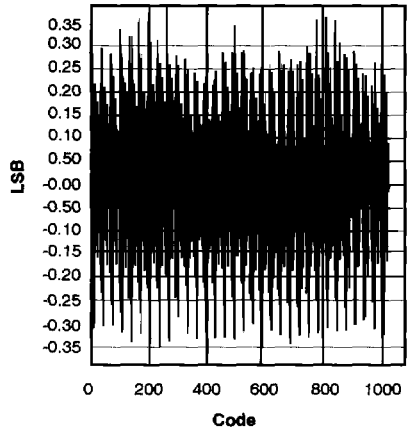

Figure 8. ADC Core Differential Non-Linearity (DNL)

Input Serial Port

A three wire serial interface is used to control the PGA code register and the offset register (there are also two test registers which should not be modified). The shift register is 10-bits long. The first two bits loaded in the shift register are the address bits for which internal register is to get updated, the following eight bits are the data (MSB first, LSB last). The port is controlled by the SCLK, LOAD and SDI pins. To enable the shift register the LOAD pin must be held low. When load is high, SCLK is internally disabled. Since SCLK is gated by LOAD, SCLK can be a continuously running clock signal, but this will increase system noise. The data at SDI is strobed into the shift register on the rising edges of SCLK. The addressed internal register is updated when the LOAD signal goes high (see *Figure 9*).

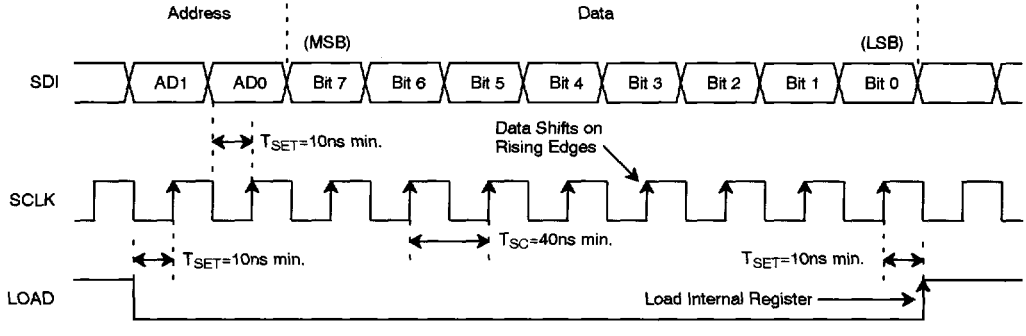

Figure 9. Serial Port Timing

The following truth table gives the address for the serial port registers.

AD1	AD0	Register
0	0	PGA Code
0	1	Offset Code
1	0	Test
1	1	Unused

Table 3. Serial Port Truth Table

Stand By Mode (Power Down)

Pulling $\overline{\text{STBY}}$ low puts the chip in the low power, stand-by mode. In this mode all sampling and conversions stop, the digital outputs go into the high impedance state and the power supply current drops to under 50μA.

Chip Reset

When the reset pin is forced high all the internal control registers are set to reset values. The chip also has an internal power-on-reset function to ensure reset conditions are established when the chip is first powered up. The reset values are:

Gain register set to minimum gain (code 00000000).

Offset register set to 08h (code 00001000).

Offset calibration register set to uncalibrated state.

ADC output register set to 000h (code 0000000000).

CDS Clock Polarity

The difference between the XRD4461 and the XRD4462 is the polarity of the CDS clocks (SHD, SHP, CLAMP) (see *Figure 10* and *Figure 11).*

On the XRD4461 & XRD44L61:

CLAMP is active high.

Falling edge of SHP samples pixel black level.

Falling edge of SHD samples pixel data.

RSTCCD high disconnects input.

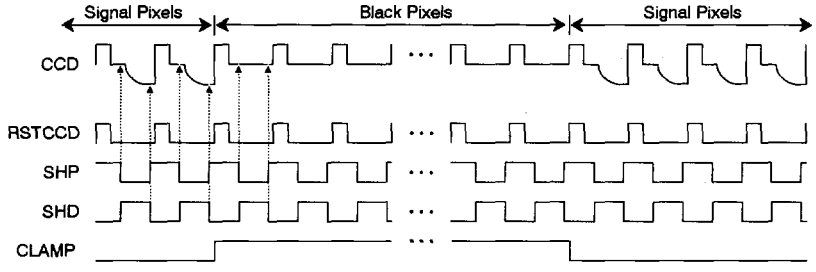

Figure 10. CDS Timing for XRD4461 & XRD44L61

On the XRD4462 & XRD44L62:

CLAMP is active low.

Rising edge of SHP samples pixel black level.

Rising edge of SHD samples pixel data.

RSTCCD high disconnects input.

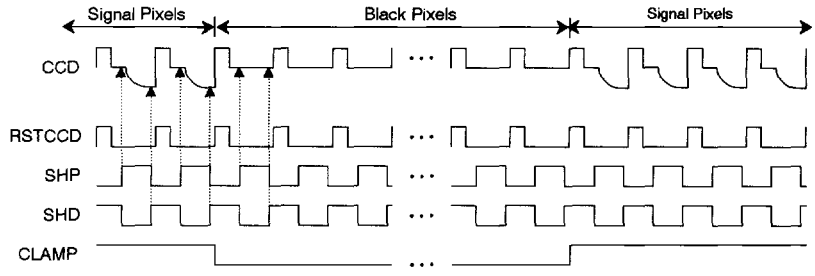

Figure 11. CDS Timing for XRD4462 & XRD44L62

Digital Output Power Supplies

The DV_{DD} and DGND pins supply power to the digital output drivers for pins DB[9:0]. DV_{DD} is isolated from V_{DD} so it can be at a voltage level less than or equal to V_{DD}. This allows the digital outputs to interface with advanced digital ASICs requiring reduced supply voltages. For example V_{DD} can be 5.0 or 3.3V, while DV_{DD} is 2.5V.

Systems which use the same voltage level for both analog and digital power supplies can take advantage of the isolated DV_{DD} & DGND pins to reduce system noise. The output drivers create large supply transients as they switch. Therefore DV_{DD} and DGND should be routed separately from the analog V_{DD} & GND to avoid injecting this noise into the analog power network (see *Figure 12.*)

Power Supply Sequencing

There are no power supply sequencing issues if DV_{DD} and V_{DD} are driven from the same supply. When DV_{DD} and V_{DD} are driven separately, V_{DD} must come up at the same time or before DV_{DD}, and go down at the same time or after DV_{DD}. If the power supply sequencing in this case is not followed, then damage may occur to the product due to current flow through the source-body junction diodes between DV_{DD} and V_{DD}. An external diode (5082-2235) layed out close to the converter from DV_{DD} to V_{DD} prevents damage from occurring when power is cycled incorrectly.

Note: *V_{DD} must be greater than or equal to DV_{DD} or the source-body diodes will be forward biased.*

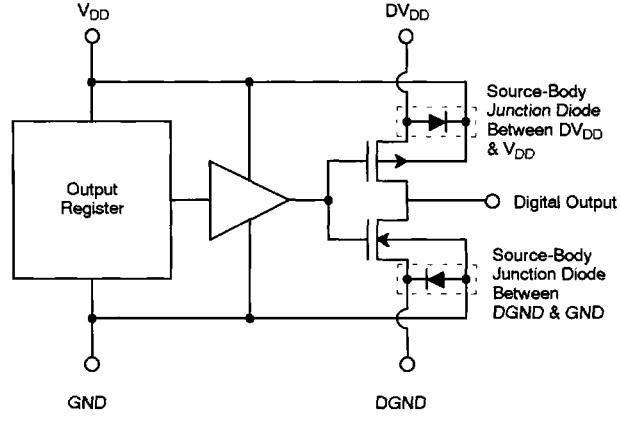

Figure 12. DV_{DD} & DGND Digital Output Power Supplies

General Power Supply and Board Design Issues

All of the GND pins, other than DGND, are tied to the substrate and should be connected directly to the analog ground plane. The V_{DD}'s should be supplied from a low noise, well filtered regulator which derives the power supply voltage from the CCD power supply. All of the V_{DD} pins are analog power supplies and should be locally decoupled to the nearest GND pin with a 0.01µF, high frequency capacitor. DV_{DD} and DGND are the power supplies for the digital outputs and should be locally decoupled. DV_{DD} and DGND should be connected to the same power supply network as the digital ASIC which receives data from this chip.

In general, all traces leading to this part should be as short as possible to minimize signal crosstalk and high frequency digital signals from feeding into sensitive analog inputs. The two CCD inputs, In_Pos and In_Neg, should be routed as fully differential signals and should be shielded and matched. Efforts should be made to minimize the board leakage currents on In_Pos and In_Neg since these nodes are AC coupled to the CCD. The digital output traces should be as short as possible to minimize the capacitive loading on the output drivers (see *Figure 13.*)

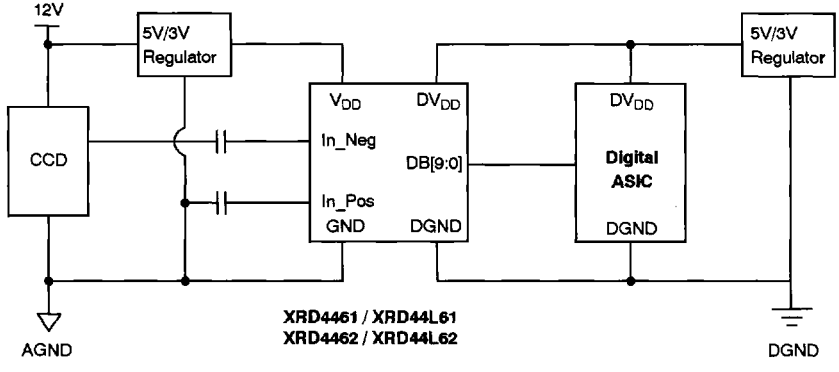

Figure 13. Power Supply Connections

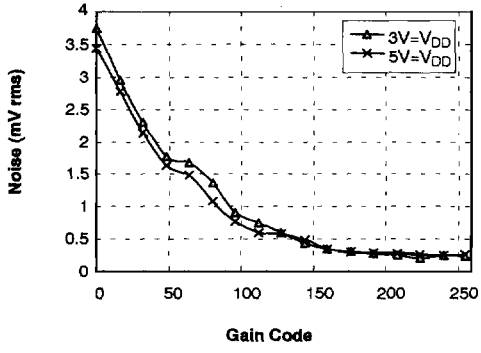

Figure 14. Input Referred Noise vs Gain Code, F_S=16MSPS

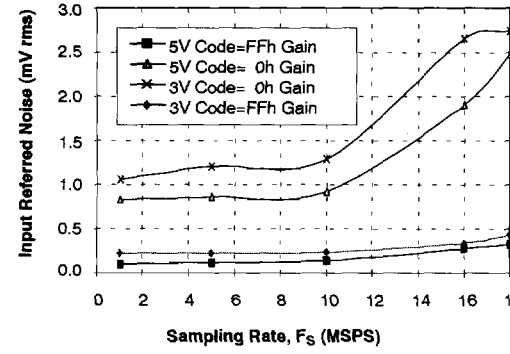

Figure 15. Input Referred Noise at Gain Code FFh and 0 vs Sampling Rate

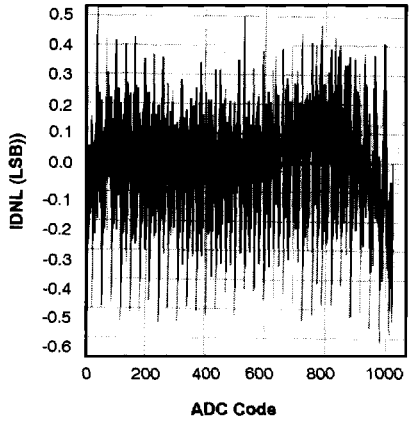

Figure 16. DNL_S for the Entire Chip

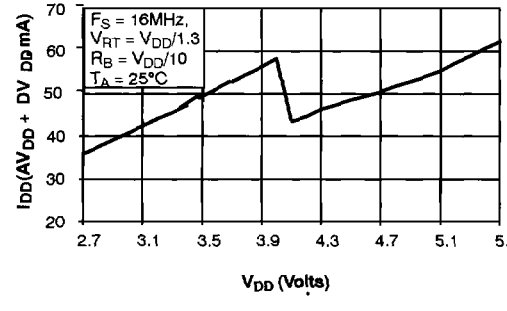

Figure 17. I_{DD} vs V_{DD} Shows the Internal Regulation of V_{DD}

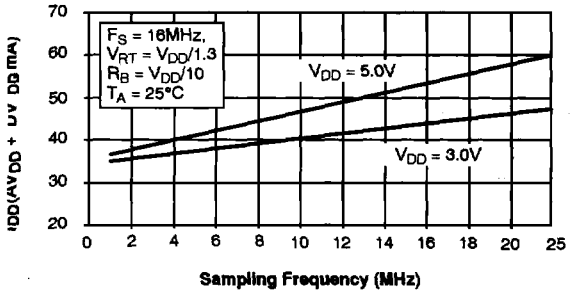

Figure 18. I_{DD} vs Sample Rate

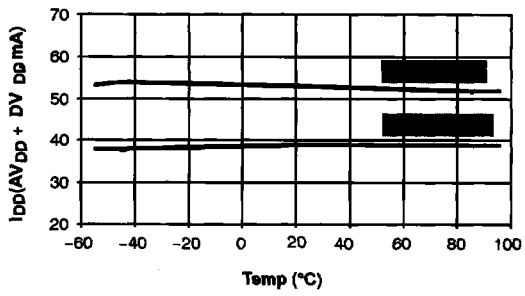

Figure 19. I_{DD} vs Temperature, F_S=16MSPS, V_{RT}=V_{DD}/1.3, V_{RB}=V_{DD}/10

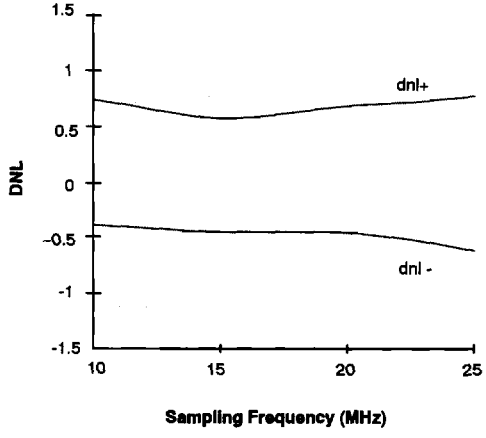

Figure 20. 4461 DNL vs Sampling Frequecy, V_{DD} = 3V

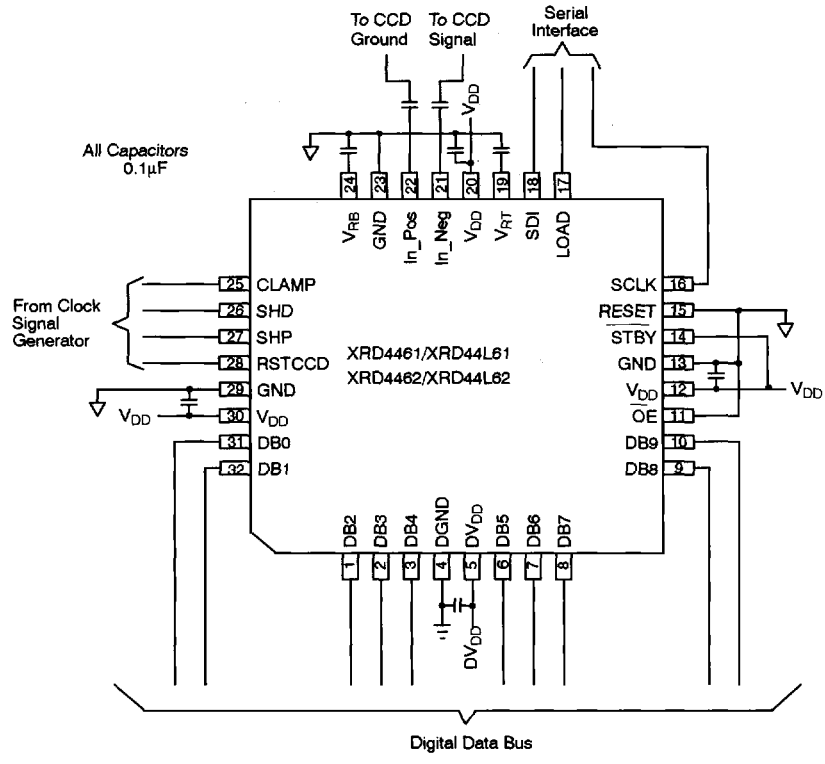

Figure 21. Application Schematic