June 1988

Z8® Z8681
ROMless Microcomputer

FEATURES

- Complete microcomputer, 24 I/O lines, and up to 64K bytes of addressable external space each for program and data memory.
- 143-byte register file, including 124 general-purpose registers, three I/O port registers, and 16 status and control registers.
- Vectored, priority interrupts for I/O, counter/timers, and UART.
- On-chip oscillator that accepts crystal or external clock drive.
- Full-duplex UART and two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler.
- Register Pointer so that short, fast instructions can access any one of the nine working-register groups.
- Single +5V power supply—all I/O pins TTL-compatible.
- Available in 8 MHz.

GENERAL DESCRIPTION

The Z8681 is the ROMless version of the Z8 single-chip microcomputer. The Z8681 offers all the outstanding features of the Z8 family architecture except an on-chip program ROM. Use of external memory rather than a preprogrammed ROM enables this Z8 microcomputer to be used in low volume applications or where code flexibility is required.

The Z8681 can provide up to 16 output address lines, thus permitting an address space of up to 64K bytes of data or program memory. Eight address outputs (AD_0-AD_7) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits can be provided by the software configuration of Port 0 to output address bits A_8-A_{15}.

Available address space can be doubled (up to 128K bytes) by programming bit 4 of Port 3 ($P3_4$) to act as a data memory select output (DM). The two states of DM together with the 16 address outputs can define separate data and memory address spaces of up to 64Kbytes each.

There are 143 bytes of RAM located on-chip and organized as a register file of 124 general-purpose registers, 16 control and status registers, and three I/O port registers. This register file can be divided into nine groups of 16 working registers each. Configuring the register file in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly.

ABSOLUTE MAXIMUM RATINGS

Guaranteed by characterization/design

Voltages on all pins except $\overline{RESET}$
with respect to GND . . . . . −0.3V to +7.0V
Operating Case Temperature . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Absolute Maximum Power Dissipation . . . . . 1.7 W

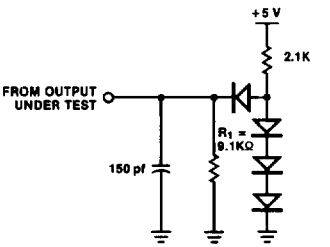
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The DC characteristics listed below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

Military Operating Temperature Range (T_C)
−55°C to +125°C

Standard Military Test Condition
$+4.5 \leqslant V_{CC} \leqslant +5.5V$



Test Load

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Condition
V_{CH}	Clock Input High Voltage	3.8[a]	V_{CC}[b]	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	−0.3[b]	0.8[a]	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0[a]	V_{CC}[b]	V	
V_{IL}	Input Low Voltage	−0.3[b]	0.8[a]	V	
V_{RH}	Reset Input High Voltage	3.8[a]	V_{CC}[b]	V	
V^{RL}	Reset Input Low Voltage	−0.3[b]	0.8[a]	V	
V_{OH}	Output High Voltage	2.4[a]		V	I_{OH} = −250 μA
V_{OL}	Output Low Voltage		0.4[a]	V	I_{OL} = +2.0 mA
I_{IL}	Input Leakage	−10[a]	10[a]	μA	V_{IN} = 0V, 5.5V
I_{OL}	Output Leakage	−10[a]	10[a]	μA	V_{IN} = 0V, 5.5V
I_{IR}	Reset Input Current		−50[a]	μA	V_{CC} = MAX, V_{RL} = 0V
I_{CC}	V_{CC} Supply Current		230[a]	mA	All outputs and I/O pins floating

CAPACITANCE

Symbol	Parameter	Max	Unit
C_{MAX}	Maximum Capacitance	15[c]	pf

T_A = 25°C, f = 1 MHz.

Parameter Test Status:

[a] Tested
[b] Guaranteed
[c] Guaranteed by Characterization/Design

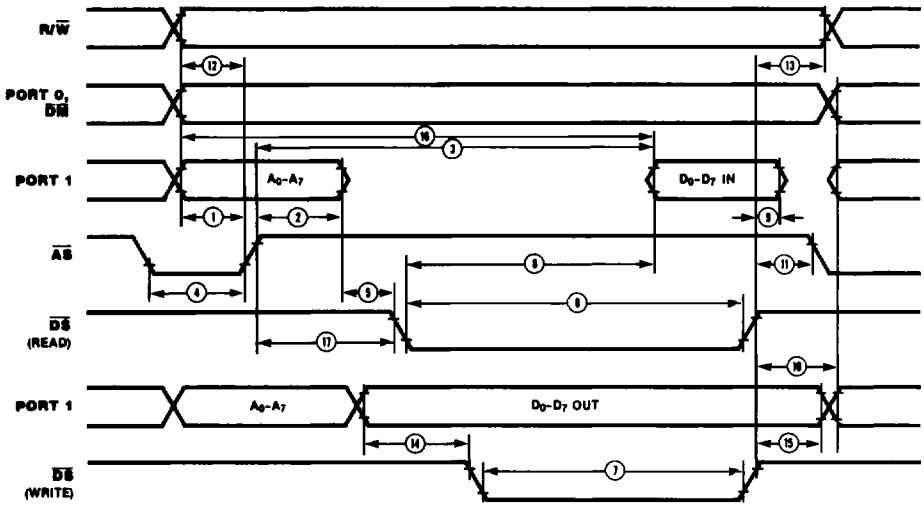


Figure 1. External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

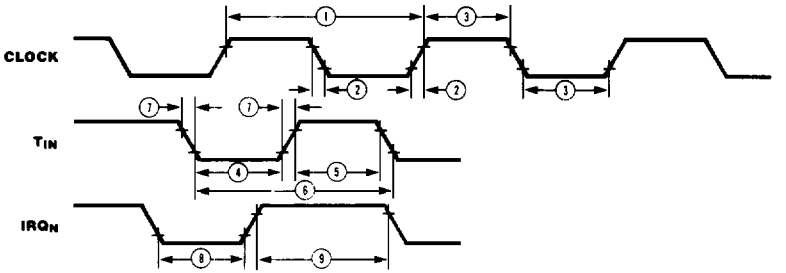
External I/O or Memory Read and Write Timing

Number	Symbol	Parameter	Z8681 8 MHz Min	Z8681 8 MHz Max	Notes* °
1	TdA(AS)	Address Valid to $\overline{AS}$ ↑ Delay	50[a]		2,3
2	TdAS(A)	$\overline{AS}$ ↑ to Address Float Delay	70[a]		2,3
3	TdAS(DR)	$\overline{AS}$ ↑ to Read Data Required Valid		420[a]	1,2,3
4	TwAS	$\overline{AS}$ Low Width	80[a]		2,3
5	TdAz(DS)	Address Float to $\overline{DS}$ ↓	0[b]		
6	TwDSR	$\overline{DS}$ (Read) Low Width	250[a]		1,2,3
7	TwDSW	$\overline{DS}$ (Write) Low Width	160[a]		1,2,3
8	TdDSR(DR)	$\overline{DS}$ ↓ to Read Data Required Valid		200[a]	1,2,3
9	ThDR(DS)	Read Data to $\overline{DS}$ ↑ Hold Time	0[a]		
10	TdDS(A)	$\overline{DS}$ ↑ to Address Active Delay	70[a]		2,3
11	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	70[a]		2,3
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ ↑ Delay	50[a]		2,3
13	TdDS(R/W)	$\overline{DS}$ ↑ to R/$\overline{W}$ Not Valid	60[a]		2,3
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ (Write) ↓ Delay	50[a]		2,3
15	TdDS(DW)	$\overline{DS}$ ↑ to Write Data Not Valid Delay	60[a]		2,3
16	TdA(DR)	Address Valid to Read Data Required Valid		410[a]	1,2,3
17	TdAS(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	80[a]		2,3

NOTES:
1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. See clock cycle time dependent characteristics table.

* All units in nanoseconds (ns).
° All timing references use 2.0V for a logic "1" and 0.8V for a logic "0".

Parameter Test Status:
[a] Tested
[b] Guaranteed
[c] Guaranteed by Characterization/Design



AC CHARACTERISTICS

Additional Timing Table

Number	Symbol	Parameter	Z8681 8 MHz Min	Z8681 8 MHz Max	Notes*
1	TpC	Input Clock Period	125[a]	1000[a]	1
2	TrC,TfC	Clock Input Rise and Fall Times		25[b]	1
3	TwC	Input Clock Width	37[b]		1
4	TwTinL	Timer Input Low Width	100[b]		2
5	TwTinH	Timer Input High Width	3TpC[b]		2
6	TpTin	Timer Input Period	8TpC[b]		2
7	TrTin,TfTin	Timer Input Rise and Fall Times		100[b]	2
8A	TwIL	Interrupt Request Input Low Time	100[b]		2,3,4
8B	TwIL	Interrupt Request Input Low Time	3TpC[b]		2,3,5
9	TwIH	Interrupt Request Input High Time	3TpC[b]		2,3

NOTES:

1. Clock timing references use 3.8V for a logic "1" and 0.8V for a logic "0".
2. Timing references use 2.0V for a logic "1" and 0.8V for a logic "0".
3. Interrupt request via Port 3.
4. Interrupt request via Port 3 ($P3_1$-$P3_3$)
5. Interrupt request via Port 3 ($P3_0$)

* Units in nanoseconds (ns).

Parameter Test Status:

[a] Tested
[b] Guaranteed
[c] Guaranteed by Characterization/Design

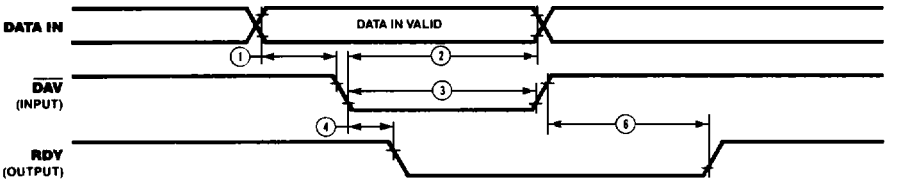


Figure 3a. Input Handshake Timing

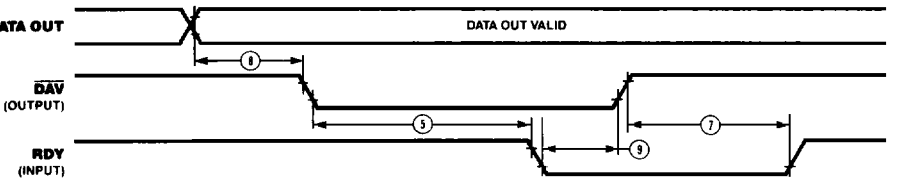


Figure 3b. Output Handshake Timing

AC CHARACTERISTICS

Handshake Timing

Number	Symbol	Parameter	Z8681 Min	Z8681 Max	Notes†*
1	TsDI(DAV)	Data In Setup Time	0[a]		
2	ThDI(DAV)	Data In Hold Time	230[a]		
3	TwDAV	Data Available Width	175[a]		
4	TdDAVIf(RDY)	$\overline{DAV}$ ↓ Input to RDY ↓ Delay		175[a]	1
5	TdDAVOf(RDY)	$\overline{DAV}$ ↓ Output to RDY ↓ Delay	0[a]		2
6	TdDAVIr(RDY)	$\overline{DAV}$ ↑ Input to RDY ↑ Delay		175[a]	1
7	TdDAVOr(RDY)	$\overline{DAV}$ ↑ Output to RDY ↑ Delay	0[a]		2
8	TdDO(DAV)	Data Out to $\overline{DAV}$ ↓ Delay	50[a]		
9	TdRDY(DAV)	Rdy ↓ Input to $\overline{DAV}$ ↑ Delay	0[b]	200[a]	

NOTES:
1. Input handshake
2. Output handshake

† All timing references use 2.0V for a logic "1" and 0.8V for a logic "0".

* Units in nanoseconds (ns).

Parameter Test Status:

[a] Tested
[b] Guaranteed
[c] Guaranteed by Characterization/Design

CLOCK CYCLE TIME-DEPENDENT CHARACTERISTICS

Number	Symbol	Z8681 8 MHz Equation
1	TdA(AS)	TpC-75
2	TdAS(A)	TpC-55
3	TdAS(DR)	4TpC-140 *
4	TwAS	TpC-45
6	TwDSR	3TpC-125 *
7	TwDSW	2TpC-90 *
8	TdDSR(DR)	3TpC-175 *
10	Td(DS)A	TpC-55
11	TdDS(AS)	TpC-55
12	TdR/W(AS)	TpC-75
13	TdDS(R/W)	TpC-65
14	TdDW(DSW)	TpC-75
15	TdDS(DW)	TpC-55
16	TdA(DR)	5TpC-215 *
17	TdAS(DS)	TpC-45

* Add 2TpC when using extended memory timing

PIN DESCRIPTION

$\overline{AS}$. *Address Strobe* (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Addresses output via Port 1 for all external program or data memory transfers are valid at the trailing edge of $\overline{AS}$.

$\overline{DS}$. *Data Strobe* (output, active Low). Data Strobe is activated once for each external memory transfer.

$P0_0$-$P0_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$. *I/O Port Lines* (input/outputs, TTL-compatible). These 24 lines are divided into three 8-bit I/O ports that can be configured under program control for I/O or external memory interface.

$P1_0$-$P1_7$. *Address/Data Port* (bidirectional). Multiplexed address (A_0-A_7) and data (D_0-D_7) lines used to interface with program and data memory.

$\overline{RESET}$. *Reset* (input, active Low). $\overline{RESET}$ initializes the Z8681. After $\overline{RESET}$ the Z8681 is in the extended memory mode. When $\overline{RESET}$ is deactivated, program execution begins from program location $000C_H$.

R/$\overline{W}$. *Read/Write* (output). R/$\overline{W}$ is Low when the Z8681 is writing to external program or data memory.

XTAL1, XTAL2. *Crystal 1, Crystal 2* (time-base input and output). These pins connect a parallel-resonant crystal to the on-chip clock oscillator and buffer.

PACKAGE PINOUTS

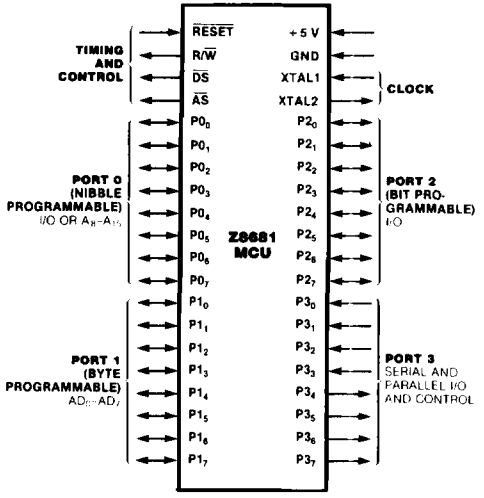


Figure 4. Pin Functions

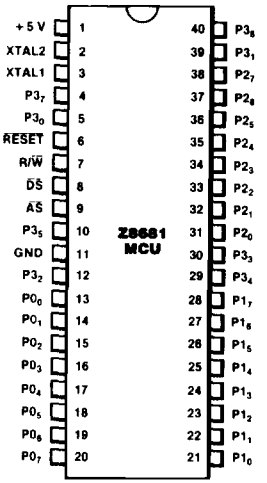


Figure 5. 40-pin Dual-In-Line Package (DIP), Pin Assignments

MIL-STD-883 MILITARY PROCESSED PRODUCT

- Mil-Std-883 establishes uniform methods and procedures for testing microelectronic devices to insure the electrical, mechanical, and environmental integrity and reliability that is required for military applications.
- Mil-Std-883 Class B is the industry standard product assurance level for military ground and aircraft application.
- The total reliability of a system depends upon tests that are designed to stress specific quality and reliability concerns that affect microelectronic products.
- The following tables detail the 100% screening and electrical tests, sample electrical tests, and Qualification/ Quality Conformance testing required.

Zilog Military Product Flow

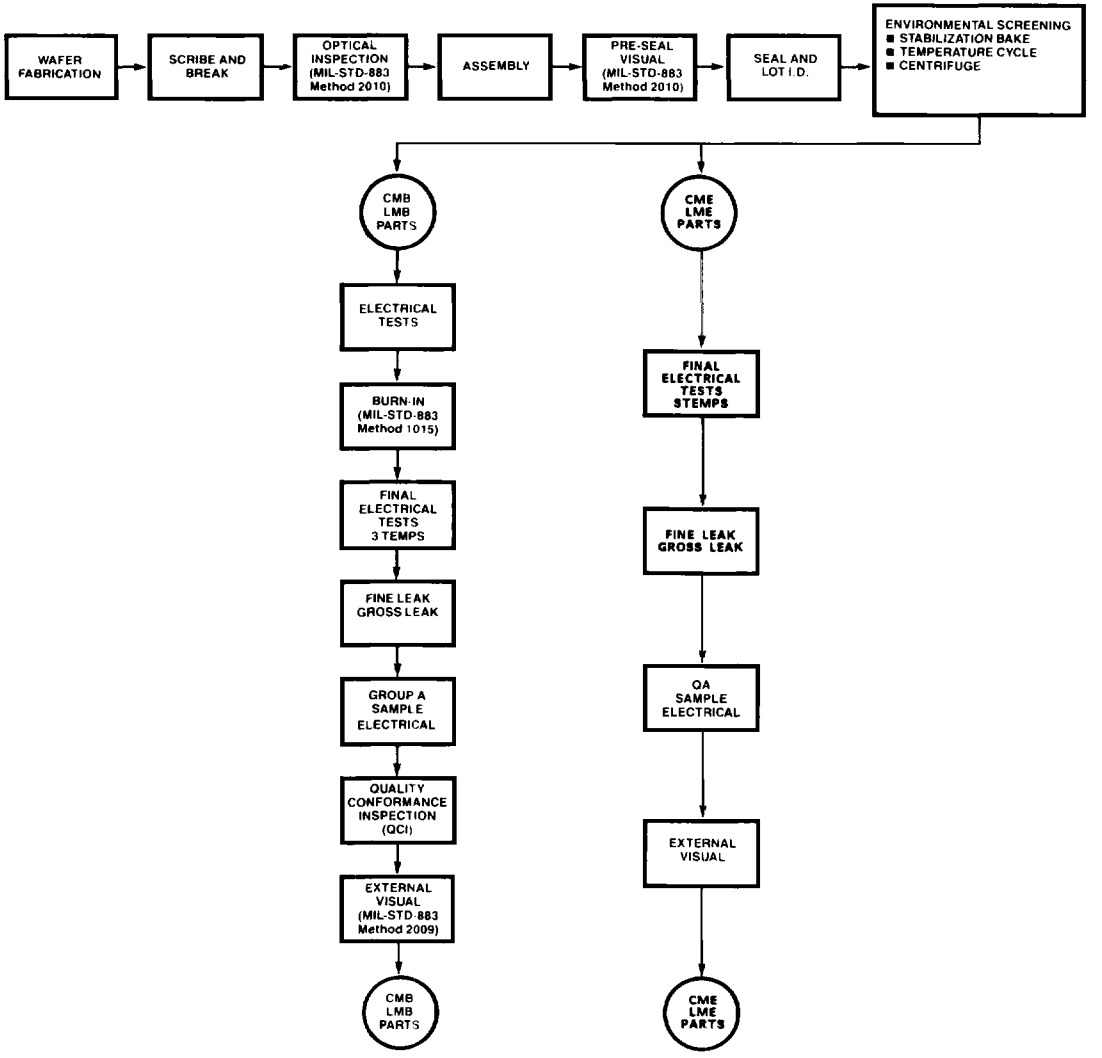


Table I

MIL-STD-883 Class B Screening Requirements
Method 5004

Test	Mil-Std-883 Method	Test Condition	Requirement
Internal Visual	2010	Condition B	100%
Stabilization Bake	1008	Condition C	100%
Temperature Cycle	1010	Condition C	100%
Constant Acceleration (Centrifuge)	2001	Condition E or D(Note 1), Y_1 Axis Only	100%
Initial Electrical Tests		Zilog Military Electrical Specification Static/DC T_C = +25°C	100%
Burn-In	1015	Condition D(Note 2), 160 hours, T_A = +125°C	100%
Interim Electrical Tests		Zilog Military Electrical Specification Static/DC T_C = +25°C	100%
PDA Calculation		PDA = 5%	100%
Final Electrical Tests		Zilog Military Electrical Specification Static/DC T_C = +125°C, −55°C Functional, Switching/AC T_C = +25°C	100%
Fine Leak	1014	Condition B	100%
Gross Leak	1014	Condition C	100%
Quality Conformance Inspection (QCI)			
Group A Each Inspection Lot	5005	(See Table II)	Sample
Group B Every Week	5005	(See Table III)	Sample
Group C Periodically (Note 3)	5005	(See Table IV)	Sample
Group D Periodically (Note 3)	5005	(See Table V)	Sample
External Visual	2009		100%
QA—Ship			100%

NOTES:

1. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.
2. In process of fully implementing of Condition D Burn-In Circuits. Contact factory for copy of specific burn-in circuit available.
3. Performed periodically as required by Mil-Std-883, paragraph 1.2.1 b(17).
4. **Fully compliant to MIL-STD-883 Rev. C.**

Table II Group A

Sample Electrical Tests
MIL-STD-883 Method 5005

Subgroup	Tests	Temperature (T_C)	LTPD Max Accept = 2
Subgroup 1	Static/DC	+25°C	2
Subgroup 2	Static/DC	+125°C	3
Subgroup 3	Static/DC	−55°C	5
Subgroup 7	Functional	+25°C	2
Subgroup 8	Functional	−55°C and +125°C	5
Subgroup 9	Switching/AC	+25°C	2
Subgroup 10	Switching/AC	+125°C	3
Subgroup 11	Switching/AC	−55°C	5

NOTES:
- The specific parameters to be included for tests in each subgroup shall be as specified in the applicable detail electrical specification. Where no parameters have been identified in a particular subgroup or test within a subgroup, no Group A testing is required for that subgroup or test.
- A single sample may be used for all subgroup testing. Where required size exceeds the lot size, 100% inspection shall be allowed.
- Group A testing by subgroup or within subgroups may be performed in any sequence unless otherwise specified.

Table III Group B

Sample Test Performed Every Week to Test Construction and Insure Integrity of Assembly Process. MIL-STD-883 Method 5005

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 1			
Physical Dimensions	2016		2/0
Subgroup 2			
Resistance to Solvents	2015		4/0
Subgroup 3			
Solderability	2003	Solder Temperature +245°C ± 5°C	15(Note 1)
Subgroup 4			
Internal Visual and Mechanical	2014		1/0
Subgroup 5			
Bond Strength	2011	C	15(Note 2)
Subgroup 6(Note 3)			
Internal Water Vapor Content	1018	1000 ppm. maximum at +100°C	3/0 or 5/1
Subgroup 7(Note 4)			
Seal	1014		5
7a) Fine Leak		7a) B	
7b) Gross Leak		7b) C	
Subgroup 8(Note 5)			
Electrostatic Discharge Sensitivity	3015	Zilog Military Electrical Specification Static/DC T_C = +25°C A = 20-2000V B = >2000V Zilog Military Electrical Specification Static/DC T_C = +25°C	15/0

NOTES:

1. Number of leads inspected selected from a minimum of 3 devices.
2. Number of bond pulls selected from a minimum of 4 devices.
3. Test applicable only if the package contains a dessicant.
4. Test not required if either 100% or sample seal test is performed between final electrical tests and external visual during Class B screening.
5. Test required for initial qualification and product redesign.

Table IV Group C

Sample Test Performed Periodically to Verify Integrity of the Die.
MIL-STD-883 Method 5005

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 1			
Steady State Operating Life	1005	Condition D(Note 1), 1000 hours at +125°C	5
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	
Subgroup 2			
Temperature Cycle	1010	Condition C	
Constant Acceleration (Centrifuge)	2001	Condition E or D(Note 2), Y_1 Axis Only	
Seal	1014		15
2a) Fine Leak		2a) Condition B	
2b) Gross Leak		2b) Condition C	
Visual Examination	1010 or 1011		
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	

NOTE:
1. In process of fully implementing Condition D Burn-In Circuits. Contact factory for copy of specific burn-in circuit available.
2. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.

Table V Group D

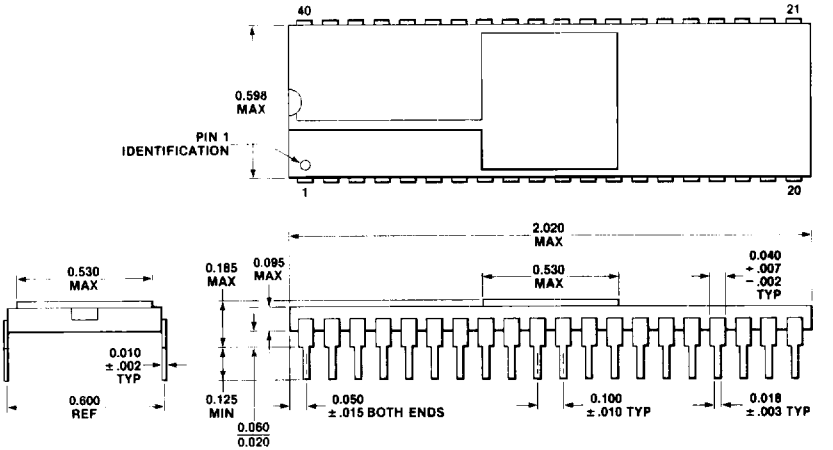
Sample Test Performed Periodically to Insure Integrity of the Package.
MIL-STD-883 Method 5005

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 1			
Physical Dimensions	2016		15
Subgroup 2			
Lead Integrity	2004	Condition B_2 or D(Note 1)	15
Subgroup 3			
Thermal Shock	1011	Condition B minimum, 15 cycles minimum	
Temperature Cycling	1010	Condition C, 100 cycles minimum	15
Moisture Resistance	1004		
Seal	1014		
3a) Fine Leak		3a) Condition B	
3b) Gross Leak		3b) Condition C	
Visual Examination	1004 or 1010		
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	
Subgroup 4			
Mechanical Shock	2002	Condition B minimum	
Vibration Variable Frequency	2007	Condition A minimum	
Constant Acceleration (Centrifuge)	2001	Condition E or D(Note 2), Y_1 Axis Only	15
Seal	1014		
4a) Fine Leak		4a) Condition B	
4b) Gross Leak		4b) Condition C	
Visual Examination	1010 or 1011		
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	
Subgroup 5			
Salt Atmosphere	1009	Condition A minimum	
Seal	1014		15
5a) Fine Leak		5a) Condition B	
5b) Gross Leak		5b) Condition C	
Visual Examination	1009		
Subgroup 6			
Internal Water Vapor Content	1018	5,000 ppm. maximum water content at +100°C	3/0 or 5/1
Subgroup 7(Note 3)			
Adhesion of Lead Finish	2025		15(Note 4)
Subgroup 8(Note 5)			
Lid Torque	2024		5/0

NOTES:

1. Lead Integrity Condition D for leadless chip carriers.
2. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.
3. Not applicable to leadless chip carriers.
4. LTPD based on number of leads.
5. Not applicable for solder seal packages.

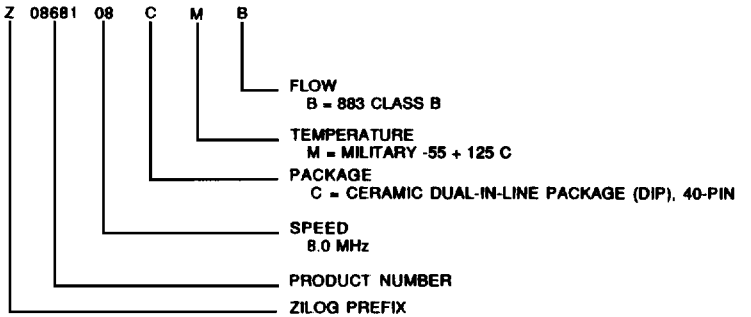
PACKAGE INFORMATION (Continued)



40-Pin Dual-In-Line Package (DIP), Ceramic

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

ZILOG ORDERING INFORMATION



AVAILABLE MILITARY PRODUCTS

Z8 ROMless MCU, 8.0 MHz
40-pin DIP
Z0868108CME
Z0868108CMB

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