



### Features

- This Circuit is Processed in Accordance to Mil-Std-883C and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- 0 to 25.6MHz Sample Rate
- Eight Filter Cells
- 8-Bit Coefficients and Signal Data
- Low Power CMOS Operation
  - ICCSB 500µA Maximum
  - ICCOP 160µA Maximum @ 20MHz
- 26-Bit Accumulator Per Stage
- Filter Lengths Up to 1032 Taps
- Shift and Add Output Stage for Combining Filter Outputs
- Expandable Coefficient Size, Data Size and Filter Length
- Decimation by 2, 3 or 4

### Applications

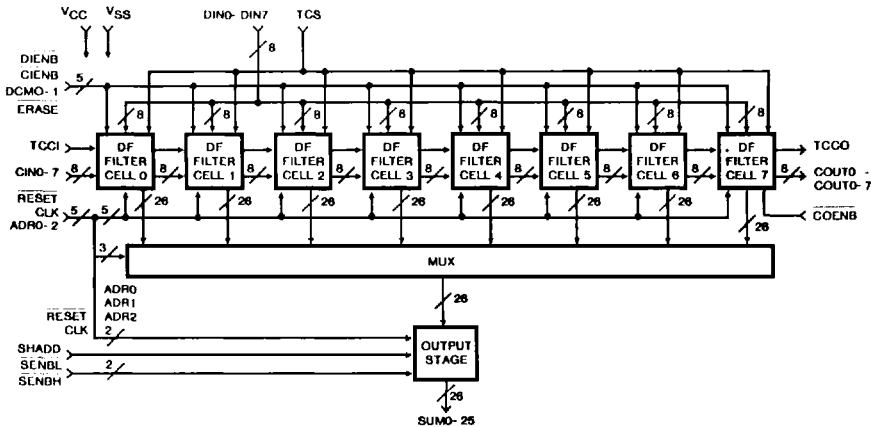
- 1-D and 2-D FIR Filters
- Radar/Sonar
- Digital Video and Audio
- Adaptive Filters
- Echo Cancellation
- Correlation/Convolution
- Complex Multiply-Add
- Butterfly Computation
- Matrix Multiplication
- Sample Rate Converters

### Description

The HSP43881/883 is a video speed Digital Filter (DF) designed to efficiently implement vector operations such as FIR digital filters. It is comprised of eight filter cells cascaded internally and a shift and add output stage, all in a single integrated circuit. Each filter cell contains an 8x8 bit multiplier, three decimation registers and a 26-bit accumulator. The output stage contains an additional 26-bit accumulator which can add the contents of any filter cell accumulator to the output stage accumulator shifted right by 8 bits. The HSP43881/883 has a maximum sample rate of 25.6MHz. The effective multiply accumulate (mac) rate is 204MHz. The HSP43881/883 DF can be configured to process expanded coefficient and word sizes. Multiple DFs can be cascaded for larger filter lengths without degrading the sample rate or a single DF can process larger filter lengths at less than 25.6MHz with multiple passes. The architecture permits processing filter lengths of over 1000 taps with the guarantee of no overflows. In practice, most filter coefficients are less than 1.0, making even larger filter lengths possible. The DF provides for 8-bit unsigned or two's complement arithmetic, independently selectable for coefficients and signal data.

Each DF filter cell contains three resampling or decimation registers which permit output sample rate reduction at rates of 1/2, 1/3 or 1/4 the input sample rate. These registers also provide the capability to perform 2-D operations such as matrix multiplication and NxN spatial correlations/convolutions for image processing applications.

### Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.  
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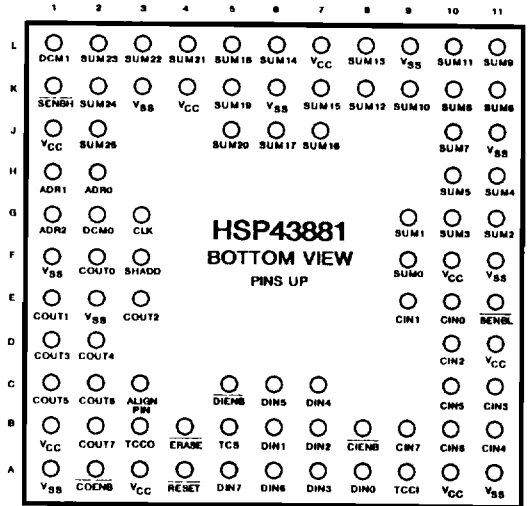
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1-D FILTERS

# HSP43881/883

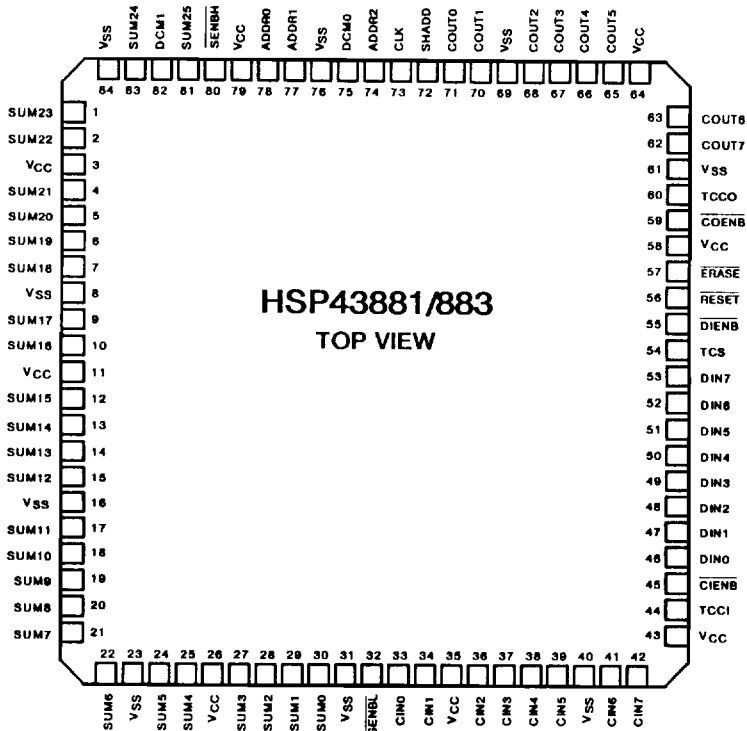
## Pinouts

### 85 PIN GRID ARRAY (PGA)

	1	2	3	4	5	6	7	8	9	10	11			
A	V <sub>SS</sub>	COENB	V <sub>CC</sub>	RESET	DIN7	DIN6	DIN3	DINO	TCCI	V <sub>CC</sub>	V <sub>SS</sub>			
B	V <sub>CC</sub>	COU7	TCCO	ERASE	TCS	DIN1	DIN2	CIENB	CIN7	CIN6	CIN4			
C	COU5	COU8	ALIGN PIN		DIENB	DIN5	DIN4	8834HSP43881 P4388101 GEM		CIN5	CIN3			
D	COU3	COU4		<b>HSP43881/883</b> <b>TOP VIEW</b> <b>PINS DOWN</b>						CIN2	V <sub>CC</sub>			
E	COU1	V <sub>SS</sub>	COU2									CIN1	CIN0	SENBL
F	V <sub>SS</sub>	COU0	SHADD									SUM0	V <sub>CC</sub>	V <sub>SS</sub>
G	ADR2	DCM0	CLK									SUM1	SUM3	SUM2
H	ADR1	ADR0										SUM5	SUM4	
J	V <sub>CC</sub>	SUM25			SUM20	SUM17	SUM16		SUM7	V <sub>SS</sub>				
K	SENH	SUM24	V <sub>SS</sub>	V <sub>CC</sub>	SUM19	V <sub>SS</sub>	SUM15	SUM12	SUM10	SUM9	SUM6			
L	DCM1	SUM23	SUM22	SUM21	SUM18	SUM14	V <sub>CC</sub>	SUM13	V <sub>SS</sub>	SUM11	SUM8			



### 84 LEAD CERAMIC QUAD FLATPACK PACKAGE



Note: An overbar on a signal name represents an active LOW signal.

# Specifications HSP43881/883

## Absolute Maximum Ratings

Supply Voltage .....	+8.0V
Input, Output Voltage Applied .....	GND-0.5V to $V_{CC}+0.5V$
Storage Temperature Range .....	-65°C to +150°C
Junction Temperature .....	+175°C
Lead Temperature (Soldering, Ten Seconds) .....	+300°C
ESD Classification .....	Class 1

## Reliability Information

Thermal Resistance	$\theta_{ja}$	$\theta_{jc}$
Ceramic PGA Package .....	34.66°C/W	7.78°C/W
Maximum Package Power Dissipation at +125°C		
Ceramic PGA Package .....	1.44 Watt	
Gate Count .....	17762 Gates	

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## Operating Conditions

Operating Voltage Range .....	+4.5V to +5.5V
Operating Temperature Range .....	-55°C to +125°C

**TABLE 1. HSP43881/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS**

Devices Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Logical One Input Voltage	$V_{IH}$	$V_{CC} = 5.5V$	1, 2, 3	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	2.2	-	V
Logical Zero Input Voltage	$V_{IL}$	$V_{CC} = 4.5V$	1, 2, 3	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-	0.8	V
Output HIGH Voltage	$V_{OH}$	$I_{OH} = -400\mu A$ $V_{CC} = 4.5V$ (Note 1)	1, 2, 3	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	2.6	-	V
Output LOW Voltage	$V_{OL}$	$I_{OL} = +2.0mA$ $V_{CC} = 4.5V$ (Note 1)	1, 2, 3	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-	0.4	V
Input Leakage Current	$I_I$	$V_{IN} = V_{CC}$ or GND $V_{CC} = 5.5V$	1, 2, 3	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-10	+10	$\mu A$
Output Leakage Current	$I_O$	$V_{OUT} = V_{CC}$ or GND $V_{CC} = 5.5V$	1, 2, 3	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-10	+10	$\mu A$
Clock Input High	$V_{IHC}$	$V_{CC} = 5.5V$	1, 2, 3	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	$V_{CC}-0.8$	-	V
Clock Input Low	$V_{ILC}$	$V_{CC} = 4.5V$	1, 2, 3	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-	0.8	V
Standby Power Supply Current	$I_{CCSB}$	$V_{IN} = V_{CC}$ or GND $V_{CC} = 5.5V$ , Outputs Open	1, 2, 3	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-	500	$\mu A$
Operating Power Supply Current	$I_{CCOP}$	$f = 20.0MHz$ $V_{CC} = 5.5V$ (Note 2)	1, 2, 3	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-	160.0	mA
Functional Test	FT	(Note 3)	7, 8	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-	-	

**NOTES:**

1. Interchanging of force and sense conditions is permitted.
2. Operating Supply Current is proportional to frequency, typical rating is 8.0mA/MHz.
3. Tested as follows:  $f = 1MHz$ ,  $V_{IH} = 2.6$ ,  $V_{IL} = 0.4$ ,  $V_{OH} \geq 1.5V$ ,  $V_{OL} \leq 1.5V$ ,  $V_{IHC} = V_{CC} - 0.4V$ , and  $V_{ILC} = 0.4V$ .

**3**  
1-D FILTERS

# Specifications HSP43881/883

**TABLE 2. HSP43881/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS**

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	-20 (20MHz)		-25 (25.6MHz)		UNITS
					MIN	MAX	MIN	MAX	
Clock Period	T <sub>CP</sub>	Note 1	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	50	-	39	-	ns
Clock Low	T <sub>CL</sub>	Note 1	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	20	-	16	-	ns
Clock High	T <sub>CH</sub>	Note 1	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	20	-	16	-	ns
Input Setup	T <sub>IS</sub>	Note 1	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	20	-	17	-	ns
Input Hold	T <sub>IH</sub>	Note 1	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	0	-	0	-	ns
CLK to Coefficient Output Delay	T <sub>ODC</sub>	Note 1	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	-	24	-	20	ns
Output Enable Delay	T <sub>OED</sub>	Note 1	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	-	20	-	15	ns
CLK to SUM Output Delay	T <sub>ODS</sub>	Note 1	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	-	31	-	25	ns

NOTE: 1. Loading is as specified in the test load circuit with C<sub>L</sub> = 40pF.

**TABLE 3. HSP43881/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	-20		-25		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	C <sub>IN</sub>	V <sub>CC</sub> =Open, f=1MHz All measurements are referenced to device GND.	1	T <sub>A</sub> = +25°C	-	15	-	15	pF
Output Capacitance	C <sub>OUT</sub>		1	T <sub>A</sub> = +25°C	-	15	-	15	pF
Output Disable Delay	T <sub>ODD</sub>		1, 2	-55°C ≤ T <sub>A</sub> ≤ +125°C	-	20	-	15	ns
Output Rise Time	T <sub>OR</sub>		1, 2	-55°C ≤ T <sub>A</sub> ≤ +125°C	-	7	-	6	ns
Output Fall Time	T <sub>OF</sub>		1, 2	-55°C ≤ T <sub>A</sub> ≤ +125°C	-	7	-	6	ns

**NOTES:**

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

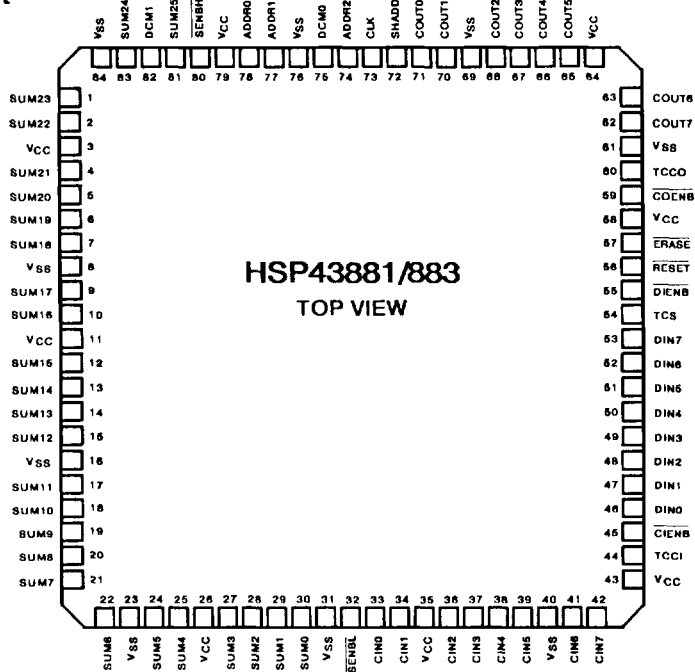
2. Loading is as specified in the test load circuit, C<sub>L</sub> = 40pF.

**TABLE 4. APPLICABLE SUBGROUPS**

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

# HSP43881/883

## Burn-In Circuit



HSP43881/883  
TOP VIEW

QFP LEAD	PIN NAME	BURN-IN SIGNAL	QFP LEAD	PIN NAME	BURN-IN SIGNAL	QFP LEAD	PIN NAME	BURN-IN SIGNAL	QFP LEAD	PIN NAME	BURN-IN SIGNAL
1	SUM23	V <sub>CC</sub> /2	22	SUM6	V <sub>CC</sub> /2	43	V <sub>CC</sub>	V <sub>CC</sub>	64	V <sub>CC</sub>	V <sub>CC</sub>
2	SUM22	V <sub>CC</sub> /2	23	V <sub>SS</sub>	GND	44	TCCI	F9	65	COUT5	V <sub>CC</sub> /2
3	V <sub>CC</sub>	V <sub>CC</sub>	24	SUM5	V <sub>CC</sub> /2	45	CIENB	F10	66	COUT4	V <sub>CC</sub> /2
4	SUM21	V <sub>CC</sub> /2	25	SUM4	V <sub>CC</sub> /2	46	DINO	F0	67	COUT3	V <sub>CC</sub> /2
5	SUM20	V <sub>CC</sub> /2	26	V <sub>CC</sub>	V <sub>CC</sub>	47	DIN1	F1	68	COUT2	V <sub>CC</sub> /2
6	SUM19	V <sub>CC</sub> /2	27	SUM3	V <sub>CC</sub> /2	48	DIN2	F2	69	V <sub>SS</sub>	GND
7	SUM18	V <sub>CC</sub> /2	28	SUM2	V <sub>CC</sub> /2	49	DIN3	F3	70	COUT1	V <sub>CC</sub> /2
8	V <sub>SS</sub>	GND	29	SUM1	V <sub>CC</sub> /2	50	DIN4	F4	71	COUT0	V <sub>CC</sub> /2
9	SUM17	V <sub>CC</sub> /2	30	SUM0	V <sub>CC</sub> /2	51	DIN5	F5	72	SHADD	F9
10	SUM16	V <sub>CC</sub> /2	31	V <sub>SS</sub>	GND	52	DIN6	F6	73	CLK	F0
11	V <sub>CC</sub>	V <sub>CC</sub>	32	SENBL	F10	53	DIN7	F8	74	ADDR2	F2
12	SUM15	V <sub>CC</sub> /2	33	CIN0	F0	54	TCS	F7	75	DCM0	F5
13	SUM14	V <sub>CC</sub> /2	34	CIN1	F1	55	DIENB	F10	76	V <sub>SS</sub>	GND
14	SUM13	V <sub>CC</sub> /2	35	V <sub>CC</sub>	V <sub>CC</sub>	56	RESET	F11	77	ADDR1	F1
15	SUM12	V <sub>CC</sub> /2	36	CIN2	F2	57	ERASE	F10	78	ADDR0	F0
16	V <sub>SS</sub>	GND	37	CIN3	F3	58	V <sub>CC</sub>	V <sub>CC</sub>	79	V <sub>CC</sub>	V <sub>CC</sub>
17	SUM11	V <sub>CC</sub> /2	38	CIN4	F4	59	COENB	F10	80	SENBH	F10
18	SUM10	V <sub>CC</sub> /2	39	CIN5	F5	60	TCCO	V <sub>CC</sub> /2	81	SUM25	V <sub>CC</sub> /2
19	SUM9	V <sub>CC</sub> /2	40	V <sub>SS</sub>	GND	61	V <sub>SS</sub>	GND	82	DCM1	F6
20	SUM8	V <sub>CC</sub> /2	41	CIN6	F6	62	COUT7	V <sub>CC</sub> /2	83	SUM24	V <sub>CC</sub> /2
21	SUM7	V <sub>CC</sub> /2	42	CIN7	F7	63	COUT6	V <sub>CC</sub> /2	84	V <sub>SS</sub>	GND

- NOTES: 1. V<sub>CC</sub>/2 (2.7V ±10%) used for outputs only.  
 2. 47KΩ (±20%) resistor connected to all pins except V<sub>CC</sub> and GND.  
 3. V<sub>CC</sub> = 5.5 ±0.5V.

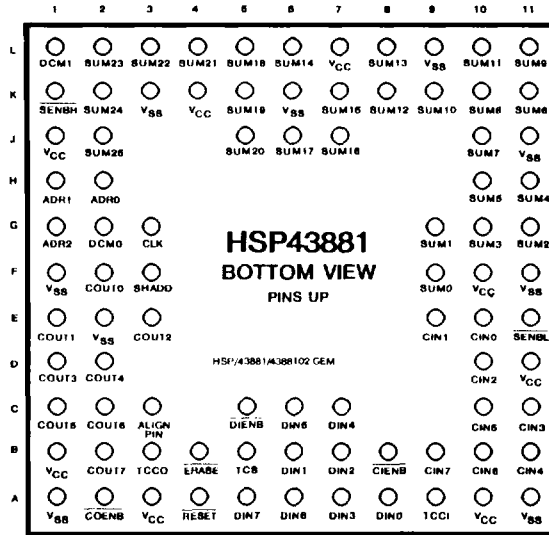
4. 0.1μF (min) capacitor between V<sub>CC</sub> and GND per position.  
 5. F0 = 100KHz ±10%, F1 = F0/2, F2 = F1/2, . . . . ., F11 = F10/2, 40% - 60% Duty Cycle.  
 6. Input voltage limits: V<sub>IL</sub> = 0.8V max, V<sub>IH</sub> = 4.5V ±10%

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1-D FILTERS

# HSP43881/883

## Burn-In Circuit

HSP43881/883 PIN GRID ARRAY (PGA)



PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
A1	VSS	GND	C1	COU5	VCC/2	F10	VCC	VCC	K4	VCC	VCC
A2	COENB	F10	C2	COU6	VCC/2	F11	VSS	GND	K5	SUM19	VCC/2
A3	VCC	VCC	C3	ALIGN	NC	G1	ADR2	F2	K6	VSS	GND
A4	I.ESET	F11	C5	DIENB	F10	G2	DCM0	F5	K7	SUM15	VCC/2
A5	DIN7	F8	C6	DIN5	F5	G3	CLK	F0	K8	SUM12	VCC/2
A6	DIN6	F6	C7	DIN4	F4	G9	SUM1	VCC/2	K9	SUM10	VCC/2
A7	DIN3	F3	C10	CIN5	F5	G10	SUM3	VCC/2	K10	SUM8	VCC/2
A8	DIN0	F0	C11	CIN3	F3	G11	SUM2	VCC/2	K11	SUM6	VCC/2
A9	CIN8/TCCI	F8	D1	COU3	VCC/2	H1	ADR1	F1	L1	DCM1	F6
A10	VCC	VCC	D2	COU4	VCC/2	H2	ADR0	F0	L2	SUM23	VCC/2
A11	VSS	GND	D10	CIN2	F2	H10	SUM5	VCC/2	L3	SUM22	VCC/2
B1	VCC	VCC	D11	VCC	VCC	H11	SUM4	VCC/2	L4	SUM21	VCC/2
B2	COU7	VCC/2	E1	COU1	VCC/2	J1	VCC	VCC	L5	SUM18	VCC/2
B3	COU8/TCC0	VCC/2	E2	VSS	GND	J2	SUM25	VCC/2	L6	SUM14	VCC/2
B4	ERASE	F10	E3	COU2	VCC/2	J5	SUM20	VCC/2	L7	VCC	VCC
B5	DIN8/TCS	F7	E9	CIN1	F1	J8	SUM17	VCC/2	L8	SUM13	VCC/2
B6	DIN1	F1	E10	CIN0	F0	J7	SUM16	VCC/2	L9	VSS	GND
B7	DIN2	F2	E11	SENBL	F10	J10	SUM7	VCC/2	L10	SUM11	VCC/2
B8	CIENB	F10	F1	VSS	GND	J11	VSS	GND	L11	SUM9	VCC/2
B9	CIN7	F7	F2	COU0	VCC/2	K1	SENBH	F10			
B10	CIN6	F6	F3	SHADD	F9	K2	SUM24	VCC/2			
B11	CIN4	F4	F9	SUM0	VCC/2	K3	VSS	GND			

**NOTES:**

- VCC/2 (2.7V ± 10%) used for outputs only.
- 47KΩ (±20%) resistor connected to all pins except VCC and GND.
- VCC = 5.5V ± 0.5V.
- 0.1µF (min) capacitor between VCC and GND per device.
- F0 = 100kHz ± 10%, F1 = F0/2, F2 = F1/2, ..., F11 = F10/2, 40% - 60% Duty Cycle.
- Input voltage Limits: V<sub>IL</sub> = 0.8V Max, V<sub>IH</sub> = 4.5V ± 10%

**Die Characteristics**

**DIE DIMENSIONS:**

328 x 283 x 19 ±1 mils

**METALLIZATION:**

Type: Si-Al or Si-Al-Cu  
Thickness: 8kÅ

**GLASSIVATION:**

Type: Nitrox  
Thickness: 10kÅ

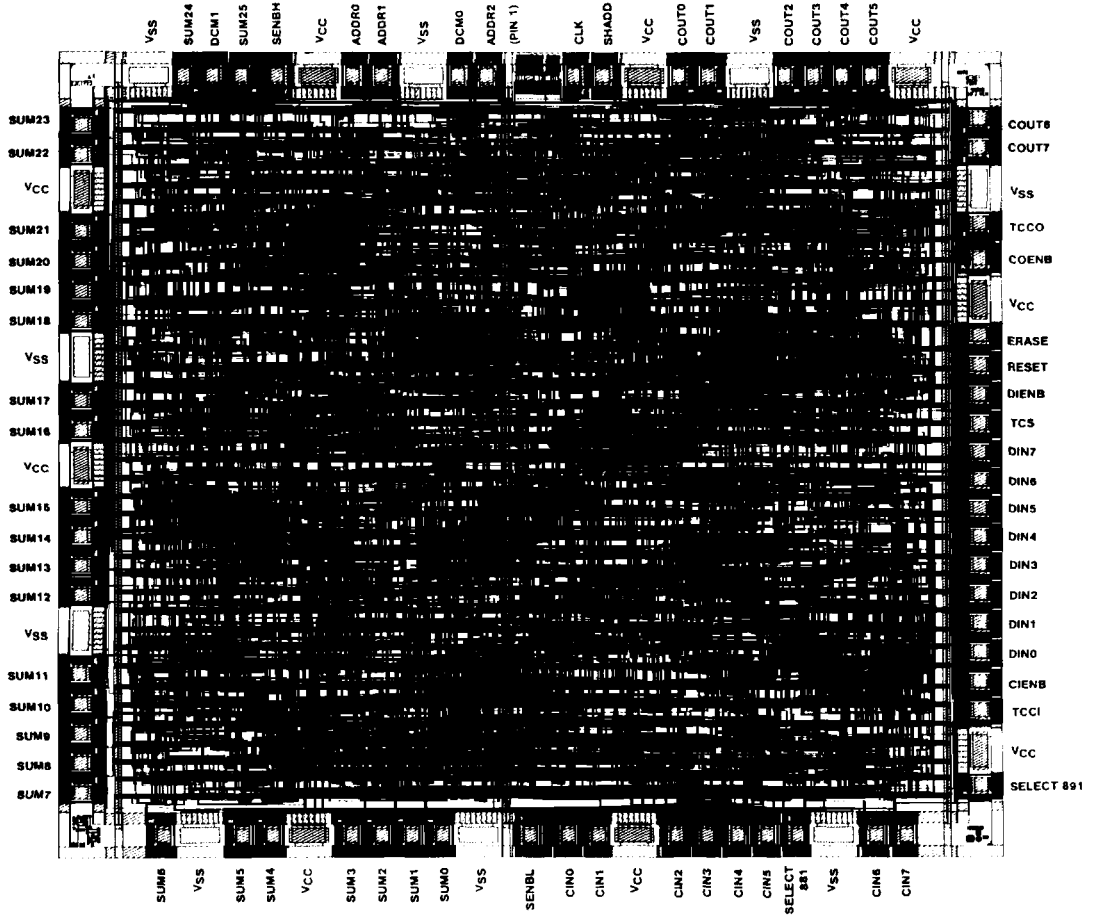
**DIE ATTACH:**

Material: Si-Au Eutectic Alloy (PGA)  
Silver Glass (QFP)

**WORST CASE CURRENT DENSITY:** 1.2 x 10<sup>5</sup>A/cm<sup>2</sup>

**Metallization Mask Layout**

HSP43881/883

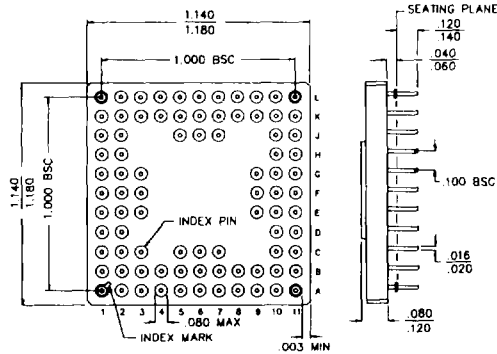


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1-D FILTERS

Packaging†

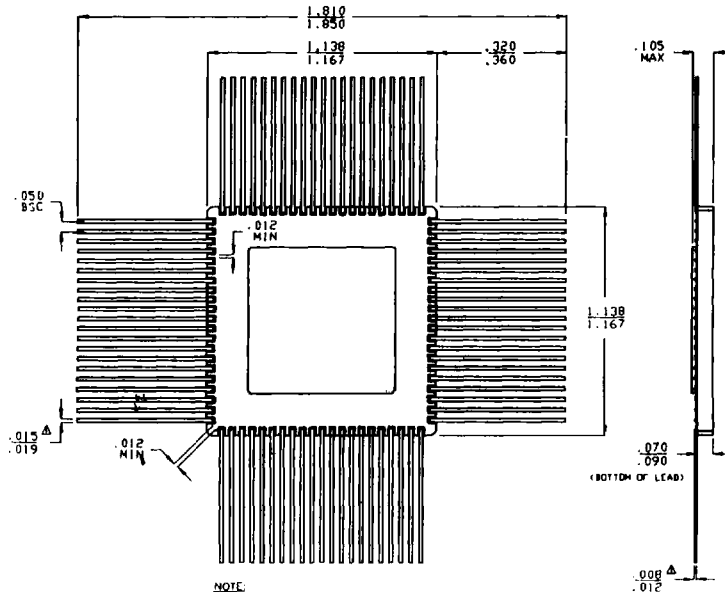
85 PIN CERAMIC PIN GRID ARRAY (PGA)



**LEAD MATERIAL:** Type B  
**LEAD FINISH:** Type C  
**PACKAGE MATERIAL:** Ceramic, 90% Alumina  
**PACKAGE SEAL:**  
 Material: Gold/Tin  
 Temperature: 320°C ± 10°C  
 Method: Furnace Seal

**INTERNAL LEAD WIRE:**  
 Material: Aluminum  
 Diameter: 1.25 Mil  
 Bonding Method: Ultrasonic  
**COMPLIANT OUTLINE:** 38510 P-AC

84 PIN QUAD FLATPACK (QFP)



**LEAD MATERIAL:** Type B  
**LEAD FINISH:** Type C  
**PACKAGE MATERIAL:** Ceramic, 90% Alumina  
**PACKAGE SEAL:**  
 Material: Gold/Tin  
 Temperature: 320°C ± 10°C  
 Method: Furnace Braze

**INTERNAL LEAD WIRE:**  
 Material: Aluminum  
 Diameter: 1.25 Mil  
 Bonding Method: Ultrasonic Wedge  
**COMPLIANT OUTLINE:** 38510 C-G6

NOTE: All Dimensions are  $\frac{\text{Min}}{\text{Max}}$ , Dimensions are in inches.

† Mf-M-38510 Compliant Materials, Finishes, and Dimensions.