1750AE/SOS SINGLE CHIP, 30MHz, ENHANCED SPACE PROCESSOR

FEATURES

- Implements the MIL-STD-1750A Instruction Set Architecture
- Single Chip MIL-STD-1750A Processor
- Form, Fit, and Functionally Compatible with the P1750AE CMOS Processor
- DAIS Instruction Mix Execution Including Floating Point Arithmetic
  - 1.8 MIPS at 20 MHz
  - 2.25 MIPS at 25 MHz
  - 2.7 MIPS at 30 MHz
- BIF Instructions Allow for High Throughput Implementations of Transcedental Functions, Navigational Algorithms, and DSP Functions
- 20, 25 and 30 MHz Operation over the Military Temperature Range (-55 to +125°C)
- Extensive Error, Fault Management and Interrupt Handling Capability. Built in Self Test.
- Two programmable Timers
- 26 User Accessible Registers
- TTL Signal Level Compatible Inputs and Outputs
- Single 5V ± 10% Power Supply
- Multiprocessor and Co-processor Capability
- Available in:
  - 68-Lead Quad Pack (Leaded Chip Carrier)
- Space Radiation Tolerant
  - Absolute latch up immunity
  - Total Dose: > 200K Rad/Si
  - SEU Tolerance
    - $<10^{-10}$ errors per day

GENERAL DESCRIPTION

The P1750AE/SOS is a general purpose, single chip, 16-bit CMOS/SOS microprocessor designed for high performance floating point and integer arithmetic, with extensive real time environment support. It offers a variety of data types, including bits, bytes, 16-bit and 32-bit integers, and 32-bit and 48-bit floating point numbers. It provides 13 addressing modes, including direct, indirect, indexed, based, based indexed and immediate long and short, and it can access 2 MWords of memory.

The P1750AE/SOS offers a well-rounded instruction set with 130 instruction types, including a comprehensive integer, floating point, integer-to-floating point and floating point-to-integer set, a variety of stack manipulation instructions, high level language support instructions such as Compare Between Bounds and Loop Control Instructions. It also offers some unique instructions such as vectored I/O, as well as supports executive and user modes, and provides an escape mechanism which allows user-defined instructions, using a coprocessor.

The chip includes an array of real time application support resources, such as 2 programmable timers, a complete interrupt controller supporting 16 levels of prioritized internal and external interrupts, and a faults and exceptions handler controlling internally and externally generated faults.

The P1750AE/SOS uses a single multiplexed 16-bit parallel bus. Status signals are provided to determine whether the processor is in the memory or I/O bus cycle, reading and writing, and whether the bus cycle is for data or instructions.

The P1750AE/SOS is fabricated using insulated substrate silicon on saphire technology to provide absolute immunity from destructive latch up caused by natural space radiation as well as increased total dose and SEU tolerance.

P1750A, P1750A/SOS, P1750AE, & P1750AE/SOS PROCESSORS

Performance Semiconductor offers four single chip MIL-STD-1750A Processors. Two of these processors, the P1750A and the P1750AE are manufactured with industry standard CMOS Technology. The P1750A/SOS and the P1750AE/SOS are derivatives of the P1750A and P1750AE and are manufactured with insulated substrate Silicon on Sapphire, CMOS/SOS Technology to provide absolute immunity from destructive latch up caused by the exposure of a space vehicle to natural space radiation.

The P1750AE is architecturally more efficient than the P1750A and provides higher throughput at the same clock frequency. All four processors are mechanically interchangeable, they have the same pinouts. The processors are electrically interchangeable as long as the specification limits for the slowest processor in the interchangeability matrix are not violated. All four processors are stand alone, single chip, fully compliant MIL-STD-1750A Processors.

The P1750AE is a second generation MIL-STD-1750A Processor that has been designed as a direct ("plug in") electrical, mechanical, and software compatible replacement for the P1750A. The P1750A and the P1750AE are also proven replacements for other MIL-STD-1750A Processors that are no longer available. The P1750AE has been application proven in a number of critical applications aboard a wide range of platforms including combat aircraft, helicopters, submarines, surface vehicles, and satellites. The P1750AE operates the MIL-STD-1750A Instruction Set in fewer "clocks" than the P1750A. Depending upon the number of arithmetic instructions used, the P1750AE can easily provide more than 3X the throughput of the P1750A at the same clock frequency with the same operational software; see Tables 1 and 2. The P1750A and P1750AE have the same bus cycle. Basic execution instructions such as add/subtract, set/test/reset bit, load & store, byte manipulation, logical OR/NAND/AND, etc. all execute with the same number of "clocks" in both the P1750A and P1750AE. The standard CMOS P1750A and P1750AE are specified by DSCC SMD 5962-87665.

The P1750A/SOS and P1750AE/SOS are derivatives of the P1750A and P1750AE. These SOS processors are targeted for use aboard space vehicles and are manufactured with insulated substrate Silicon on Sapphire (SOS) Technology so as to provide high tolerance to the natural space radiation environment which can degrade or destroy standard CMOS Technology processors. The space radiation tolerance for the P1750AE/SOS is shown in Table 4. The P1750AE/SOS is interchangeable with the P1750A and the P1750AE/SOS is interchangeable with the P1750AE provided that the electrical specifications for the SOS Processor are utilized in the design. Processors manufactured with SOS Technology have higher power requirements and, for some signals, longer delays than the standard CMOS Processors. However, both the CMOS and CMOS/SOS Processors operate the MIL-STD-1750A Instructions with the same number of clocks.

In space, CMOS/SOS provides absolute immunity from destructive Single Event Latchup which can occur when high energy ionizing particles, found naturally in space, enter the space craft when passing through an integrated circuit, there particles introduce enough charge in standard CMOS devices to cause a destructive internal short circuit from the device power supply through the standard CMOS Technology substrate to ground. This latchup current can be more than the integrated circuit can safely carry and the device is either severely weakened reducing its operational life time or is immediately destroyed.

DIFFERENCES BETWEEN THE P1750A AND P1750AE

The P1750AE achieves a 40% boost in performance (in clock cycles) over the P1750A. This reduction in clocks per instruction is because of three architectural enhancements:

1) The inclusion of a 24 x 24 Multiply Accumulate (MAC) array.
2) A reduction in non-bus cycles to 2 clocks (bus cycles remain at 4 clocks to maintain full compatability with the CPU's peripheral chips).
3) Branch calculation logic.

Table 1. P1750A vs. P1750AE # of "Clocks" Required to Execute Selected Instructions

Instruction	P1750A # of Clocks	P1750AE # of Clocks	(1) Throughput Increase
Integer Multiply	23	4	5.75
Compare Between Limits	24	20	1.2
Flt. Point Add/Subtract	28	18	1.56
Flt. Point Multiply	43	9	4.78
Flt. Point Compare	6	4	1.5
Convert Flt. Point To Integer	22	16	1.38
Shift Logical Left/Right	9	6	1.5
Exchange	6	4	1.5
Branch	12	8	1.5

NOTES: (1) Number of P1750A Clocks divided by number of P1750AE Clocks.

Table 2. PACE1750AE BUILT IN FUNCTIONS

A core set of additional instructions has been included in the PACE1750AE. These instructions utilize the Built-in Function (BIF) opcode space. The objective of these new opcodes is to enhance the performance of the 1750AE in critical application areas such as navigation, DSP, transcendentals, and other LINPAK and matrix instructions. Below is a list of the BIFs and their execution times (N = the number of elements in the vector being processed).

Instruction	Mnemonic	Address Mode	Number of Clocks	Notes
Memory Parametric Dot Product - Single	VDPS	4F3(RA)	10+8xN	Interruptable
Memory Parametric Dot Product - Double	VDPD	4F1(RA)	10+16xN	Interruptable
3 x 3 Register Dot Product	R3DP	4F03	6	
Double Precision Multiply Accumulate	MACD	4F02	8	
Polynomial	POLY	4F06	7xN-2	
Clear Accumulator	CLAC	4F00	4	
Store Accumulator (32-Bit)	STA	4F08	7	
Store Accumulator (48-Bit)	STAL	4F04	11	
Load Accumulator (32-Bit)	LAC	4F05	9	
Load Accumulator Long (48-Bit)	LACL	4F07	9	
Move MMU Page Block	MMPG	4F0F	16+8xN	Privileged
Load Timer A Reset Register	LTAR	4F0D	4	
Load Timer B Reset Register	LTBR	4F0E	4	

Table 3.

ABSOLUTE MAXIMUM RATINGS1

Supply Voltage Range	-0.5V to +7.0V
Input Voltage Range	-0.5V to Vcc +0.5V
Storage Temperature Rnage	-65°C to +150°C
Input Current Range	-30mA to +5mA
Voltage applied to Inputs	-0.5V to Vcc +0.5V
Current applied to Output3	150 mA
Maximum Power Dissipation2	1.5W

Notes:

1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

MAXIMUM CONTINUOUS OPERATING RANGE

Case Temperature	GND	Vcc
-55°C to +125°C	0	4.5V to +5.5V

Table 4. SPACE RADIATION TOLLERANCE

Requirement	Specification	Comment
Total Dose (Ionizing Radiation)	≥200 K Rads (Si)	MIL-STD-883 TM1019 Cond. B Processor meets all data sheet specification limits following exposure to ≥ 200K Rad (Si).
Single Event Upset (SEU)	$<10^{-10}$ Errors per day	Adams 90% worst case cosmic Ray environment upset rate calculated with creme.
Single Event Latchup (SEL)	Absolute Immunity	CMOS/SOS Technology eliminates the latchup mechanism.

TABLE 5. DC ELECTRICAL SPECIFICATIONS (Over recommended operating conditions)

Symbol	Parameter		Min	Max	Unit	Conditions[1]	
V_{IH}	Input HIGH Level Voltage		2.0	V_{CC} + 0.5	V		
V_{IL}	Input LOW Level Voltage[2]		–0.5	0.8	V		
V_{CD}	Input Clamp Diode Voltage			–1.2	V	V_{CC} = 4.5V, I_{IN} = –18mA	
V_{OH}	Output HIGH Level Voltage		2.4		V	V_{CC} = 4.5V,	I_{OH} = –8.0mA
			V_{CC} – 0.2		V	V_{CC} = 4.5V,	I_{OH} = –300µA
V_{OL}	Output LOW Level Voltage			0.5	V	V_{CC} = 4.5V,	I_{OL} = 8.0mA
				0.2	V	V_{CC} = 4.5V,	I_{OL} = 300µA
I_{IH1}	Input HIGH Level Current, except $IB_0 – IB_{15}$.			100	µA	$V_{IN} = V_{CC}$, V_{CC} = 5.5V	
I_{IH2}	BUS BUSY, BUS LOCK Input HIGH Level Current, $IB_0 – IB_{15}$.			100	µA	$V_{IN} = V_{CC}$, V_{CC} = 5.5V	
I_{IL1}	BUS BUSY, BUS LOCK Input LOW Level Current, except $IB_0 – IB_{15}$.		-50		µA	V_{IN} = GND, V_{CC} = 5.5V	
I_{IL2}	BUS BUSY, BUS LOCK Input LOW Level Current, $IB_0 – IB_{15}$.		-50		µA	V_{IN} = GND, V_{CC} = 5.5V	
	BUS BUSY, BUS LOCK						
I_{OZH}	Output Three-State Current			50	µA	V_{OUT} = 2.4V, V_{CC} = 5.5V	
I_{OZL}	Output Three-State Current		-50		µA	V_{OUT} = 0.5V, V_{CC} = 5.5V	
I_{CCQC}	Quiescent Power Supply Current (CMOS Input Levels)			25	mA	V_{IN} < 0.2V or < V_{CC} – 0.2V, f = 0MHz, Outputs Open, V_{CC} = 5.5V	
I_{CCQT}	Quiescent Power Supply Current (TTL Input Levels)			100	mA	V_{IN} < 3.4V, f = 0MHz, Outputs Open, V_{CC} = 5.5V	
I_{CCD}	Dynamic Power Supply Current	20MHz		140	mA	V_{CC} = 0V to V_{CC}, tr = tf = 2.5 ns, Outputs Open,	
		25MHz		150	mA		
		30MHz		160	mA	V_{CC} = 5.5V	
I_{OS}	Output Short Circuit Current[3]			-25	mA	V_{OUT} = GND, V_{CC} = 5.5V	
C_{IN}	Input Capacitance			10	pF		
C_{OUT}	Output Capacitance			15	pF		
$C_{I/O}$	Bi-directional Capacitance			15	pF		

Notes

1. 4.5V ≤ V_{CC} ≤ 5.5V, –55°C ≤ T_C ≤ +125°C. Unless otherwise specified, testing shall be conducted at worst-case conditions.
2. V_{IL} = –3.0V for pulse widths less than or equal to 20ns.
3. Duration of the short should not exceed one second; only one output may be shorted at a time.

TABLE 6. SIGNAL PROPAGATION DELAYS[1,2]

Symbol	Parameter	20 MHz		25MHz		30 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$t_{C(BR)L}$	$\overline{\text{BUS REQ}}$		33		30		26	ns
$t_{C(BR)H}$	$\overline{\text{BUS REQ}}$		33		30		26	ns
$t_{BGV(C)}$	$\overline{\text{BUS GNT}}$ setup	5		5		5		ns
$t_{C(BG)X}$	$\overline{\text{BUS GNT}}$ hold	5		5		5		ns
$t_{C(BB)L}$	$\overline{\text{BUS BUSY}}$ LOW		38		33		25	ns
$t_{C(BB)H}$	$\overline{\text{BUS BUSY}}$ HIGH		38		33		25	ns
$t_{BBV(C)}$	$\overline{\text{BUS BUSY}}$ setup	5		5		5		ns
$t_{C(BB)X}$	$\overline{\text{BUS BUSY}}$ hold	5		5		5		ns
$t_{C(BL)L}$	$\overline{\text{BUS LOCK}}$ LOW		38		34		32	ns
$t_{C(BL)H}$	$\overline{\text{BUS LOCK}}$ HIGH		34		30		32	ns
$t_{BLV(C)}$	$\overline{\text{BUS LOCK}}$ setup	5		5		5		ns
$t_{C(BL)X\ (IN)}$	$\overline{\text{BUS LOCK}}$ hold	5		5		5		ns
$t_{C(ST)V}$	D/$\overline{\text{I}}$ Status, AS_0-AS_3, AK_0-AK_3 M/$\overline{\text{IO}}$, R/$\overline{\text{W}}$		32 32		28 28		25 25	ns ns
$t_{C(ST)X}$	M/$\overline{\text{IO}}$, R/$\overline{\text{W}}$, D/$\overline{\text{I}}$ Status, AS_0-AS_3, AK_0-AK_3	0		0		0		ns
$t_{C(SA)H}$	STRBA HIGH		24		20		18	ns
$t_{C(SA)L}$	STRBA LOW		24		20		18	ns
$t_{SAL(IBA)X}$	Address hold from STRBA LOW	5		5		5		ns
$t_{RAV(C)}$	RDYA setup	5		5		5		ns
$t_{C(RA)X}$	RDYA hold	5		5		5		ns
$t_{C(SDW)L}$	$\overline{\text{STRBD}}$ LOW write		24		20		18	ns
$t_{C(SD)H}$	$\overline{\text{STRBD}}$ HIGH		24		20		18	ns
$t_{FC(SDR)L}$	$\overline{\text{STRBD}}$ LOW read		24		20		18	ns
$t_{(SDR)HIBDX}$	$\overline{\text{STRBD}}$ HIGH	0		0		0		ns
$t_{SDWH(IBD)X}$	$\overline{\text{STRBD}}$ HIGH	28		27		25		ns
$t_{SDL(SD)H}$	$\overline{\text{STRBD}}$ write	28		26		24		ns
$t_{RDV(C)}$	RDYD setup	5		5		5		ns
$t_{C(RD)X}$	RDYD hold	5		5		5		ns
$t_{C(IBA)V}$	IB_0-IB_{15}		36		32		28	ns
$t_{FC(IBA)V}$	IB_0-IB_{15}	0		0		0		ns
$t_{IBDRV(C)}$	IB_0-IB_{15} setup	5		5		5		ns
$t_{C(IBD)X}$	IB_0-IB_{15} hold (read)	5		5		5		ns
$t_{C(IBD)X}$	Data valid out (write)	0		0		0		ns

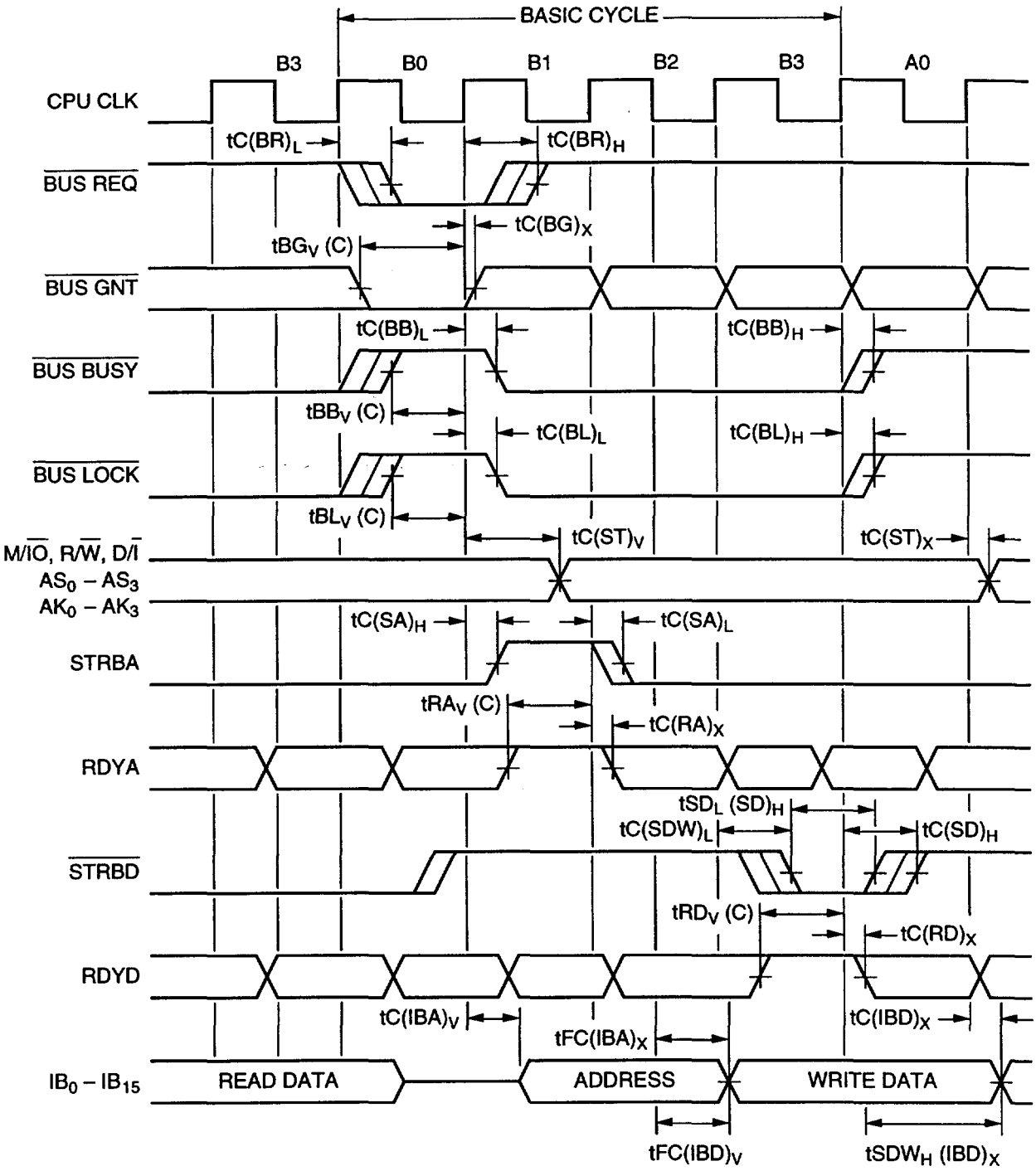
TABLE 6. SIGNAL PROPAGATION DELAYS[1,2] (continued)

Symbol	Parameter	20 MHz		25 MHz		30 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$t_{FC(IBD)V}$	IB_0-IB_{15}		38		34		32	ns
$t_{C(SNW)}$	SNEW		34		30		28	ns
$t_{FC(TGO)}$	TRIGO RST		34		30		28	ns
$t_{RSTL(DMA\ ENL)}$	DMA enable		44		40		38	ns
$t_{C(DME)}$	DMA enable		44		40		38	ns
$t_{FC(NPU)}$	Normal power up		44		40		38	ns
$t_{C(ER)}$	Clock to major error unrecoverable		60		55		52	ns
$t_{RSTL(NPU)}$	$\overline{RESET}$		50		45		40	ns
$t_{REQV(C)}$	Console request	0		0		0		ns
$t_{C(REQ)X}$	Console request	15		15		15		ns
$t_{FV(BB)H}$	Level sensitive faults	5		5		5		ns
$t_{BBH(F)X}$	Level sensitive faults	5		5		5		ns
$t_{IRV(C)}$	IOL_{1-2}INT user interrupt (0-5) setup	0		0		0		ns
$t_{C(IR)X}$	Power down interrupt level sensitive hold	15		15		15		ns
t_{RSTL} (t_{RSTH})	Reset pulse width	25		25		20		ns
$t_{C(XX)Z}$	Clock to three-state		24		20		18	ns
$t_{f(F)}$, $t_{1(1)}$	Edge sensitive pulse width	5		5		5		ns
t_r, t_f	Clock rise and fall		5		4		3	ns

Notes

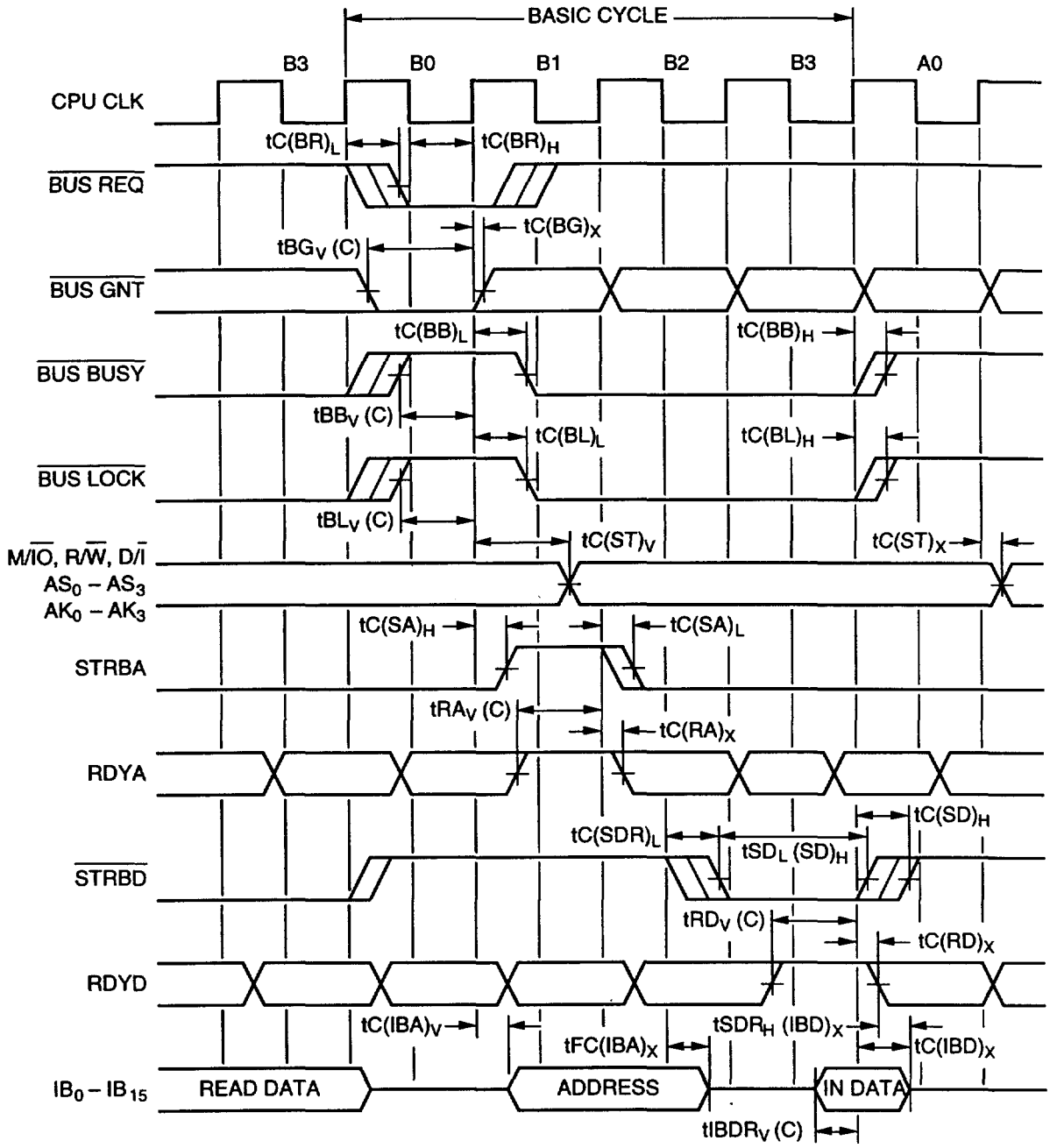
1. $4.5V \le V_{CC} \le 5.5V$, $-55°C \le T_C \le +125°C$. Unless otherwise specified, testing shall be conducted at worst-case conditions.
2. All timing parameters are composed of three elements. The first "t" stands for timing. The second represents the "from" signal. The third in parentheses indicates "to" signal. When the CPU clock is one of the signal elements, either the rising edge "C" or the falling edge "FC" is referenced. When other elements are used, an additional suffix indicates the final logic level of the signal. "L" - low level, "H" - high level, "V" - valid, "Z" - high impedance, "X" - don't care, "LH" - low to high, "ZH" - high impedance to high, "R" - read cycle, and "W" - write cycle.
3. Functional tests shall consist of the same functional test patterns used when testing the equivalent standard CMOS SMD 5962-87665 processor.

MINIMUM WRITE BUS CYCLE TIMING DIAGRAM



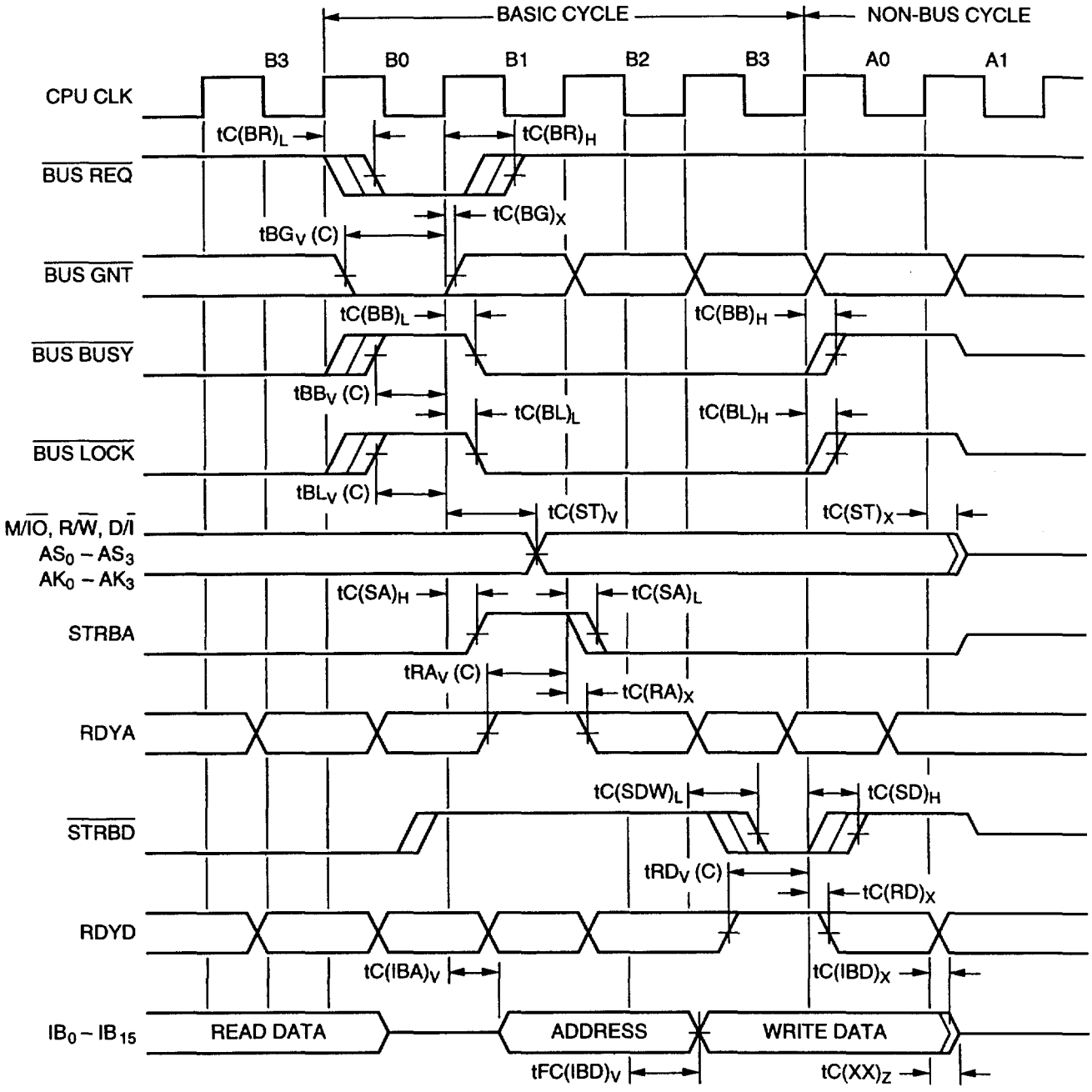
Note:
All time measurements on active signals relate to the 1.5 volt level.

MINIMUM READ BUS CYCLE TIMING DIAGRAM



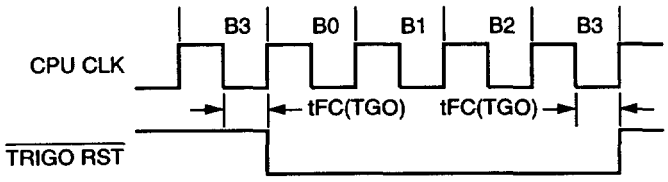
Note:
All time measurements on active signals relate to the 1.5 volt level.

MINIMUM WRITE BUS CYCLE, FOLLOWED BY A NON-BUS CYCLE, TIMING DIAGRAM

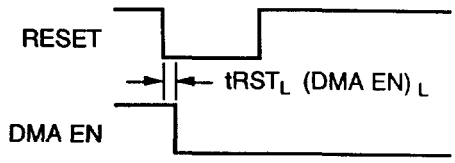


Note:
All time measurements on active signals relate to the 1.5 volt level.

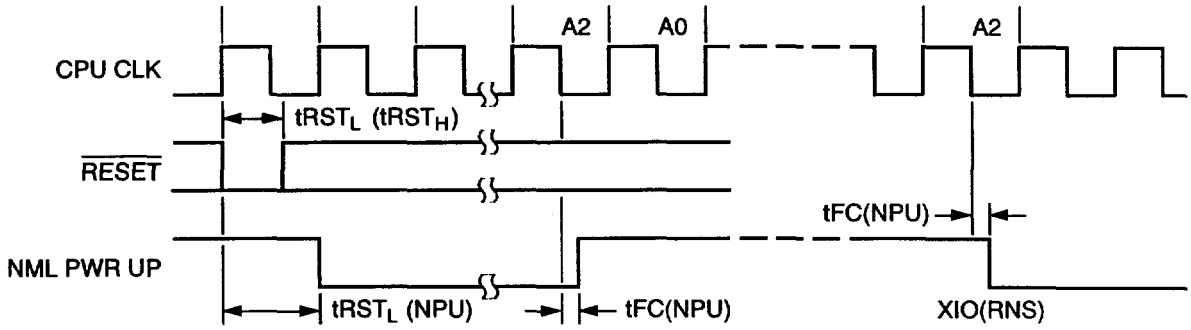
TRIGO RST DISCRETE TIMING DIAGRAM



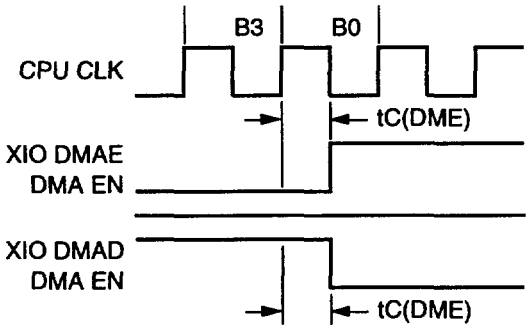
DMA EN DISCRETE TIMING DIAGRAM



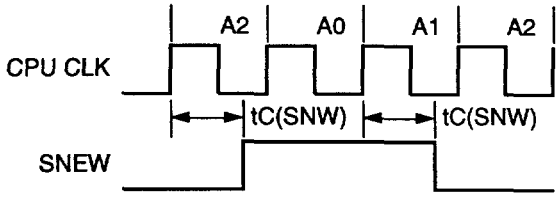
NORMAL POWER UP DISCRETE TIMING DIAGRAM



XIO OPERATIONS



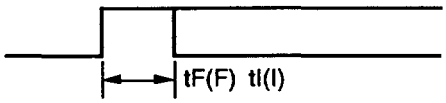
SNEW DISCRETE TIMING DIAGRAM



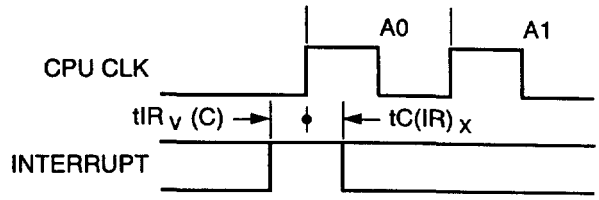
Note:
All time measurements on active signals relate to the 1.5 volt level.

EXTERNAL FAULTS AND INTERRUPTS TIMING DIAGRAM

Edge-sensitive interrupts and faults ($SYSFLT_0$, $SYSFLT_1$) min. pulse width

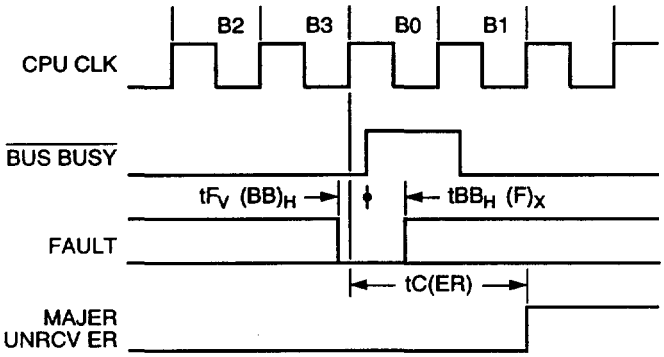


Level-sensitive interrupts



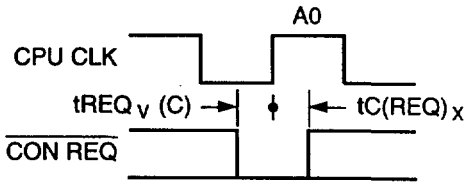
Note:
$tC(IR)_X$ max = 35 clocks

Level-sensitive faults

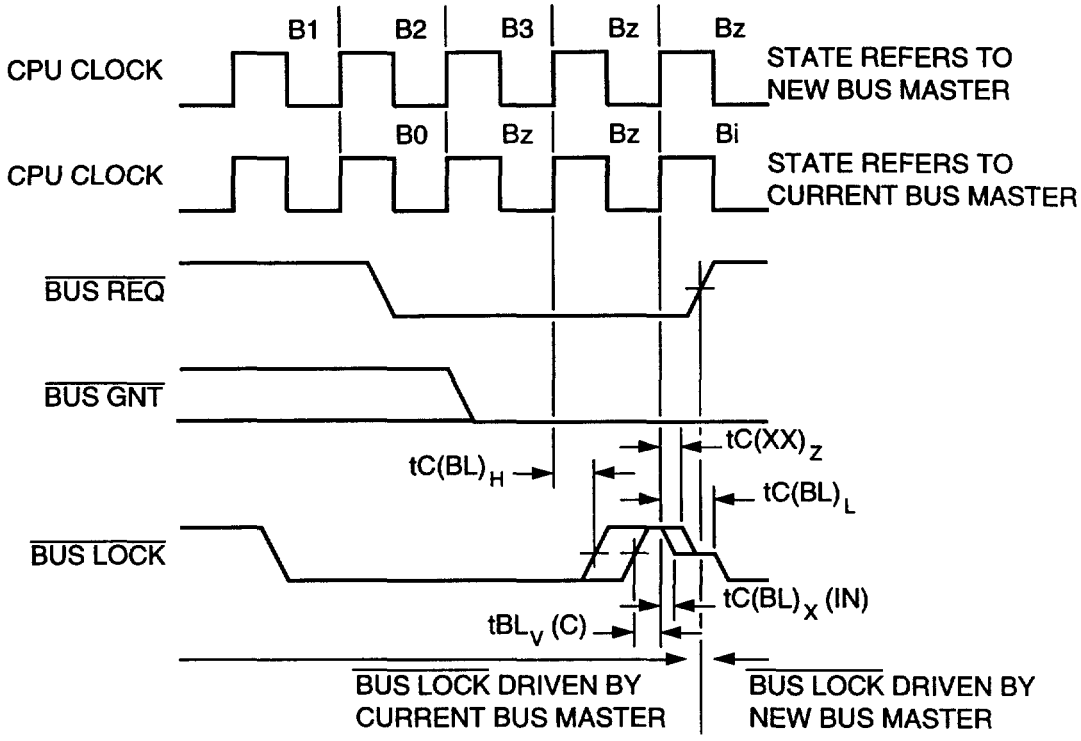


Note:
All time measurements on active signals relate to the 1.5 volt level.

CON REQ



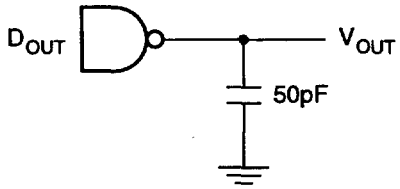
BUS ACQUISITION



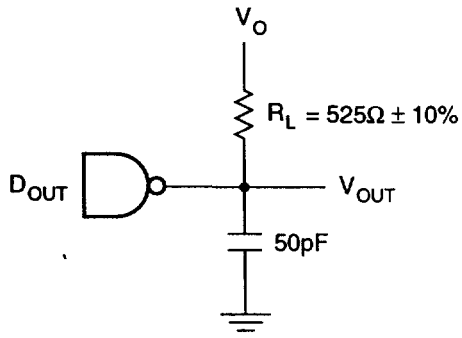
Note:
A CPU contending for the BUS, will assert the $\overline{\text{BUS REQ}}$ line, and will acquire it when $\overline{\text{BUS GNT}}$ is assserted and the BUS is not locked ($\overline{\text{BUS LOCK}}$ is high).

SWITCHING TIME TEST CIRCUITS

Standard Output (Non-Three-State)



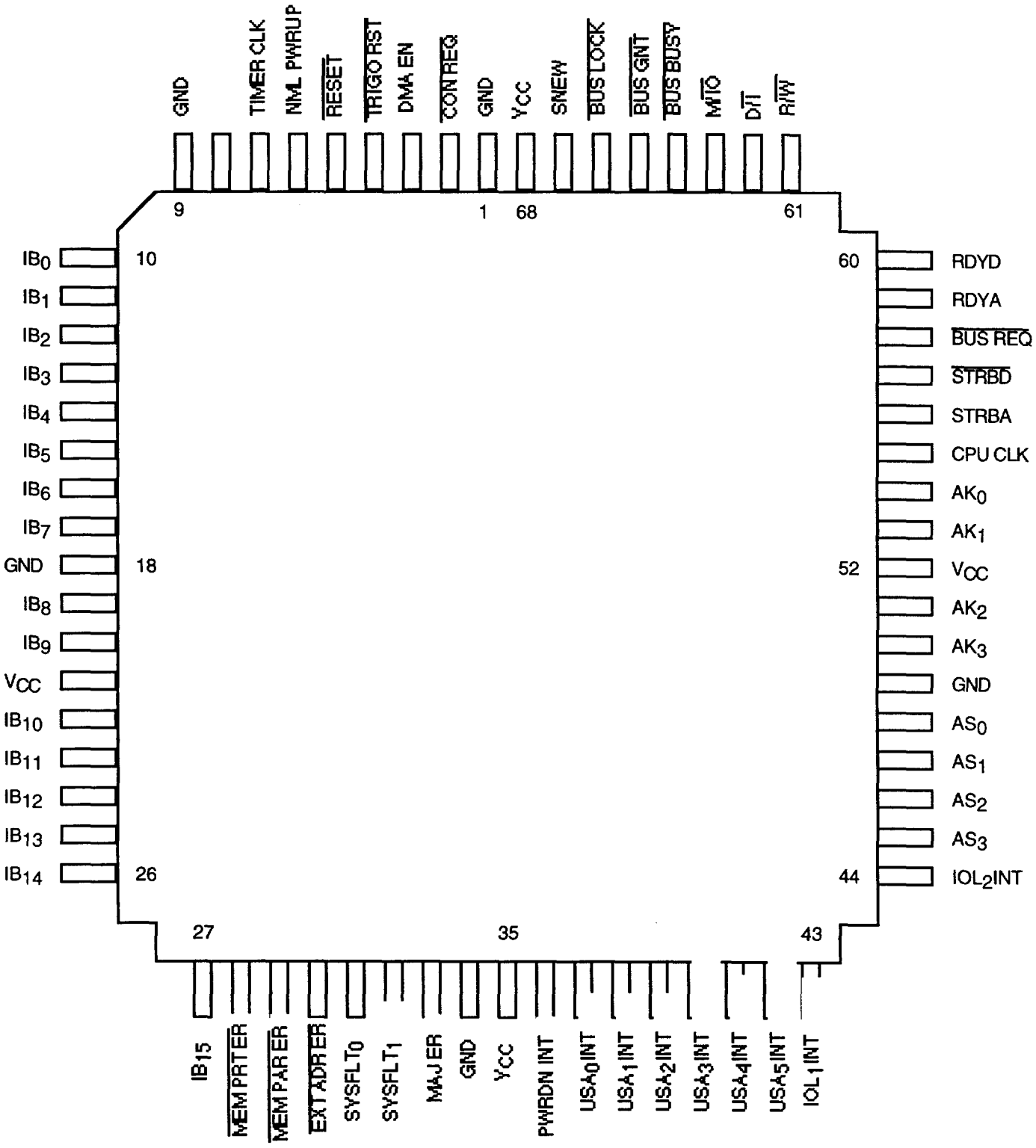
Three-State



Note:
All time measurements on active signals relate to the 1.5 volt level.

Parameter	V0	VMEA
t_{PLZ}	≥ 3V	0.5V
t_{PHZ}	0V	V_{CC} – 0.5V
t_{PXL}	$V_{CC}/2$	1.5V
t_{PXH}	$V_{CC}/2$	1.5V

P1750AE/SOS Terminal Connections
Case Types - QL and QG



SIGNAL DESCRIPTIONS

CLOCKS AND EXTERNAL REQUESTS

Mnemonic	Name	Description
CPU CLK	CPU clock	A single phase input clock signal (0-30 MHz, 40 percent to 60 percent duty cycle.
TIMER CLK	Timer clock	A 100 kHz input that, after synchronization with CPU CLK provides the clock for timer A and timer B. If timers are used, the CPU CLK signal frequency must be > 300 kHz.
$\overline{\text{RESET}}$	Reset	An active low input that initializes the device.
$\overline{\text{CON REQ}}$	Console request	An active low input that initiates console operations after completion of the current instruction.

INTERRUPT INPUTS

Mnemonic	Name	Description
PWRDN INT	Power down interrupt	An interrupt request input that cannot be masked or disabled. This signal is active on the positive going edge or the high level, according to the interrupt mode bit in the configuration register.
USR_0INT - USR_5INT	User interrupt	Interrupt request input signals that are active on the positive going edge or the high level, according to the interrupt mode bit in the configuration register
IOL_1INT IOL_2INT	I/O level interrupts	Active high interrupt request inputs that can be used to expand the number of user interrupts.

FAULTS

Mnemonic	Name	Description
$\overline{\text{MEM PRT ER}}$	Memory protect error	An active low input generated by the MMU or BPU, or both and sampled by the $\overline{\text{BUS BUSY}}$ signal into the Fault Register (bit 0 CPU bus cycle, bit 1 if non-CPU bus cycle).
$\overline{\text{MEM PAR ER}}$	Memory parity error	An active low input sampled by the $\overline{\text{BUS BUSY}}$ signal into bit 2 of the fault register.
$\overline{\text{EXT ADR ER}}$	External address error	An active low input sampled by the $\overline{\text{BUS BUSY}}$ signal into the Fault register (bit 5 or 8), depending on the cycle (memory or I/O).
$SYSFLT_0$ $SYSFLT_1$	System fault $_0$, System fault $_1$,	Asynchronous, positive edge-sensitive inputs that set bit 7 ($SYSFLT_0$) or bits 13 and 15 ($SYSFLT_1$) in the Fault register.

ERROR CONTROL

Mnemonic	Name	Description
UNRCV ER	Unrecoverable error	An active high output that indicates the occurrence of an error classified as unrecoverable.
MAJ ER	Major error	An active high output that indicates the occurrence of an error classified as major.

SIGNAL DESCRIPTIONS (Continued)

BUS CONTROL

Mnemonic	Name	Description
D/$\overline{I}$	Data or instruction	An output signal that indicates whether the current bus cycle access is for Data (high) or Instruction (low). It is three-state during bus cycles not assigned to this CPU. This line can be used as an additional memory address bit for systems that require separate data and program memory.
R/$\overline{W}$	Read or write	An output signal that indicates direction of data flow with respect to the current bus master. A high indicates a read or input operation and a low indicates a write or output operation. The signal is three-state during bus cycles not assigned to this CPU.
M/$\overline{IO}$	Memory or I/O	An output signal that indicates whether the current bus cycle is memory (high) or I/O (low). This signal is three-state during bus cycles not assigned to this CPU.
STRBA	Address strobe	An active high output that can be used to externally latch the memory or I/O address at the high-to-low transition of the strobe. The signal is three-state during bus cycles not assigned to this CPU.
RDYA	Address ready	An active high input that can be used to extend the address phase of a bus cycle. When RDYA is not active wait states are inserted by the device to accommodate slower memory or I/O devices.
$\overline{STRBD}$	Data strobe	An active low output that can be used to strobe data in memory and XIO cycles. This signal is three-state during bus cycles not assigned to this CPU.
RDYD	Data ready	An active high input that extends the data phase of a bus cycle. When RDYD is not active, wait states are inserted by the device to accommodate slower memory or I/O devices.

INFORMATION BUS

Mnemonic	Name	Description
IB_0 - IB_{15}	Information bus	A bidirectional time-multiplexed address/data bus that is three-state during bus cycles not assigned to this CPU. IB0 is the most significant bit.

STATUS BUS

Mnemonic	Name	Description
AK_0 - AK_3	Access key	Outputs used to match the access lock in the MMU for memory accesses (a mismatch will cause the MMU to pull the $\overline{MEM\ PRT\ ER}$ signal low), and also indicates processor state (PS). Privileged instructions can be executed with PS = 0 only. These signals are three-state during bus cycles not assigned to this CPU.
AS_0 - AS_3	Address state	Outputs that select the page register group in the MMU. It is three-state during bus cycles not assigned to this CPU. [These outputs together with D/$\overline{I}$ can be used to expand the device direct addressing space to 4 MBytes, in a nonprotected mode (no MMU)]. However, using this addressing mode may produce situations not specified in MIL-STD-1750A.

SIGNAL DESCRIPTIONS (Continued)

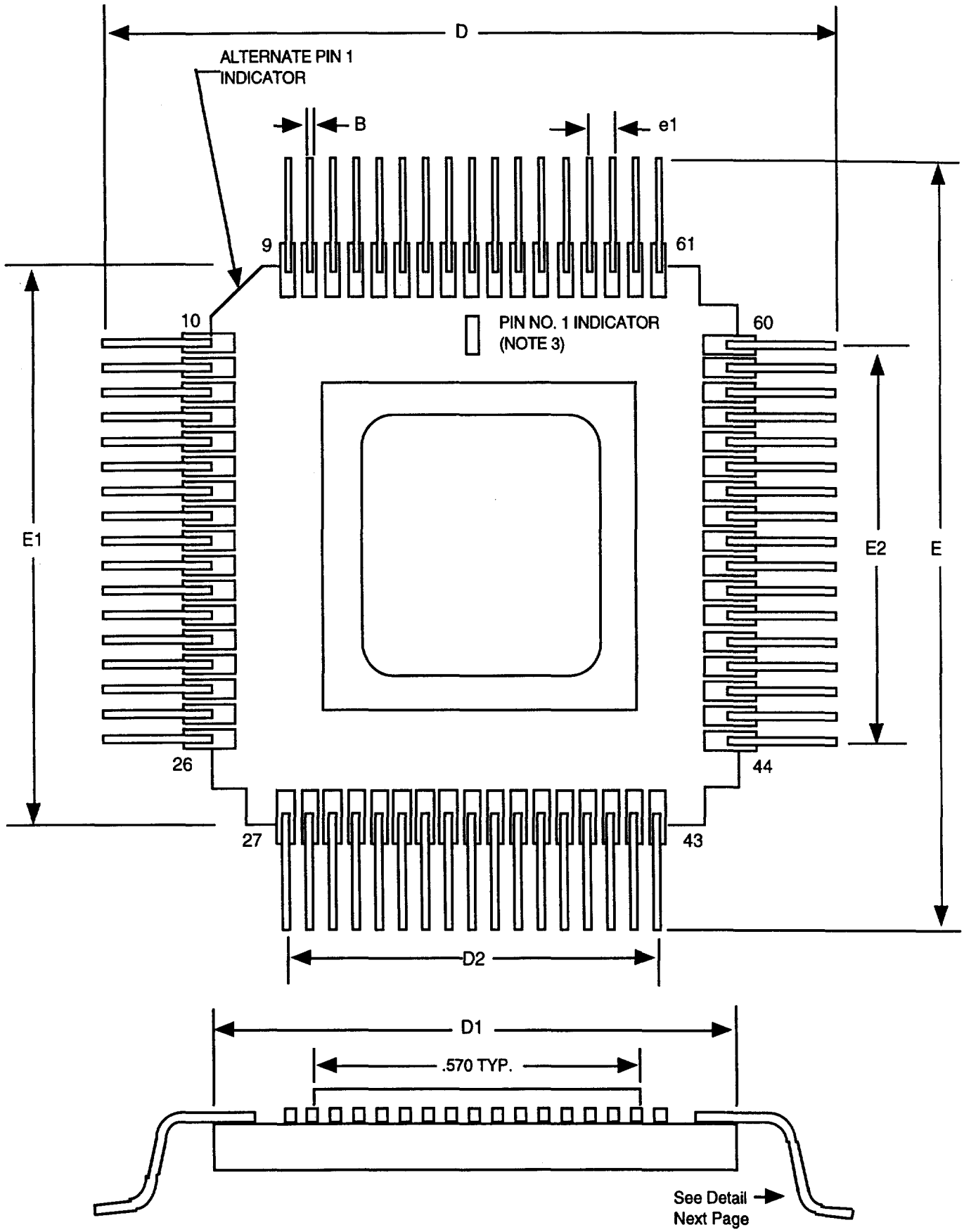
BUS ARBITRATION

Mnemonic	Name	Description
$\overline{\text{BUS REQ}}$	Bus request	An active low output that indicates the CPU requires the bus. It becomes inactive when the CPU has acquired the bus and started the bus cycle.
$\overline{\text{BUS GNT}}$	Bus grant	An active low input from an external arbiter that indicates the CPU currently has the highest priority bus request. If the bus is not used and not locked, the CPU may begin a bus cycle, commencing with the next CPU clock. A high level will hold the CPU in Hi-Z state (Bz), three-stating the IB bus status lines (D/$\overline{\text{I}}$, R/$\overline{\text{W}}$, M/$\overline{\text{IO}}$), strobes (STRBA, $\overline{\text{STRBD}}$), and all the other lines that go three-state when this CPU does not have the bus.
$\overline{\text{BUS BUSY}}$	Bus busy	An active low, bidirectional signal used to establish the beginning and end of a bus cycle. The trailing edge (low-to-high transition) is used for sampling bits into the fault register. It is three-state in bus cycles not assigned to this CPU. However, the CPU monitors the $\overline{\text{BUS BUSY}}$ line for latching non-CPU bus cycle faults into the fault register.
$\overline{\text{BUS LOCK}}$	Bus lock	An active low, bi-directional signal used to lock the bus for successive bus cycles. During non-locked bus cycles, the $\overline{\text{BUS LOCK}}$ signal mimics the $\overline{\text{BUS BUSY}}$ signal. It is three-state during bus cycles not assigned to this CPU. The following instructions will lock the bus: INCM, DECM, SB, RB, TSB, SRM, STUB and STLB.

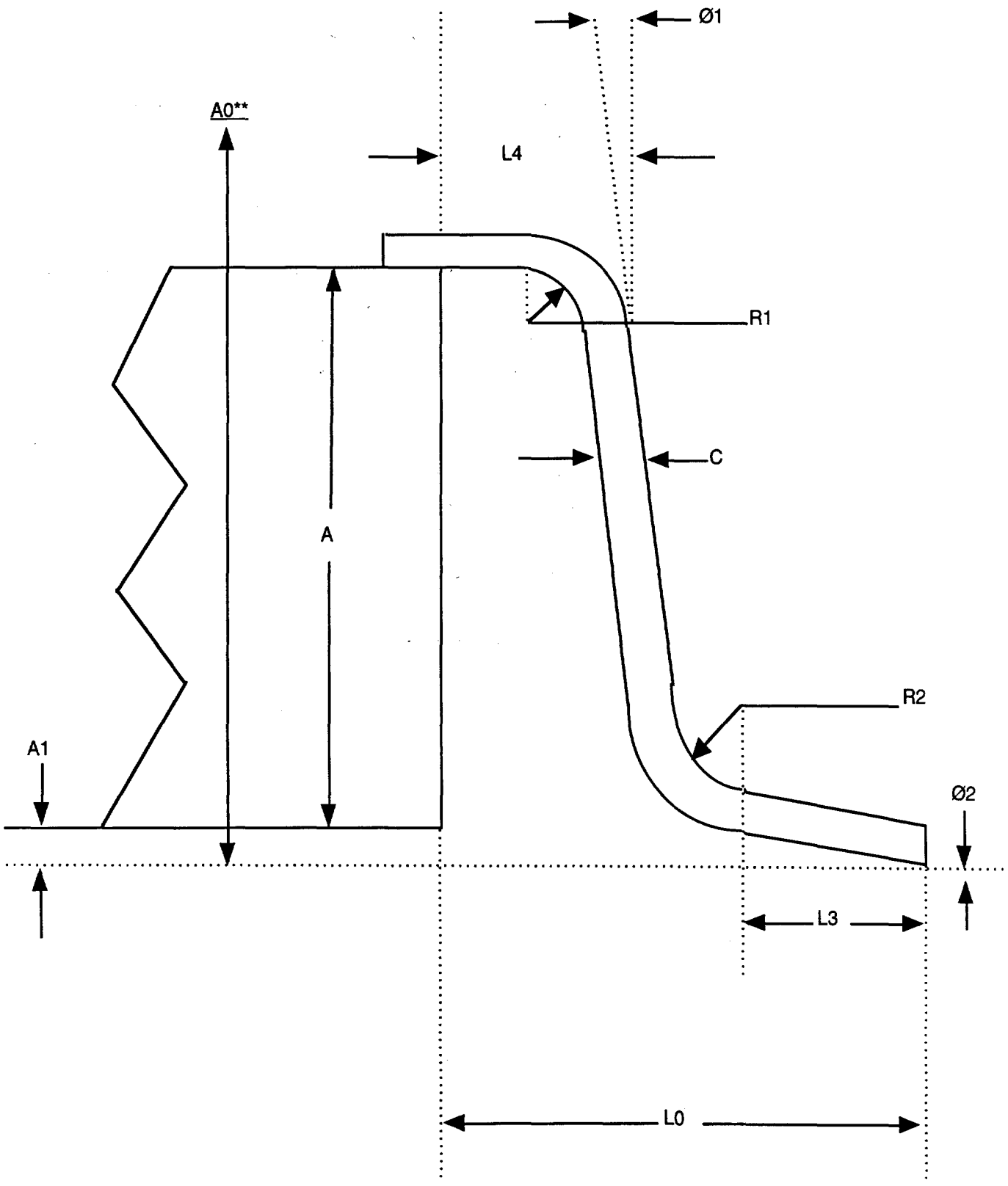
DISCRETE CONTROL

Mnemonic	Name	Description
DMA EN	Direct memory Access enable	An active high output that indicates the DMA is enabled. It is disabled when the CPU is initialized (reset) and can be enabled or disabled under program control (I/O commands DMAE, DMAD).
NML PWRUP	Normal power up	An active high output that is set when the CPU has successfully completed the built-in self test in the initialization sequence. It can be reset by the I/O command RNS.
SNEW	Start new	An active high output that indicates a new instruction is about to start executing in the next cycle.
$\overline{\text{TRIGO RST}}$	Trigger-go reset	An active low discrete output. This signal can be pulsed low under program control I/O address 400B (Hex) and is automatically pulsed during processor initialization.

P1750AE/SOS QG Case Outline



Lead Form Detail



QG Case Outline Dimensions

Drawing & # of Lead (N)	SOS 68 Leads	
	Minimum	Maximum
A	.050	0.090
A1	0.011	0.031
B	0.016	0.021
C	.004	.008
e1	0.050 BSC	
D	1.210	1.250
D1	.945	.965
D2	.800 BSC	
E	1.210	1.250
E1	.945	.965
E2	.800 BSC	
L*	0.270 Nominal	
L0	0.120	.210
L3	0.040	.050
L4	.086	.109
R1	.018	.020
R2	.018	.020
Ø1	4 °	8 °
Ø2	-1 °	7 °
A0**		0.141
Square Lid	.57 Typical per side	

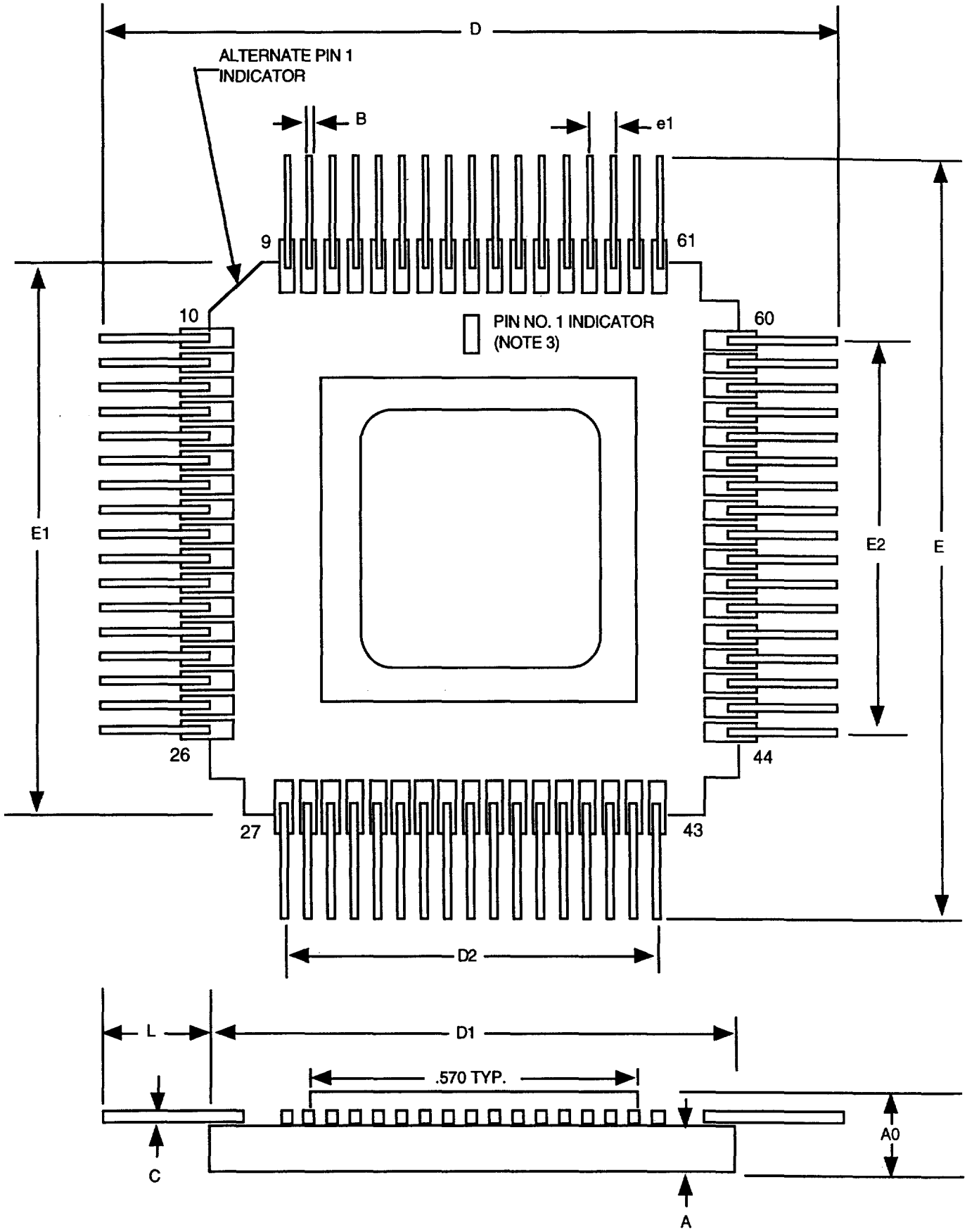
* Lead length in the straight lead configuration, prior to leadforming (used for all test and in-process WIP operations).

** Measured from the highest of the top of the leads or the top of the lid.

NOTES:

1. Dimensions are in inches.
2. Unless otherwise specified, tolerances are .02 (0.51mm) for two place decimals and .005 (0.13mm) for three place decimals.
3. Pin 1: Indicator can be either rectangle, dot, or triangle at specified location or reference to the uniquely beveled corner.
4. Corner indicated as notched may be either notched or square (w/radius).

P1750AE/SOS QL Case Outline



Drawing & # of Lead (N)	SOS 68 Leads	
	Minimum	Maximum
A	.050	0.090
B	0.016	0.021
C	.004	.008
e1	0.050 BSC	
D	1.405	1.505
D1	.945	.965
D2	.800 BSC	
E	1.405	1.505
E1	.945	.965
E2	.800 BSC	
L	0.23	0.27
A0**		0.116
Square Lid	.57 Typical per side	

** Measured from the highest of the top of the leads or the top of the lid.

NOTES:

1. Dimensions are in inches.
2. Unless otherwise specified, tolerances are .02 (0.51mm) for two place decimals and .005 (0.13mm) for three place decimals.
3. Pin 1: Indicator can be either rectangle, dot, or triangle at specified location or reference to the uniquely beveled corner.
4. Corner indicated as notched may be either notched or square (w/radius).

MARKING

Processors will be marked as a minimum with the following:

- Index Point
- Part Number i.e., "P1750AE/SOS-25QGM"
- Performance Semiconductor's Identification
- Date Code
- Country of Origin

MIL-STD-1750A implemented instruction Instruction Type Description MIL-STD-1750A Pg (xxx)	Primary Symbol	Address Modes	Number of clock cycles WO = Wait states instr. fetch 0 1 2 1 2 1 2 WA = Wait states data R/$\overline{W}$ 0 0 0 1 1 2 2	Notes
INTEGER ARITHMETIC AND LOGIC				
Single precision add	A	R	4 5 6 5 6 5 6	
	A	B	10 11 12 12 13 13 14	
	A	BX	10 11 12 12 13 13 14	
	A	ISP	6 7 8 7 8 7 8	
	A	D	12 14 16 15 17 16 18	
	A	DX	12 14 16 15 17 16 18	
	A	IM	8 10 12 10 12 10 12	
(89)				
Double precision add	DA	R	6 6 6 6 6 6 6	
	DA	D	16 18 20 20 22 22 24	
	DA	DX	18 19 20 21 22 23 24	
(94)				
Single precision subtract	S	R	4 5 6 5 6 5 6	
	S	B	10 11 12 12 13 13 14	
	S	BX	10 11 12 12 13 13 14	
	S	ISP	6 7 8 7 8 7 8	
	S	D	12 14 16 15 17 16 18	
	S	DX	12 14 16 15 17 16 18	
	S	IM	8 10 12 10 12 10 12	
(99)				
Double precision subtract	DS	R	6 6 6 6 6 6 6	
	DS	D	16 18 20 20 22 22 24	
	DS	DX	18 19 20 21 22 23 24	
(104)				
Single precision multiply 16-bit product	MS	R	4 5 6 5 6 5 6	
	MS	ISP	6 7 8 7 8 7 13	
	MS	ISN	6 7 8 7 8 7 13	
	MS	D	12 14 16 15 17 16 17	
	MS	DX	12 14 16 15 17 16 17	
	MS	IM	8 10 12 10 12 10 11	
(109)				
Single precision multiply 32-bit product	M	R	5 5 5 5 5 5 5	
	M	B	11 11 11 12 12 13 13	
	M	BX	11 11 11 12 12 13 13	
	M	D	13 14 15 15 16 16 17	
	M	DX	13 14 15 15 16 16 17	
	M	IM	9 10 11 10 11 10 11	
(110)				
Double precision multiply	DM	R	9 9 9 9 9 9 9	
	DM	D	17 19 21 21 23 23 25	
	DM	DX	19 21 23 23 25 25 27	
(111)				

See footnotes at end of list.

MIL-STD-1750A implemented instruction Instruction Type Description MIL-STD-1750A Pg (xxx)	Primary Symbol	Address Modes	Number of clock cycles WO = Wait states instr. fetch 0 1 2 1 2 1 2 WA = Wait states data R/$\overline{W}$ 0 0 0 1 1 2 2	Notes
Single precision divide 16-bit dividend	DV	R	48 48 48 48 48 48 48	
	DV	ISP	50 50 50 50 50 50 50	
	DV	ISN	50 50 50 50 50 50 50	
	DV	D	52 52 52 53 53 54 54	
	DV	DX	54 54 54 55 55 56 56	
(116)	DV	IM	52 53 54 53 54 53 54	
Single precision divide 32-bit dividend	D	R	58 58 58 58 58 58 58	
	D	B	64 65 66 65 66 65 66	
	D	BX	64 65 66 65 66 65 66	
	D	D	62 62 62 63 63 64 64	
	D	DX	64 64 64 65 65 66 66	
(117)	D	IM	62 63 64 63 64 63 64	
Double precision divide	DD	R	88 88 88 88 88 88 88	
	DD	D	96 96 96 98 98 100 100	
(118)	DD	DX	98 98 98 100 100 102 102	
Increment memory by positive integer	INCM	D	16 18 20 20 22 22 24	
(91)	INCM	DX	16 18 20 20 22 22 24	
Decrement memory by positive integer	DECM	D	16 18 20 20 22 22 24	
(101)	DECM	DX	16 18 20 20 22 22 24	
Single precision absolute value	ABS	R	4 5 6 5 6 5 6	Pos. number
(92)	ABS	R	6 6 6 6 6 6 6	Neg. number
Double precision absolute value	DABS	R	6 6 6 6 6 6 6	Pos. number
(93)	DABS	R	8 8 8 8 8 8 8	Neg. number
Single precision negate	NEG	R	4 5 6 5 6 5 6	
(102)				
Double precision negate	DNEG	R	6 6 6 6 6 6 6	
(103)				
Single precision compare	C	R	4 5 6 5 6 5 6	
	C	B	10 11 12 12 13 13 14	
	C	BX	10 11 12 12 13 13 14	
	C	ISP	6 7 8 7 8 7 8	
	C	ISN	6 7 8 7 8 7 8	
	C	D	12 14 16 15 17 16 18	
	C	DX	12 14 16 15 17 16 18	
(132)	C	IM	8 10 12 10 12 10 12	

See footnotes at end of list.

MIL-STD-1750A implemented instruction Instruction Type Description MIL-STD-1750A Pg (xxx)	Primary Symbol	Address Modes	Number of clock cycles WO = Wait states instr. fetch 0 1 2 1 2 1 2 WA = Wait states data R/$\overline{W}$ 0 0 0 1 1 2 2	Notes
Compare between limits (133)	CBL CBL	D DX	20 21 22 23 24 25 26 20 21 22 23 24 25 26	
Double precision compare (134)	DC DC DC	R D DX	4 5 6 5 6 5 6 16 18 20 20 22 22 24 16 18 20 20 22 22 24	
Logical inclusive-OR (122)	OR OR OR OR OR OR	R B BX D DX IM	4 5 6 5 6 5 6 10 11 12 12 13 13 14 10 11 12 12 13 13 14 12 14 16 15 17 16 18 12 14 16 15 17 16 18 8 10 12 10 12 10 12	
Logical exclusive-OR (124)	XOR XOR XOR XOR	R D DX IM	4 5 6 5 6 5 6 12 14 16 15 17 16 18 12 14 16 15 17 16 18 8 10 12 10 12 10 12	
Logical AND (123)	AND AND AND AND AND AND	R B BX D DX IM	4 5 6 5 6 5 6 10 11 12 12 13 13 14 10 11 12 12 13 13 14 12 14 16 15 17 16 18 12 14 16 15 17 16 18 8 10 12 10 12 10 12	
Logical NAND (125)	NAND NAND NAND NAND	R D DX IM	4 5 6 5 6 5 6 12 14 16 15 17 16 18 12 14 16 15 17 16 18 8 10 12 10 12 10 12	
FLOATING POINT ARITHMETIC				
Floating point add (95)	FA FA FA FA FA	R B BX D DX	18 18 18 18 18 18 18 28 28 28 30 30 32 32 28 28 28 30 30 32 32 26 26 26 28 28 30 30 28 28 28 30 30 32 32	
Floating point add extended precision (97)	EFA EFA EFA	R D DX	34 34 34 34 34 34 34 46 46 46 49 49 52 52 48 48 48 51 51 54 54	

See footnotes at end of list.

MIL-STD-1750A implemented instruction Instruction Type Description MIL-STD-1750A Pg (xxx)	Primary Symbol	Address Modes	Number of clock cycles WO = Wait states instr. fetch 0 1 2 1 2 1 2 WA = Wait states data R/$\overline{W}$ 0 0 0 1 1 2 2	Notes
Floating point subtract (105)	FS	R	18 18 18 18 18 18 18	
	FS	B	28 28 28 30 30 32 32	
	FS	BX	28 28 28 30 30 32 32	
	FS	D	26 26 26 28 28 30 30	
	FS	DX	28 28 28 30 30 32 32	
Floating point subtract extended precision (107)	EFS	R	34 34 34 34 34 34 34	
	EFS	D	46 46 46 49 49 52 52	
	EFS	DX	48 48 48 51 51 54 54	
Floating point multiply (112)	FM	R	9 9 9 9 9 9 9	
	FM	B	19 19 19 21 21 23 23	
	FM	BX	19 19 19 21 21 23 23	
	FM	D	17 19 21 21 23 23 25	
	FM	DX	19 21 23 23 25 25 27	
Floating point mulitply extended precision (114)	EFM	R	17 17 17 17 17 17 17	
	EFM	D	29 29 29 32 32 35 35	
	EFM	DX	31 31 31 34 34 37 37	
Floating point divide (119)	FD	R	74 74 74 74 74 74 74	
	FD	B	84 84 84 86 86 88 88	
	FD	BX	84 84 84 86 86 88 88	
	FD	D	82 82 82 84 84 86 86	
	FD	DX	84 84 84 86 86 88 88	
Floating point divide extended precision (121)	EFD	R	122 122 122 122 122 122 122	
	EFD	D	134 134 134 137 137 140 140	
	EFD	DX	136 136 136 139 139 142 142	
Floating point compare (135)	FC	R	4 5 6 5 6 5 6	
	FC	B	14 15 16 17 18 19 20	
	FC	BX	14 15 16 17 18 19 20	
	FC	D	16 18 20 20 22 22 24	
	FC	DX	16 18 20 20 22 22 24	
Floating point compare extended precision (136)	EFC	R	10 10 10 10 10 10 10	
	EFC	D	22 22 24 25 27 28 30	
	EFC	DX	24 24 26 27 29 30 32	
Floating point absolute value (98)	FABS	R	6 6 6 6 6 6 6	Pos. number
	FABS	R	14 14 14 14 14 14 14	Neg. number
Floating point negate (108)	FNEG	R	12 12 12 12 12 12 12	

See footnotes at end of list.

MIL-STD-1750A implemented instruction Instruction Type Description MIL-STD-1750A Pg (xxx)	Primary Symbol	Address Modes	Number of clock cycles WO = Wait states instr. fetch 0 1 2 1 2 1 2 WA = Wait states data R/$\overline{W}$ 0 0 0 1 1 2 2	Notes
Convert floating point to 16-bit integer (126)	FIX	R	14 14 14 14 14 14 14	
Convert 16-bit integer to floating point (127)	FLT	R	10 10 10 10 10 10 10	
Convert floating point extended precision to 32-bit integer (128)	EFIX	R	28 28 28 28 28 28 28	
Convert 32-bit integer to extended precision floating point (129)	EFLT	R	16 16 16 16 16 16 16	
Bit operations				
Set bit (34)	SB	R	4 5 6 5 6 5 6	
	SB	D	12 14 16 15 17 16 18	
	SB	DX	12 14 16 15 17 16 18	
	SB	I	16 18 20 20 22 22 24	
	SB	IX	16 18 20 20 22 22 24	
Reset bit (35)	RB	R	4 5 6 5 6 5 6	
	RB	D	12 14 16 15 17 16 18	
	RB	DX	12 14 16 15 17 16 18	
	RB	I	16 18 20 20 22 22 24	
	RB	IX	16 18 20 20 22 22 24	
Test bit (36)	TB	R	4 5 6 5 6 5 6	
	TB	D	12 14 16 15 17 16 18	
	TB	DX	12 14 16 15 17 16 18	
	TB	I	16 18 20 20 22 22 24	
	TB	IX	16 18 20 20 22 22 24	
Test and set bit (37)	TSB	D	18 20 22 22 24 24 26	
	TSB	DX	18 20 22 22 24 24 26	
Set variable bit (38)	SVBR	R	4 5 6 5 6 5 6	
reset variable bit (39)	RVBR	R	4 5 6 5 6 5 6	
test variable bit (40)	TVBR	R	4 5 6 5 6 5 6	

See footnotes at end of list.

MIL-STD-1750A implemented instruction Instruction Type Description MIL-STD-1750A Pg (xxx)	Primary Symbol	Address Modes	Number of clock cycles WO = Wait states instr. Fetch 0 1 2 1 2 1 2 WA = Wait states data R/$\overline{W}$ 0 0 0 1 1 2 2	Notes
Shift operations				
Shift left logical	SLL	R	6 6 6 6 6 6 6	One shift
	SLL	R	1 1 1 1 1 1 1	Incremental
Shift right logical	SRL	R	6 6 6 6 6 6 6	One shift
	SRL	R	1 1 1 1 1 1 1	Incremental
Shift right	SRA	R	6 6 6 6 6 6 6	One shift
Arithmetic	SRA	R	1 1 1 1 1 1 1	Incremental
Shift left cyclic	SLC	R	6 6 6 6 6 6 6	One shift
	SLC	R	1 1 1 1 1 1 1	Incremental
Double shift left	DSLL	R	10 10 10 10 10 10 10	One shift
Logical	DSLL	R	1 1 1 1 1 1 1	Incremental
Double shift right	DSRL	R	10 10 10 10 10 10 10	One shift
Logical	DSRL	R	1 1 1 1 1 1 1	Incremental
Double shift right	DSRA	R	10 10 10 10 10 10 10	One shift
Arithmetic	DSRA	R	1 1 1 1 1 1 1	Incremental
Double shift left	DSLC	R	10 10 10 10 10 10 10	One shift
Cyclic (41) (42) (43) (44) (45) (46) (47) (48)	DSLC	R	1 1 1 1 1 1 1	Incremental
Shift logical **Count in register**	SLR	R	8 8 8 8 8 8 8	No shift
			10 10 10 10 10 10 10	Right
			1 1 1 1 1 1 1	Incremental
	SLR	R	12 12 12 12 12 12 12	Left
(49)			1 1 1 1 1 1 1	Incremental
Shift arithmetic **count in register**	SAR	R	8 8 8 8 8 8 8	No shift
			10 10 10 10 10 10 10	Right
			1 1 1 1 1 1 1	Incremental
	SAR	R	12 12 12 12 12 12 12	Left
(50)			1 1 1 1 1 1 1	Incremental
Shift cyclic **count in register**	SCR	R	8 8 8 8 8 8 8	No shift
			8 8 8 8 8 8 8	Right
			1 1 1 1 1 1 1	Incremental
	SCR	R	12 12 12 12 12 12 12	Left
(51)			1 1 1 1 1 1 1	Incremental
Double shift **logical count in** **register**	DSLR	R	8 8 8 8 8 8 8	No shift
			14 14 14 14 14 14 14	Right
			1 1 1 1 1 1 1	Incremental
	DSLR	R	16 16 16 16 16 16 16	Left
(52)			1 1 1 1 1 1 1	Incremental

MIL-STD-1750A implemented instruction Instruction Type Description MIL-STD-1750A Pg (xxx)	Primary Symbol	Address Modes	Number of clock cycles WO = Wait states instr. fetch 0 1 2 1 2 1 2 WA = Wait states data R/W 0 0 0 1 1 2 2	Notes
Double shift arthmetic count in register	DSAR	R	8 8 8 8 8 8 8	No shift
			14 14 14 14 14 14 14	Right
			1 1 1 1 1 1 1	Incremental
	DSAR	R	16 16 16 16 16 16 16	Left
(53)			1 1 1 1 1 1 1	Incremental
Double shift cyclic count in register	DSCR	R	8 8 8 8 8 8 8	No shift
			14 14 14 14 14 14 14	Right
			1 1 1 1 1 1 1	Incremental
	DSCR	R	16 16 16 16 16 16 16	Left
(54)			1 1 1 1 1 1 1	Incremental
Load/store/exchange				
Load single precision	L	R	4 5 6 5 6 5 6	
	L	B	10 11 12 12 13 13 14	
	L	BX	10 11 12 12 13 13 14	
	L	ISP	4 5 6 5 6 5 6	
	L	ISN	4 5 6 5 6 5 6	
	L	D	12 14 16 15 17 16 18	
	L	DX	12 14 16 15 17 16 18	
	L	IM	8 10 12 10 12 10 12	
	L	IMX	8 10 12 10 12 10 12	
	L	I	16 18 20 20 22 22 24	
(70)	L	IX	16 18 20 20 22 22 24	
Load double precision	DL	R	6 6 6 6 6 6 6	
	DL	B	14 14 14 16 16 18 18	
	DL	BX	14 14 14 16 16 18 18	
	DL	D	16 18 20 20 22 22 24	
	DL	DX	16 18 20 20 22 22 24	
	DL	I	22 24 26 27 29 30 32	
(72)	DL	IX	22 24 26 27 29 30 32	
Load floating point extended precision	EFL	D	20 22 24 25 27 28 30	
(74)	EFL	DX	20 22 24 25 27 28 30	
Load from upper byte	LUB	D	12 14 16 15 17 16 18	
	LUB	DX	12 14 16 15 17 16 18	
	LUB	I	16 18 20 20 22 22 24	
(75)	LUB	IX	16 18 20 20 22 22 24	
Load from lower byte	LLB	D	12 14 16 15 17 16 18	
	LLB	DX	12 14 16 15 17 16 18	
(76)	LLB	I	16 18 20 20 22 22 24	

See footnotes at end of list.

MIL-STD-1750A implemented instruction Instruction Type Description MIL-STD-1750A Pg (xxx)	Primary Symbol	Address Modes	Number of clock cycles WO = Wait states instr. fetch 0 1 2 1 2 1 2 WA = Wait states data R/$\overline{W}$ 0 0 0 1 1 2 2	Notes
Store	ST	B	10 11 12 12 13 13 14	
single precision	ST	BX	10 11 12 12 13 13 14	
	ST	D	12 14 16 15 17 16 18	
	ST	DX	12 14 16 15 17 16 18	
	ST	I	16 18 20 20 22 22 24	
(78)	ST	IX	16 18 20 20 22 22 24	
Store	STC	D	12 14 16 15 17 16 18	
a positive constant	STC	DX	12 14 16 15 17 16 18	
	STC	I	16 18 20 20 22 22 24	
(79)	STC	IX	16 18 20 20 22 22 24	
Store	DST	B	14 15 16 17 18 19 20	
double precision	DST	BX	14 15 16 17 18 19 20	
	DST	D	16 18 20 20 22 22 24	
	DST	DX	16 18 20 20 22 22 24	
	DST	I	20 22 24 25 27 28 30	
(81)	DST	IX	20 22 24 25 27 28 30	
Store	SRM	D	18 20 22 22 24 24 26	Bus lock
register through	SRM	DX	18 20 22 22 24 24 26	Bus lock
mask (82)				
Store floating	EFST	D	20 22 24 25 27 28 30	
Point extended	EFST	DX	20 22 24 25 27 28 30	
Precision (84)				
Store	STUB	D	16 18 20 20 22 22 24	Bus lock
into upper byte	STUB	DX	16 18 20 20 22 22 24	Bus lock
	STUB	I	20 22 24 25 26 28 30	Bus lock
(85)	STUB	IX	20 22 24 25 26 28 30	Bus lock
Store	STLB	D	16 18 20 20 22 22 24	Bus lock
into lower byte	STLB	DX	16 18 20 20 22 22 24	Bus lock
	STLB	I	20 22 24 25 27 28 30	Bus lock
(86)	STLB	IX	20 22 24 25 27 28 30	Bus lock
Exchange				
Bytes in register	XBR	R	4 5 6 5 6 5 6	
Words in register (130) (131)	XWR	R	4 5 6 5 6 5 6	
Multiple load/store				
Push multiple	PSHM	R	16 17 18 18 19 19 20	One push
registers onto the	PSHM	R	8 8 8 9 9 10 10	Incremental
stack (87)				

See footnotes at end of list.

MIL-STD-1750A implemented instruction Instruction Type Description MIL-STD-1750A Pg (xxx)	Primary Symbol	Address Modes	Number of clock cycles WO = Wait states instr. fetch 0 1 2 1 2 1 2 WA = Wait states data R/$\overline{W}$ 0 0 0 1 1 2 2	Notes
Pop multiple registers off the stack (77)	POPM	R	18 19 20 20 21 21 22	One pop
	POPM	R	10 10 10 11 11 12 12	Incremental
Load multiple registers (73)	LM	D	16 18 20 19 21 20 22	One load
	LM	D	4 4 4 5 5 6 6	Incremental
	LM	DX	16 18 20 19 21 20 22	One load
	LM	DX	4 4 4 5 5 6 6	Incremental
Store multiple registers (83)	STM	D	14 16 18 17 19 18 20	One load
	STM	D	4 4 4 5 5 6 6	Incremental
	STM	DX	14 16 18 17 19 18 20	One load
	STM	DX	4 4 4 5 5 6 6	Incremental
Move multiple words memory-to-memory (80)	MOV	D	8 9 10 9 10 9 10	No move
	MOV	D	24 26 28 27 29 28 30	One move
	MOV	D	8 8 8 10 10 12 12	Incremental
Program control				
Jump on condition (55)	JC	D	8 10 12 10 12 10 12	No jump
	JC	D	8 10 12 10 12 10 12	Jump
	JC	DX	10 12 14 12 14 12 14	No jump
	JC	DX	10 12 14 12 14 12 14	Jump
	JC	I	12 14 16 15 17 16 18	No jump
	JC	I	12 14 16 15 17 16 18	Jump
	JC	IX	14 16 18 17 19 18 20	No jump
	JC	IX	14 16 18 17 19 18 20	Jump
Jump to subroutine (57)	JS	D	10 12 14 12 14 12 14	
	JS	DX	10 12 14 12 14 12 14	
Subtract one and jump (58)	SOJ	D	14 17 20 17 20 17 20	No jump
	SOJ	D	10 11 12 11 12 11 12	Jump
	SOJ	DX	16 19 22 19 22 19 22	No jump
	SOJ	DX	12 13 14 13 14 13 14	Jump
Branch unconditionally (59)	BR	ICR	8 10 12 10 12 10 12	
Branch if equal to zero (60)	BEZ	ICR	4 5 6 5 6 5 6	No branch
	BEZ	ICR	8 10 12 10 12 10 12	Branch
Branch if less than zero (61)	BLT	ICR	4 5 6 5 6 5 6	No branch
	BLT	ICR	8 10 12 10 12 10 12	Branch

See footnotes at end of list.

MIL-STD-1750A implemented instruction Instruction Type Description MIL-STD-1750A Pg (xxx)	Primary Symbol	Address Modes	Number of clock cycles WO = Wait states instr. fetch 0 1 2 1 2 1 2 WA = Wait states data R/$\overline{W}$ 0 0 0 1 1 2 2	Notes
Branch if less than or equal to zero (63)	BLE BLE	ICR ICR	4 5 6 5 6 5 6 8 10 12 10 12 10 12	No branch Branch
Branch if greater than zero (64)	BGT BGT	ICR ICR	4 5 6 5 6 5 6 8 10 12 10 12 10 12	No branch Branch
Branch if not equal to zero (65)	BNZ BNZ	ICR ICR	4 5 6 5 6 5 6 8 10 12 10 12 10 12	No branch Branch
Branch if greater than or equal to zero (66)	BGE BGE	ICR ICR	4 5 6 5 6 5 6 8 10 12 10 12 10 12	No branch Branch
Branch to executive (62)	BEX BEX	S S	71 77 77 88 88 89 89 75 75 75 86 86 97 97	No MMU With MMU
Load status (67)	LST LST LST LST LST LST LST LST	D D DX DX I I IX IX	32 34 36 37 39 40 42 34 36 38 39 41 42 44 32 34 36 37 39 40 42 34 36 38 39 41 42 44 38 40 42 44 46 48 50 40 42 44 46 48 50 52 38 40 42 44 46 48 50 40 42 44 46 48 50 52	No MMU With MMU No MMU With MMU No MMU With MMU No MMU With MMU
Stack IC and jump to subroutine (68)	SJS SJS	D DX	14 16 18 17 19 18 20 14 16 18 17 19 18 20	
Unstack IC and return from subroutine (69)	URS	S	14 16 18 17 19 18 20	
No operation (137)	NOP	S	4 4 4 4 4 4 4	
Break point (138)	BPT	S	14 14 14 14 14 14 14	No console I/O
Built-in function to implement external co-processor (138a)	BIF BIF BIF BIF	D DX I IX	30 31 32 32 33 33 34 30 31 32 32 33 33 34 34 35 36 36 37 37 38 34 35 36 36 37 37 38	

See footnotes at end of list.

MIL-STD-1750A implemented instruction Instruction Type Description MIL-STD-1750A Pg (xxx)	Primary Symbol	Address Modes	Number of clock cycles WO = Wait states instr. fetch 0 1 2 1 2 1 2 WA = Wait states data R/$\overline{W}$ 0 0 0 1 1 2 2	Notes
Execute	XIO	IM	34	Input
input/output	XIO	IMX	34	Input
	XIO	IM	24	Output
	XIO	IMX	24	Output
(29)				
Vectored	VIO	D	70	Overhead-in
input/output	VIO	D	44	Incremental
2/ 3/ 4/	VIO	D	8	Incremental-Unused
	VIO	DX	70	Overhead-in
	VIO	DX	44	Incremental
	VIO	DX	8	Incremental-Unused
	VIO	D	62	Overhead-out
	VIO	D	36	Incremental
	VIO	D	8	Incremental-Unused
	VIO	DX	62	Overhead-out
	VIO	DX	36	Incremental
	VIO	DX	8	Incremental-Unused
(33)				

1. The number of clock cycles required by the CPU is listed as a function of the number of wait states. Both instruction fetch and data read/write wait states of 0, 1, and 2 clock cycles are shown in this list.
2. Overhead-in is the input VIO instruction overhead including one XIO.
3. Incremental is the number of cycles for each additional XIO.
4. Incremental unused is the number of cycles for each unused bit(0) in the vector registar.

Instruction	Mnemonic	Address mode	# of clocks	Notes
Memory parametric dot product - single	VDPS	4F3(RA)	10+(8N)	Interruptable
Memory parametric dot product - double	VDPD	4F1(RA)	10+(16N)	Interruptable
3 X 3 register dot product	R3DP	4F03	6	
Double precision multiply accumulate	MACD	4F02	8	
Polynomial	POLY	4F06	7N-2	
Clear accumulator	CLAC	4F00	4	
Store accumulator (32-bit)	STA	4F08	7	
Store accumulator (48-bit)	STAL	4F04	11	
Load accumulator (32-bit)	LAC	4F05	9	
Load accumulator long (48-bit)	LACL	4F07	9	
Move MMU page block	MMPG	4F0F		Privileged
Load timer A reset register	LTAR	4F0D	4	
Load timer B reset register	LTBR	4FOE	4	

5/ Specific application code may require additional clock cycles due to operand dependencies which are created by the sequence of instructions in the application code. These operand dependent additional clock cycles are not included in 6.1.1 and 6.1.2.

Ordering Information

PART NUMBER	CASE TEMP.	
P1750AE/SOS-20QLC P1750AE/SOS-20QGC	0°C to 70°C 0°C to 70°C	
P1750AE/SOS-25QLC P1750AE/SOS-25QGC	0°C to 70°C 0°C to 70°C	
P1750AE/SOS-30QLC P1750AE/SOS-30QGC	0°C to 70°C 0°C to 70°C	
P1750AE/SOS-20QLI P1750AE/SOS-20QGI	-20°C to +85°C -20°C to +85°C	
P1750AE/SOS-25QLI P1750AE/SOS-25QGI	-20°C to +85°C -20°C to +85°C	
P1750AE/SOS-30QLI P1750AE/SOS-30QGI	-20°C to +85°C -20°C to +85°C	
P1750AE/SOS-20QLM P1750AE/SOS-20QGM	-55°C to +125°C -55°C to +125°C	
P1750AE/SOS-25QLM P1750AE/SOS-25QGM	-55°C to +125°C -55°C to +125°C	
P1750AE/SOS-30QLM P1750AE/SOS-30QGM	-55°C to +125°C -55°C to +125°C	
P1750AE/SOS-20QLMSS P1750AE/SOS-20QGMSS	-55°C to +125°C -55°C to +125°C	SCREENING FOR SPACE APPLICATION PER FLOW SHOWN IN DATA SHEET
P1850AE/SOS 25QLMSS P1750AE/SOS-25QQMSS	-55°C to +125°C -55°C to +125°C	SCREENING FOR SPACE APPLICATION PER FLOW SHOWN IN DATA SHEET
P1850AE/SOS-30QLMSS P1750AE/SOS-30QGMSS	-55°C to +125°C -55°C to +125°C	SCREENING FOR SPACE APPLICATION PER FLOW SHOWN IN DATA SHEET
P1750AE/SOS-20QLMX P1750AE/SOS-20QGMX	-55°C to +125°C -55°C to +125°C	SCREENING PER CUSTOMER'S SPECIAL REQUIREMENTS.
P1750AE/SOS-25QLMX P1750AE/SOS-25QGMX	-55°C to +125°C -55°C to +125°C	SCREENING PER CUSTOMER'S SPECIAL REQUIREMENTS.
P1750AE/SOS-30QLMX P1750AE/SOS-30QGMX	-55°C to +125°C -55°C to +125°C	SCREENING PER CUSTOMER'S SPECIAL REQUIREMENTS.

Screening for SS Grade Product

SCREEN**	TEST CONDITION/CRITERIA OR TEST METHOD PER MIL-STD-883
Water Lot Acceptance	Performance Specification as Alternative to TM5007
SEM (Traceable to Diffusion)	In-Line at Metal One
Wire Bond Pull Monitor	TM2011, condition D, LTPD = 3 on number of leads pulled, 4 units minimum
Die Shear Monitor	TM2019, 2(0)
Nondestructive Bond Pull	Substitute Destructive B.P.; TM2011, Condition D, LTPD=3
Internal Visual Inspection	TM2010
Temperature Cycling	TM1010, Condition C, 10 cycles
Constant Acceleration	TM2001, Y1 orientation, 30Kg
Visual Inspection	TM2009 (partial)
Initial Electrical Test	At Performance's discretion
Marking	Per Data Sheet
Serialization	None.
+25°C Electrical Test	Per Data Sheet Specifications
Burn-In Dynamic	TM1015, Condition D, 240 hours minimum at 125°C
+25°C Electrical Test	Per detail part drawing with datalog of selected parameters Go/no-go per detail part drawing
Percent Defective Allowable	TM5004, para 3.5.1, 5% on subgroup 1 (+25°C DC) Failures
Fine Leak Test	1014, condition A or B
Gross Leak Test	1014, condition C
-55°C and +125°C Electrical Test	Go/no-go per detail Data Sheet Specifications
External Visual Inspection	TM2009
Group A Inspection	TM5005, Table 1, 116/0 or 100%, each lot.
Group B Inspection	TM5005, Table 2B
Group C Inspection	TM5005, Table 3
Group D Inspection	TM5005, Table 4
External Visual Inspection	TM2009 on shippable QCI units

* Group B testing per Table 2B.

* Group C uses alternate sample plan of 5/0 for 3000 hours or 3/0 for 1000 hours once per wafer lot.

* Group D for SOS devices is performed only one time. Generic Group D coverage is maintained on similar non-SOS microprocessor devices.

** To the extent permitted by MIL-STD-883 the sequence of the operations may be modified.