VANTIS

BEYOND PERFORMANCE

Vantis Configuration Memory (VCM) SPROM for Vantis VF1 FPGAs

FEATURES AND BENEFITS

- **Stores configuration patterns for Vantis VF1™ FPGA family**
- **Reprogrammable to reduce costs of design changes and upgrades**
- **1 Mbit capacity holds configuration programs for one or more VF1 FPGAs, reducing the number of VCM devices needed in a system**
- **May be cascaded when configuring multiple VF1 devices**
- **Packaged in a standard 20-pin PLCC for simple implementation**
- **Four-wire interface to VF1 FPGAs simplifies implementation**
- **Output Enable/Reset (OE/RESET) signal is programmable as either RESET high/OE low or OE high/RESET low**
- **Supported by BP and Data I/O SPROM programmers**

DESCRIPTION

Vantis VF1 family FPGAs require a companion SPROM to hold their configuration patterns when they are configured in either Master Serial or Master/Slave Serial mode. The Vantis Configuration Memory (VCM) performs that function.

The VCM is a 1 Mbit non-volatile, reprogrammable SPROM (Figure 1). It consists of a PROM matrix that stores configuration data, an address counter that selects the data to be transferred from the VCM SPROM to the VF1 FPGA, and decode logic that controls the address counter and device outputs. A simple four-wire interface connects the VCM to the VF1. A fifth signal (/CASOUT) allows multiple VCM devices to be cascaded when configuring multiple VF1 devices.

The polarity of the Output Enable/Reset (OE/RESET) signal which resets the internal address counter and enables the device data output may be programmed when the device is loaded with a VF1 configuration program. The default polarity is RESET high, OE low. However, the opposite polarity, OE high, RESET low, is required when the VCM is connected directly to a VF1 device.

VCM SPROMs are supported by BP and Data I/O industry-standard programmers.

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Amendment/**0** Issue Date: **January 1999**

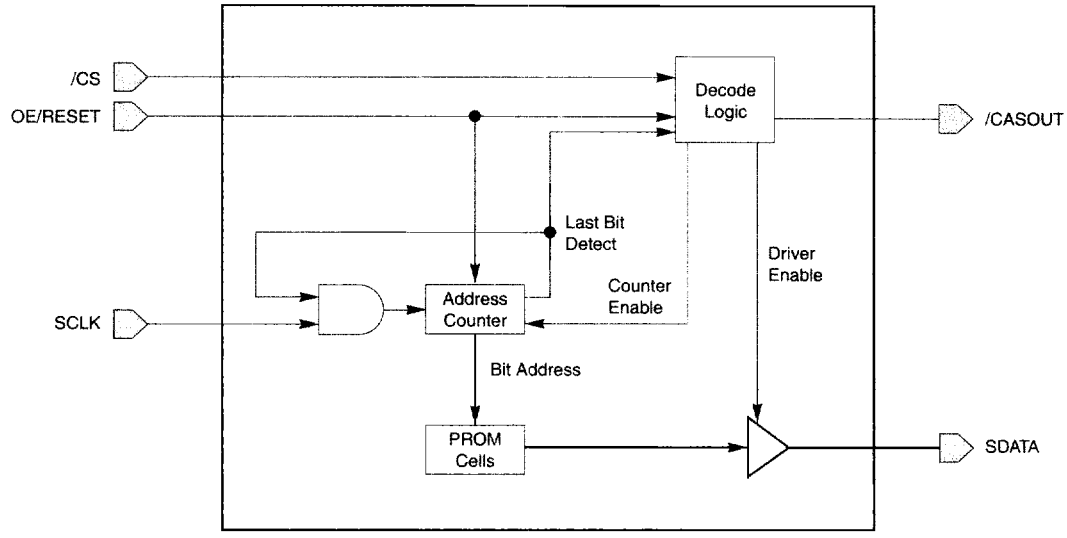


Figure 1. VCM Block Diagram

The VCM's 1 Mbit capacity is sufficient to hold configuration programs for two VF1020 or VF1025 devices, or for four VF1012 devices (Table 1). When multiple VF1 devices must be configured, two or more VCMs may be cascaded to provide the necessary capacity. For example, two VCMs can store the configuration programs for three VF1036 devices.

Table 1. VF1 Device Configuration Bits

VF1 Device	Configuration Bits
VF1012	245,156
VF1020	385,476
VF1025	474,792
VF1036	669,656

Pin configuration

The VCM is housed in a 20-pin PLCC (Figure 2). Table 2 lists pin assignments and signal definitions.

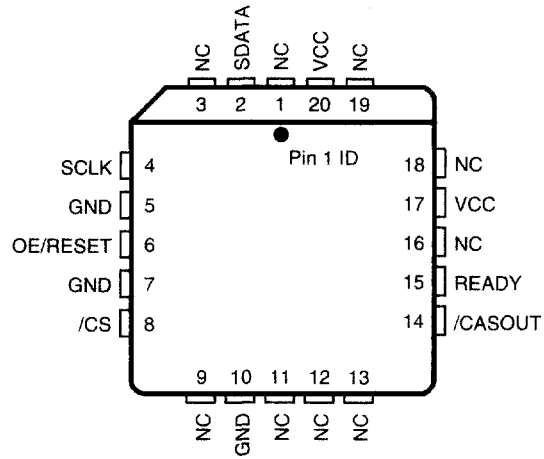


Figure 2. Package Pin Assignments

Table 2. VCM Pin Configuration

Pin Number	Signal Name	I/O	Description
2	SDATA	I/O	Three-state DATA output for reading from the VCM to a VF1 device.
4	SCLK	I	Serial clock input. The clock increments the VCM internal address counter.
5	(GND)		Connect to GND. (Pin is used for programming the VCM device.)
6	OE/RESET	I	VCM reset and output enable. /RESET is active low and OE is active high.
7	(GND)		Connect to GND. (Pin is used for programming the VCM device.)
8	/CS	I	Chip Select input. A Low level on /CS and a high on OE enables the data output driver. A high level on /CS disables both the address counter and forces the device into a low power mode.
10	GND		Ground pin.
14	/CASOUT	O	Cascade Out output. This signal is asserted low on the clock cycle following the last bit read from the memory. It will stay low as long as /CS is low and OE is high. It will then follow /CS until OE goes low. Thereafter, /CASOUT will stay high until the VCM is read again.
15	READY	O	Open collector reset state indicator. Driven low during power-up reset, released when power-up is complete. (Recommend a 4.7KΩ Pull-up on this pin if used).
17	(VCC)	I	Connect to VCC. (Pin is used for programming the VCM device and must be held high during normal operation.)
20	VCC		+3.3V power supply pin.

Master Serial Mode

A simple four-wire interface connects the VF1 FPGA with the VCM SPROM in the Master Serial Mode configuration. The following is a description of the interface between the two devices, with an arrow pointing from the source of a signal to its destination. For example, "**VF1 DONE→VCM /CS**" means that the DONE signal is an output from the VF1 FPGA and drives the /CS input to the VCM. The VF1 signal is on the left (just as the VF1 FPGA is on the left in the block diagram) and the VCM signal is on the right. The single exception is the /PROGRAM signal that starts the configuration process. This signal can originate from a number of sources, as described in the Application Note ***Configuring VF1 FPGAs***.

Refer to Master Serial Mode block diagram and timing diagram (Figure 3). The timing diagram shown in Figure 3 illustrates signal relationships only. Detailed timing is found in the AC Characteristics section of this Data Sheet. (Note: A "/" in front of a signal name identifies a low active signal.)

1. **VF1 /PROGRAM** — A low-to-high transition on the VF1 /PROGRAM pin initiates the configuration sequence.
2. **VF1 DONE → VCM /CS** — When /PROGRAM goes high, the VF1 DONE signal goes low, driving the VCM /CS low. /CS selects the VCM. DONE stays low until the VF1 is fully configured, at which time it goes high to signal the end of the configuration process.
3. **VF1 /INIT → VCM /RESET** — When /PROGRAM goes high, the VF1 /INIT signal goes low, driving the VCM OE/RESET input low. The low on OE/RESET (the /RESET part of the signal) clears the VCM internal address counter to point to data address 0.
4. **VF1 /INIT → VCM OE** — The VF1 /INIT signal remains low until the VF1 device completes its internal initialization cycle. The /INIT signal goes high when the VF1 initialization is complete, driving the VCM OE/RESET input high and providing the OE (output enable) signal to the VCM.
5. **'VF1 DIN ← VCM SDATA** — The VCM output drivers are enabled when OE is high and /CS is low, causing the VCM to place the first bit of its stored configuration program on the SDATA pin for the VF1 to read on its DIN pin.
6. **VF1 CCLK → VCM SCLK** — The VF1 device reads the first configuration bit from its DIN pin and generates a CCLK pulse to signal the VCM (SCLK input) to place the next data bit on its SDATA pin. The VCM internal address counter is incremented on the rising edge of the SCLK input and the VCM places the data bit at the new address on its SDATA pin. This sequence continues until the VF1 device is fully configured or until the last data bit in the VCM has been read.
7. **VF1 DONE → VCM /CS** — In the Master Serial Mode, with only one VF1 device to be configured, a single VCM will hold the complete configuration program. In this case, the VF1 DONE signal terminates the configuration sequence by going high. A high on the VCM /CS input de-selects the VCM. The VCM puts its SDATA output into three-state mode and does not respond to clock inputs on its SCLK pin. The VCM address counter continues to hold whatever address was in the counter when the VCM /CS signal went high.

VF1 signals DONE and /INIT are open-drain signals that require a pull-up resistor, with typical resistor values in the 1K- to 10K-ohm range.

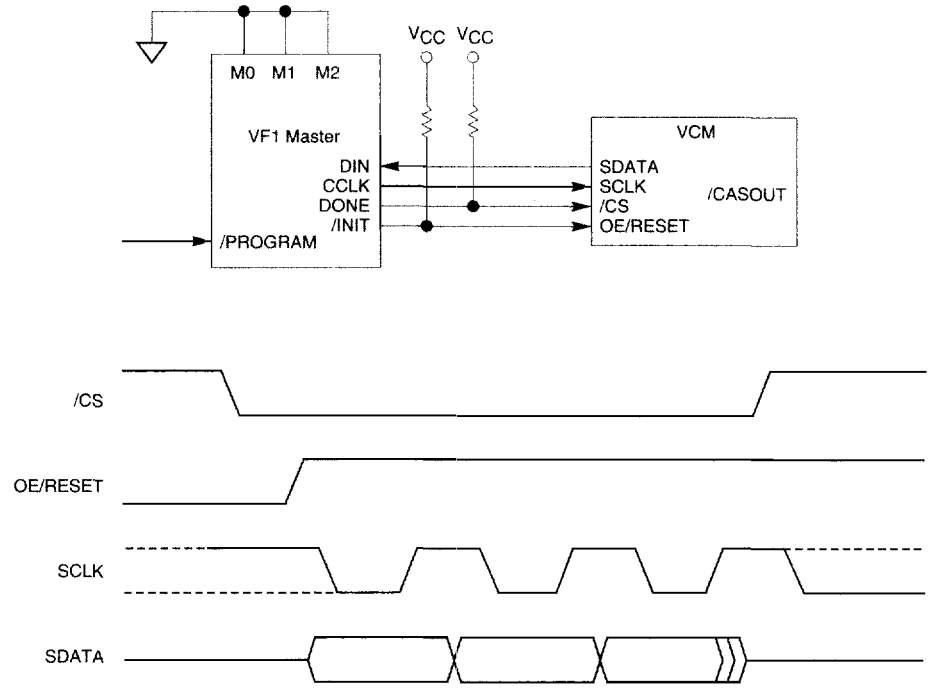


Figure 3. VF1 Master serial mode interface between VF1 FPGA and VCM Configuration Memory

Cascading VCM Devices

The 1 Mbit capacity of the VCM is sufficient to hold the configuration programs for one or more VF1 FPGAs. When configuration programs larger than 1Mbit must be stored, two or more VCM devices may be cascaded to provide the necessary program storage (Figure 4). Figure 4 shows three VF1 FPGAs connected to two VCM SPROMs. The three VF1 FPGAs are arranged in a Master/Slave daisy chain for configuration purposes. (Refer to the Vantis *VF1 FPGA Configuration Guide* for a more detailed description of the Master/Slave configuration mode.)

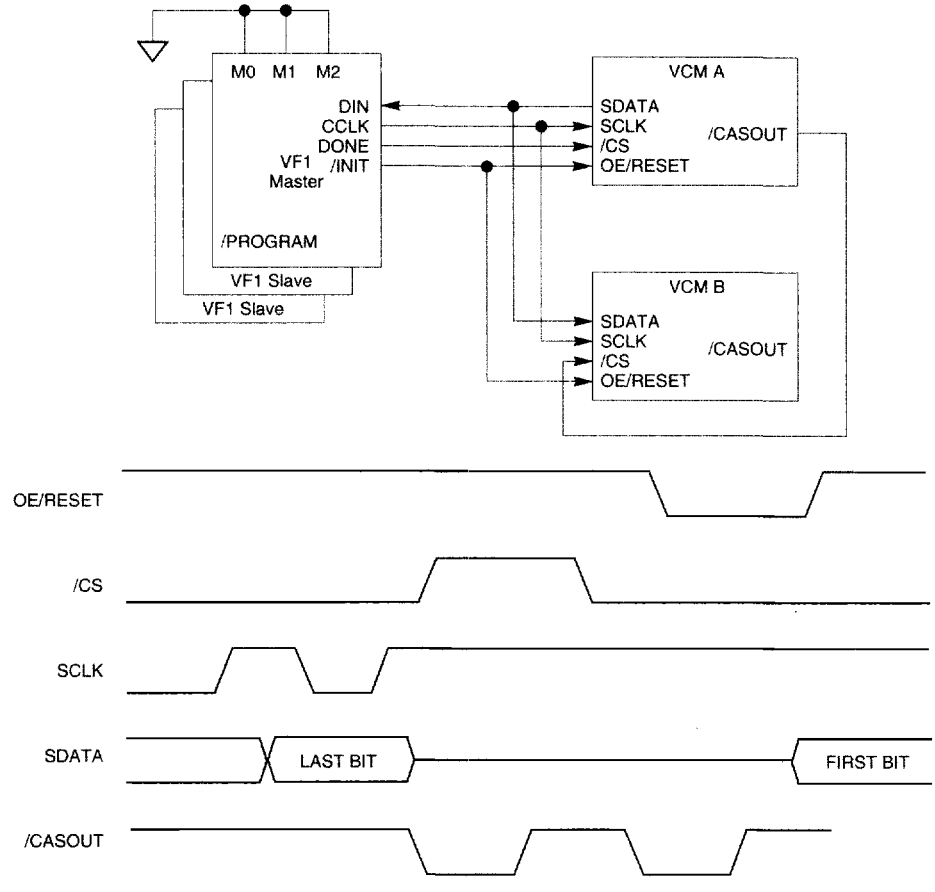


Figure 4. Cascading VCM Configuration Memories

The Master VF1 FPGA controls the configuration process. It generates the clock signal CCLK for loading itself and all other VF1 devices in the serial chain. The Master VF1 interfaces with the VCM devices in much the same manner as a single VF1 interfaces with a single VCM SPROM. The Master VF1 generates CCLK to clock data out of the VCM device and receives the data on its DIN pin. VCM A (Figure 4) puts serial data on its DATA pin until it exhausts its data. At that point, it pulls its /CASOUT signal low, enabling VCM B. At that time, the DATA pin in VCM A goes into three-state mode, and VCM B begins putting its configuration data on the common data line.

Figure 4 shows the interface between a Master VF1 device and two VCM devices and the relative timing of the /CS and /CASOUT signals. The Master/Slave Serial Mode diagram (Figure 5) shows the connections between Master VF1 and Slave VF1 devices. A detailed description of the configuration process follows:

1. **VF1 DIN←VCM A,B SDATA**
   CCLK→SCLK
   /INIT→OE/RESET.

   All VF1 signals with the exception of the DONE signal are connected to both VCM A and VCM B devices in parallel.

2. **DONE→/CS, /CASOUT→/CS.**

   The VCM /CS (chip select) and /CASOUT (cascade out) signals handle the switching from VCM A to VCM B during configuration. When the configuration sequence is started by the VF1 device, the VF1 DONE signal applies a low to the VCM A /CS input as described in Master Serial Mode step 2 above. The VCM A /CASOUT signal is high, applying a high to the VCM B /CS input. VCM B, therefore, is not selected during the early stages of the configuration process: its output drivers are not enabled and it will not respond to clocks on its SCLK input.

3. **VF1 /INIT→ VCM A and VCM B / RESET.**

   When the configuration process is initiated by the VF1 device, the low /RESET signal resets the address counter in both VCM A and VCM B. Note that the VCM B address counter is cleared by the /RESET signal although VCM B is not selected (its /CS input is high).

4. **VF1 /INIT→VCM OE**

   When the VF1 device completes its initialization cycle, its /INIT signal goes high. This applies an OE (output enable) signal to both VCM A and VCM B. VCM A responds to the signal by enabling its output drivers and by placing the first configuration bit in its memory on its SDATA pin. VCM B does not respond because it is not selected (its /CS input is high). Configuration continues as described in steps 5 and 6 of the Master serial mode above until VCM A has transferred all its configuration data.

5. **VCM A /CASOUT→VCM B /CS.**

   When VCM A sends the last bit of its configuration data to the VF1 device(s) it asserts its /CASOUT signal on the next clock cycle following the last bit read from VCM A memory. At the same time, VCM A puts its SDATA output into 3-state mode. The low /CASOUT signal from VCM A enables VCM B by activating its /CS input.

6. **VCM B SDATA→VF 1 DIN.**

   A low on the VCM B /CS input and a high on its OE input enables the VCM B output driver. VCM B places its first configuration bit on its SDATA output for the VF1 device to read. VCM B responds to subsequent clocks on its SCLK input by incrementing its address counter and placing data bits on its SDATA output. This continues until the VF 1 device terminates the configuration process by removing the OE signal (DONE goes high) or until VCM B has transmitted all its configuration data.

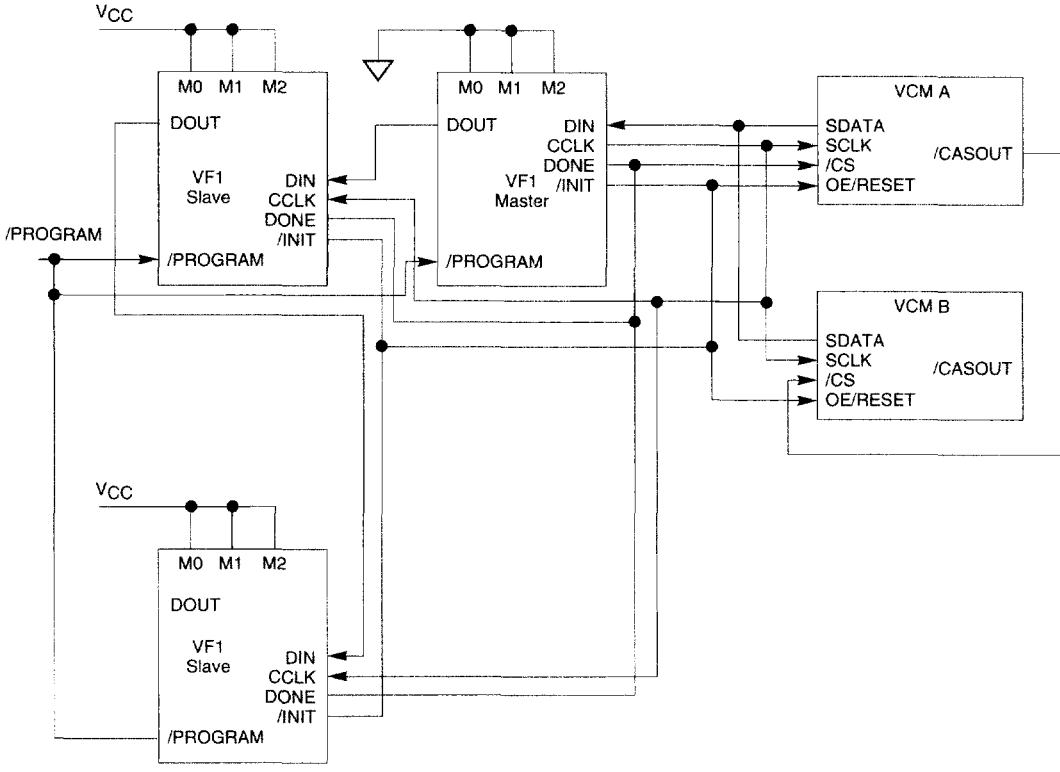


Figure 5. Master/Slave Serial Mode

The /INIT signals from all VF1 devices are tied together and then to the OE/RESET pin of all VCM devices. This ensures that the VCM devices are not enabled until all VF1 devices have completed their initialization sequence. The DONE signals from all VF1 devices are tied together and are connected to the /CS input of VCM A.

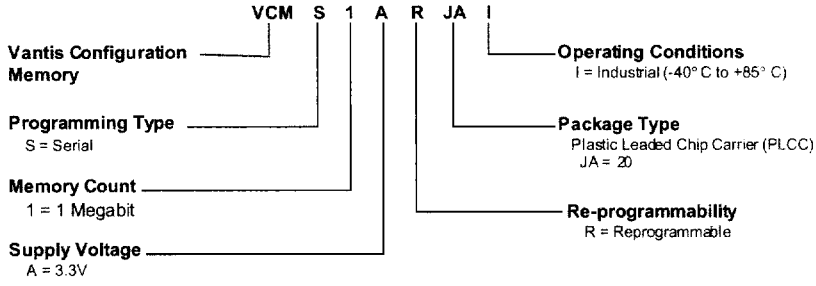
Early in the configuration process, all VF1 devices are loaded with the combined configuration bit count for all VF1 devices in the chain. The VF1 Master device configures itself, and once it is fully configured, it places overflow configuration data on its DOUT (Data Out) pin. That data is received by the first Slave VF1 device on its DIN pin. When the first Slave VF1 device is fully configured, it places subsequent configuration data on its DOUT pin for use by the third VF1 device. This process is used to configure all VF1 devices in the chain.

Each VF1 device counts all CCLK clocks, and when that count matches the configuration bit count that was loaded earlier, its DONE signal goes high. Since all VF1 devices have the same bit count and count the same CCLK clocks, all DONE signals should go high at the same time. When DONE goes high, VCM A sees a high /CS signal and halts the configuration process by driving /CASOUT high. The Master VF1 device also stops generating CCLK clock signals.

Programming VCM Devices

VF1 FPGA configuration programs can be written into VCM configuration memories by industry-standard EEPROM programmers or by test systems during device testing. BP and Data I/O programmers support the VCM device.

VCM Ordering Information



OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (TA) Operating in Free Air.....-40°C to +85°C

Supply Voltage (VCC) with Respect to Ground .....+3.0V to +3.6V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC Characteristics

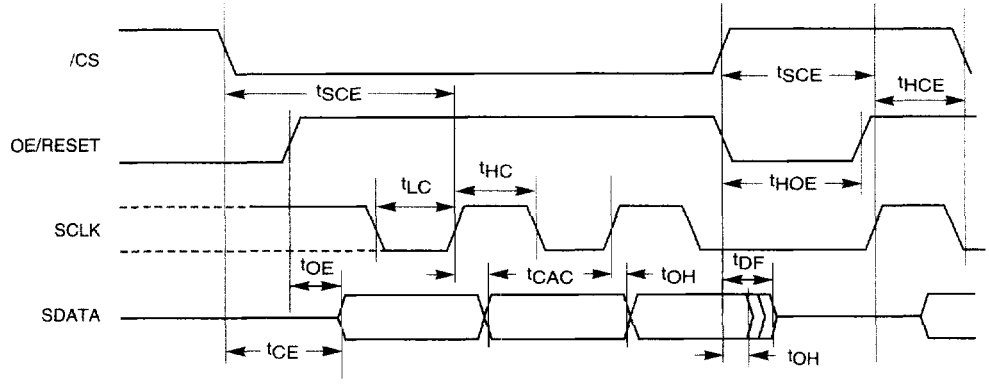
Industrial Grade Parts

V_{CC} = 3.3V ± 10%

Symbol	Parameter	Min	Max	Units
V_{IH}	High-level input voltage	2.0	V_{CC}	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -2.5 mA)	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)		0.4	V
I_{CCA}	Supply current, active mode		5	mA
I_L	Input or Output leakage current (V_{IN} = V_{CC} or GND)	-10	10	µA
I_{CCS}	Supply current, standby mode		100	µA

AC Characteristics in Master Serial Mode

AC Timing

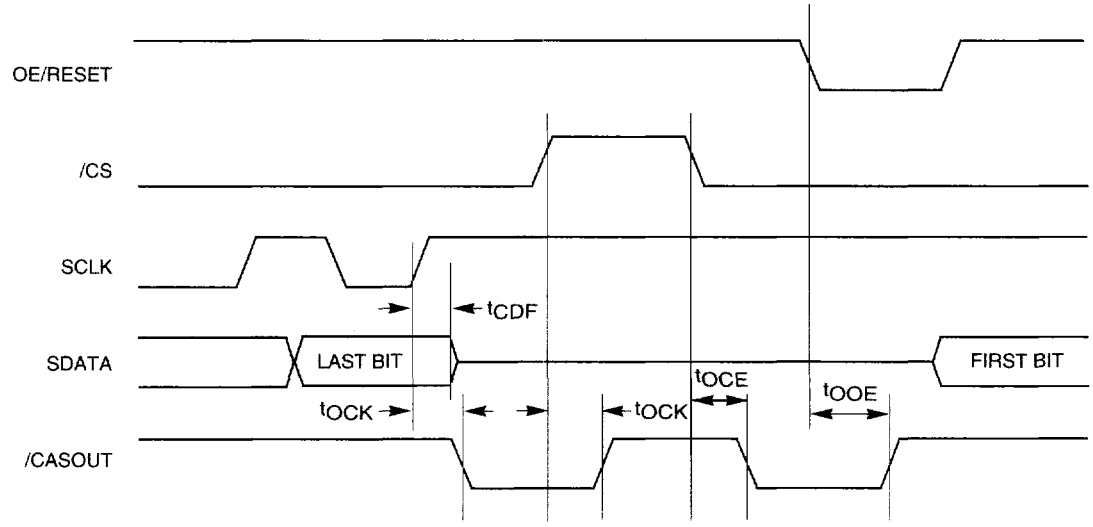


V_{CC}=3.3V ± 10%

Symbol	Description	Min	Max	Units
T_{OE}	OE to Data Delay		30	ns
T_{CE}	/CS to Data Delay		45	ns
T_{CAC}	SCLK to Data Delay		50	ns
T_{OH}	Data hold from /CS, OE, or SCLK	0		ns
T_{DF}	/CS or OE to Data Float Delay		50	ns
T_{LC}	SCLK Low Time	25		ns
T_{HC}	CLK High Time	25		ns
T_{SCE}	/CS Setup Time to SCLK (to ensure proper counting)	30		ns
T_{HCE}	/CS Hold Time to SCLK (to ensure proper counting)	0		ns
T_{HOE}	OE Low Time (to ensure counter is reset)	25		ns
F_{MAX}	Maximum Input Clock Frequency		15	MHz
V_{RDY}	Ready Pin Open Collector Voltage	1.2	2.2	V

AC CHARACTERISTICS WHEN CASCADING

AC Timing when cascading

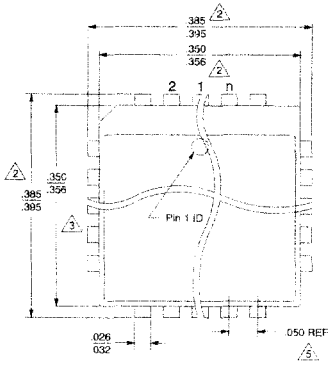


Symbol	Description	Min	Max	Units
T_{CDF} (Note 2)	CLD to Data Float Delay		50	ns
T_{OCK} (Note 1)	SCLK to /CASOUT Delay		50	ns
T_{OCE} (Note 1)	/CS to /CASOUT Delay		35	ns
T_{OOE} (Note 1)	OE/RESET to /CASOUT Delay		35	ns
F_{MAX}	Maximum Input Clock Frequency		12.5	MHz

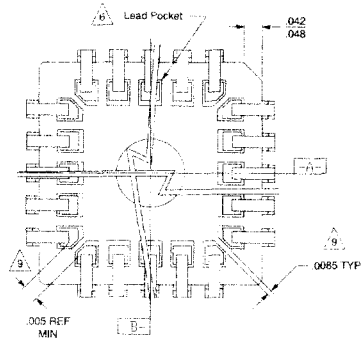
Note:

1. *AC test load = 50 pF.*
2. *Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady state active levels.*

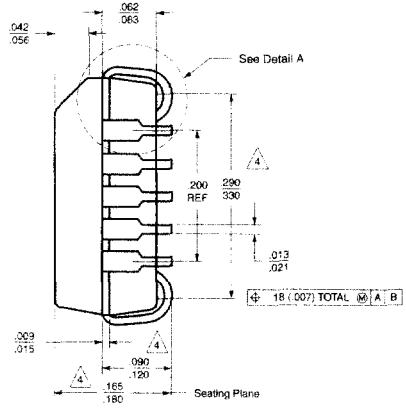
20-PIN PLCC PACKAGE



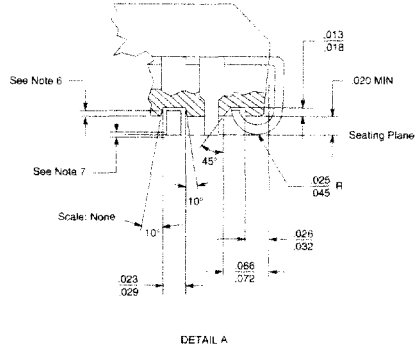
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL A

16-038-SQ_AM
PL 020
EP90
7-22-96 lv

Notes:

1. All Dimensions are in inches.
2. Dimensions "D" and "E" are measured from the outermost point.
3. Dimensions D1 and E1 do not include corner mold flash. Allowable corner mold flash is 0.010 inch.
4. Dimensions "A", "A1", "D2", and "E2" are measured at the points of contact to base plane.
5. Lead spacing as measured from the center-line to the center-line shall be within a ± 0.005 inch.
6. J-bend lead tips should be located inside the "pockets".
7. Lead coplanarity shall be within 0.004 inch as measured from seating plane.
8. Lead tweeze shall be within 0.0045 inch on each side as measured from a vertical flat plane.
9. The lead pocket may be rectangular (as shown) or oval. If corner lead pockets are connected then 0.005-inch minimum lead spacing is required.

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