SL38000-15AH

4-PLL Clock Generator with SSC

Key Features

- REFOUT=25.000MHz
- CLK1=12.000MHz
- CLK2=125.000MHz
- SSCLK1=133.333MHz with +/-0.25% spread option
- SSCLK2=50.000MHz with +0.5% spread option
- VDD=VDDO=3.3V +/-10% power supply
- 25.000MHz external crystal
- Integrated internal voltage regulator
- PD# control function
- OE control function (CLK1 only)
- SSON enable/disable function function for SSCLK1/2
- Programmable CL at XIN and XOUT pins
- Programmable output rise and fall times
- 28-pin TSSOP package with commercial and industrial temperature range available

Applications

- Broadband Home Router
- General Purpose Frequency Synthesising

Description

The SL38000-15AH a fully integrated 4 PLL low power Clock Generator with a Spread Spectrum Clock (SSC) function used for reducing Electromagnetic Interference (EMI) and general purpose frequency synthesizing. The product is designed using SpectraLinear proprietary phase-locked loop (PLL) and SSC technology to synthesize and modulate the input clock. The modulated clock can significantly reduce the measured EMI levels, leading to the compliance with regulatory agency requirements.

SSCLK1 output provides +/-0.25% center-spread and SSCLK2 output +0.5% up-spread. If SSON=1 both spreads are on. Spreads can be turned off (no-spread) if SSON=0.

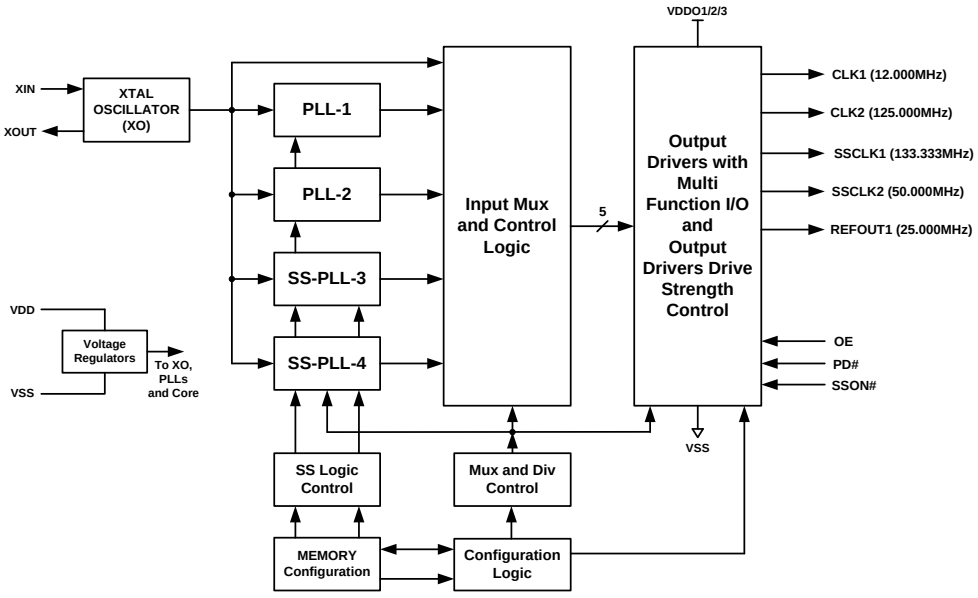
The SL38000-15AH operates from 3.3V power supply.

The product is offered in 28-pin TSSOP package with both commercial and industrial temperature grades available.

Benefits

- Eleminates the need for XOs and Xtals
- EMI Reduction
- Fast time-to-market
- Cost Reduction
- Reduction of PCB layers

Block Diagram



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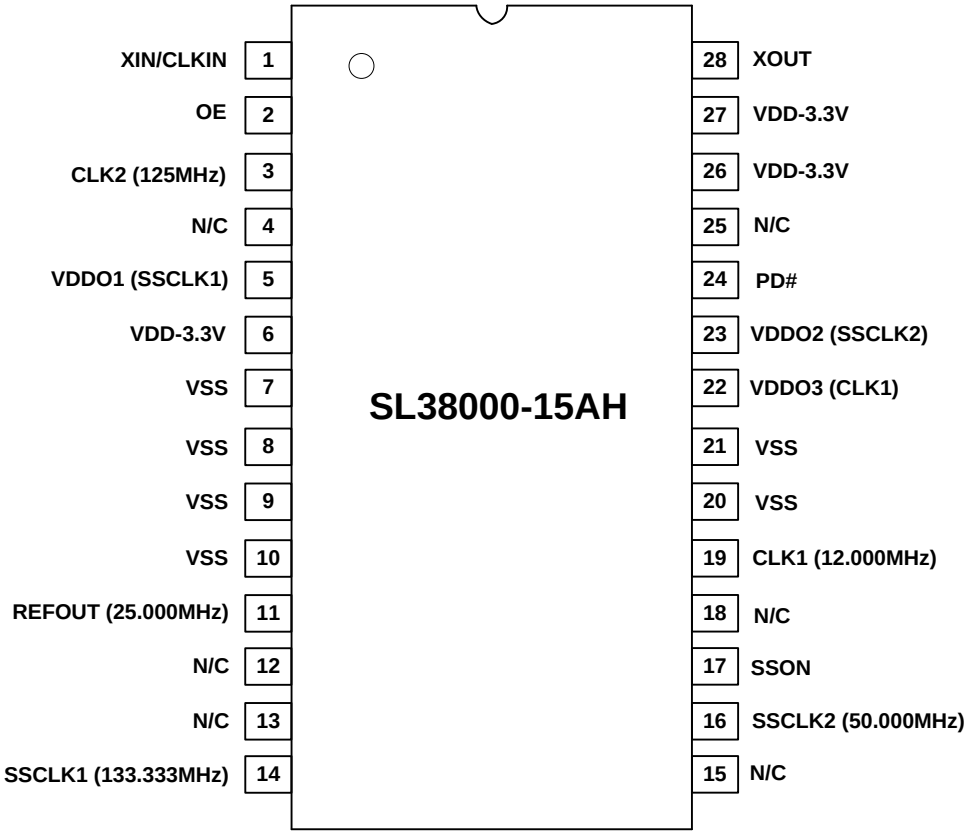
Pin Configuration



28-Pin TSSOP Package

Table 1. SSCLK1 and SSCLK2 versus SSON# Operation

SSON (Pin-17)	SSCLK1 (MHz) (Pin14)	SSCLK1 Spread % (Pin14)	SSCLK2 (MHz) (Pin16)	SSCLK2 Spread % (Pin16)
1	133.333	+/-0.25 (Center Spread)	50.000	+0.5% (Up Spread)
0	133.333	0 (No Spread)	50.000	0 (No Spread)

Table 2. Output Enable (OE) Operation

OE (Pin-2)	Output Control for CLK1 (12.000MHz) Pin-19
1	Clock is Enabled
0	Clock is Disabled (Hi-Z)

Table 3. Power Down (PD#) Operation

PD# (Pin-24)	Device Status
1	Normal Operation
0	Power Down

Pin Description

Pin Number	Pin Name	Pin Type	Pin Description
1	XIN/CLKIN	Input	External crystal oscillator input. XIN=25.000MHz. If crystal with CL=18pF is used no external crystal load capacitors are needed. See Note-2 below.
2	OE	Input	Output enable for CLK1 (12.000MHz) pin. OE=1 CLK1 is enabled. OE=0 CLK1 is disabled. Refer to Table 2. Weakly pulled-up to VDD (200kΩ-typ).
3	CLK2	Output	125.000MHz clock output. No Spread.
4,12,13, 15,18,25	N/C	N/A	No connect (leave these pins floating).
5	VDDO1	Power	Power pin for SSCLK1=133.333MHz. 3.3V+/-10%. Power supply ramp on this pin should be the same as VDD power ramp on pins 6, 26 and 27. See Note-1 below.
6,26,27	VDD	Power	3.3V+/-10%.
7,8,9,10, 20,21	VSS	Power	Power supply ground for VDD and VDDO pins.
11	REFOUT	Output	25.000MHz. (Same as crystal input frequency)
14	SSCLK1	Output	133.333MHz clock output with spread option. Spread is off if SSON=0. Spread is on if SSON=1. Refer to Table 1.
16	SSCLK2	Output	50.000MHz clock output with spread option. Spread is off if SSON=0. Spread is on if SSON=1. Refer to Table 1.
17	SSON	Input	Spread control pin for SSCLK1 (133.333MHz) and SSCLK2 (50.000MHz) clocks. If SSON=1 spread is on. If SSON=0 spread is 0% (no spread). Refer to Table 1 for spread % values. Weakly pulled-down to VSS (200kΩ-typ). SSON is powered by VDDO3 and SSON=1=VDDO3=2.5V.
19	CLK1	Output	12.000MHz clock output. No Spread.
22	VDDO3	Power	Power pin for CLK1=12.000MHz. 3.3V+/-10%. Power supply ramp on this pin should be the same as VDD power ramp on pins 6, 26 and 27. See Note-1 below.
23	VDDO2	Power	Power pin for SSCLK2=50.000MHz. 3.3V+/-10%. Power supply ramp on this pin should be the same as VDD power ramp on pins 6, 26 and 27. See Note-1 below.
24	PD#	Input	Power down control pin. PD#=1 is normal operation. Device is turned off if PD#=0. Refer to Table 3. Weakly pulled-up to VDD (200kΩ-typ).
28	XOUT	Output	External crystal output. If crystal with CL=18pF is used no external crystal load capacitors are needed. See Note-2 below.

Note-1: VDDO≤VDD at all times or all VDD and VDDO pins must be connected to same common VDD power supply.

Note-2: Xin and Xout pin capacitances are programmed as 34pF. Including 2pF parasitic PCB capacitances at each pin, the total capacitance value becomes 36pF. If a crystal with 18pF is used, no external capacitance is required since these capacitance values matches the crystal CL=18pF requirement for nominal +/-0ppm crystal accuracy.

Absolute Maximum Ratings

Description	Condition	Min	Max	Unit
Supply voltage, VDD	VDD	-0.5	4.1	V
Supply voltage, VDDO	VDDO≤VDD	-	VDD	V
All Inputs and Outputs		-0.5	VDD+0.5	V
Ambient Operating Temperature	In operation, C-Grade	0	70	°C
Ambient Operating Temperature	In operation, I-Grade	-40	85	°C
Storage Temperature	No power is applied	-65	150	°C
Junction Temperature	In operation, power is applied	-	125	°C
Soldering Temperature		-	260	°C
ESD Rating (Human Body Model)	JEDEC22-A114D	-3,000	3,000	V
ESD Rating (Machine Model)	JEDEC22-A115D	-200	200	V

DC Electrical Characteristics (C-Grade)

Unless otherwise stated VDD=VDDO==3.3V+/-10%, CL=15pF and Ambient Temperature range 0 to +70Deg C

Description	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	VDD+/-10%	2.97	3.3	3.63	V
Operating Voltage	VDDO	VDDO1/2/3, VDDO≤VDD	2.97	3.3	3.63	V
Input Low Voltage	VIL	CMOS Level, PD#, OE, SSON	0	-	0.3VDD	V
Input High Voltage	VIH	CMOS Level, Pins programmed as PD#, OE or SSON	0.7VDD	-	VDD	V
Output High Voltage	VOH1	IOH=-4mA , REFOUT and CLK1/2, SSCLK1/2 if VDDO=VDD	VDD-0.5	-	-	V
Output Low Voltage	VOL1	IOL=4mA , REFOUT, CLK1/2, SSCLK1/2	-	-	0.5	V
Input High Current	IIH	VIN=VDD, Pins 2, 3 and 24	-50	-	50	µA
Input Low Current	IIL	VIN=GND, Pins 2, 3 and 24	-50	-	50	µA
Pull-up or Down Resistors	RPU/D	Pins 2, 3 and 24	-	200	-	kΩ
Operating Supply Current	IDD	Xin=25.000MHz and all 5 clocks are active and CL=0, VDD=3.3V	-	28	38	mA
Standby Current	ISBC	PD#=GND	-	650	-	µA
Output Leakage Current	IOL	OE=GND at CLKOUT pins	-10	-	10	µA
Input Capacitance	Cin Cout	Pins 1 and 28 (On-chip CXin and CXout pin capacitances)	-	34	-	pF
Input Capacitance	CIN2	Pins 2, 17 and 24 (OE, SSON and PD#)	-	4	6	pF
Load Capacitance	CL	All CLKOUT outputs	-	-	15	pF

AC Electrical Characteristics (C-Grade)

Unless otherwise stated VDD=VDDO=3.3V+/-10%, CL=15pF and Ambient Temperature range 0 to +70 Deg C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Frequency Range	FIN1	Crystal Resonator	-	25.000	-	MHz
Output Frequency Range	FOUT1	REFOUT, Pin 11, PD#=1	-	25.000	-	MHz
Output Frequency Range	FOUT2	CLK1, Pin 19, OE=1, PD#=1	-	12.000	-	MHz
Output Frequency Range	FOUT3	CLK2, Pin 3, PD#=1	-	125.000	-	MHz
Output Frequency Range	FOUT4	SSCLK1, Pin 14, SSON=0, PD#=1	-	133.333	-	MHz
Output Frequency Range	FOUT5	SSCLK2, Pin 16, SSON=0, PD#=1	-	50.000	-	MHz
Output Duty Cycle	DC1	REFCLK, CLK1/2 and SSCLK1/2	45	50	55	%
Clock Accuracy	PPM	All clocks (Pins 3, 11, 14, 16, 19)	-1	0	1	ppm
Rise/Fall Time	Tr/f-1	REFOUT, Pin 11, CL=10pF, VDD=3.3V	-	3.2	4.0	ns
Rise/Fall Time	Tr/f-2	CLK1, Pin 19, CL=10pF, VDD02=3.3V	-	0.8	1.4	ns
Rise/Fall Time	Tr/f-3	CLK2, Pin 3, CL=10pF, VDD02=3.3V	-	0.8	1.4	ns
Rise/Fall Time	Tr/f-4	SSCLK1, Pin 14, CL=10pF, VDD01=3.3V	-	0.8	1.4	ns
Rise/Fall Time	Tr/f-5	SSCLK2, Pin 16, CL=10pF, VDD03=3.3V	-	1.6	2.4	ns
Cycle-to-Cycle Jitter	CCJ1	REFOUT=25.000MHz, CL=10pF, Pins 11	-	40	-	ps-rms
Cycle-to-Cycle Jitter	CCJ2	CLK1=12.000MHz, CL=10pF Pin 19	-	22	-	ps-rms
Cycle-to-Cycle Jitter	CCJ3	CLK2=125.000MHz, CL=10pF Pin 3	-	18	-	ps-rms
Cycle-to-Cycle Jitter	CCJ4	SSCLK2=50.000MHz, SSON=1, CL=10pF, Pin 16	-	40	-	ps-rms
Cycle-to-Cycle Jitter	CCJ5	SSCLK1=133.333MHz, SSON=1, CL=10pF, Pin 14	-	18	-	ps-rms
Power-down Time	t_{PD}	Time from PD# falling edge to Hi-Z at outputs (Asynchronous)	-	150	350	ns
Power-up Time (Crystal)	t_{PU1}	Time from VDD=3.3V rising edge to valid output frequency (Asynchronous)	-	5.0	8.0	ms
Power-up time (PD#)	t_{PU2}	Time from PD# rising edge to valid frequency at outputs (Asynchronous)		0.25	2.0	ms
Output Enable Time	t_{OE}	Time from OE rising edge to valid clock at Pin-19 (Asynchronous)	-	250	400	ns

Output Disable Time	t_{OD}	Time from OE falling edge to Hi-Z at Pin-19 (Asynchronous)	-	200	350	ns
Power Supply Ramp	t_{PSR}	Time for VDD and VDDO reaching minimum specified value and monolithic power supply ramp	0	-	12	ms
Spread Percent	SPR1	Center Spread, SSCLK1, Pin 14 SSON=1 and PD#=1	-	+/-0.25	-	%
Spread Percent	SPR1	Up Spread, SSCLK2, Pin 16 SSON=1 and PD#=1	-	+0.5	-	%
Spread Percent Variation	ΔSS%	Variation of programmed Spread %	-15	-	15	%
Modulation Frequency	FMOD	All spread spectrum clocks when spread is on	-	38.6	-	kHz

DC Electrical Characteristics (I-Grade)

Unless otherwise stated VDD=VDDO==3.3V+/-10%, CL=15pF and Ambient Temperature range -40 to +85 Deg C

Description	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	VDD+/-10%	2.97	3.3	3.63	V
Operating Voltage	VDDO	VDDO1/2/3, VDDO≤VDD	2.97	3.3	3.63	V
Input Low Voltage	VIL	CMOS Level, PD#, OE, SSON	0	-	0.3VDD	V
Input High Voltage	VIH	CMOS Level, Pins programmed as PD#, OE or SSON	0.7VDD	-	VDD	V
Output High Voltage	VOH1	IOH=-4mA , REFOUT and CLK1/2, SSCLK1/2 if VDDO=VDD	VDD-0.5	-	-	V
Output Low Voltage	VOL1	IOL=4mA , REFOUT, CLK1/2, SSCLK1/2	-	-	0.5	V
Input High Current	IIH	VIN=VDD, Pins 2, 3 and 24	-50	-	50	µA
Input Low Current	IIL	VIN=GND, Pins 2, 3 and 24	-50	-	50	µA
Pull-up or Down Resistors	RPU/D	Pins 2, 3 and 24	-	200	-	kΩ
Operating Supply Current	IDD	Xin=25.000MHz and all 5 clocks are active and CL=0, VDD=3.3V	-	30	40	mA
Standby Current	ISBC	PD#=GND	-	650	-	µA
Output Leakage Current	IOL	OE=GND at CLKOUT pins	-10	-	10	µA
Input Capacitance	Cin Cout	Pins 1 and 28 (On-chip CXin and CXout pin capacitances)	-	34	-	pF
Input Capacitance	CIN2	Pins 2, 17 and 24 (OE, SSON and PD#)	-	4	6	pF
Load Capacitance	CL	All CLKOUT outputs	-	-	15	pF

AC Electrical Characteristics (I-Grade)

Unless otherwise stated VDD=VDDO=3.3V+/-10%, CL=15pF and Ambient Temperature range -40 to +85 Deg C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Frequency Range	FIN1	Crystal Resonator	-	25.000	-	MHz
Output Frequency Range	FOUT1	REFOUT, Pin 11, PD#=1	-	25.000	-	MHz
Output Frequency Range	FOUT2	CLK1, Pin 19, OE=1, PD#=1	-	12.000	-	MHz
Output Frequency Range	FOUT3	CLK2, Pin 3, PD#=1	-	125.000	-	MHz
Output Frequency Range	FOUT4	SSCLK1, Pin 14, SSON=0, PD#=1	-	133.333	-	MHz
Output Frequency Range	FOUT5	SSCLK2, Pin 16, SSON=0, PD#=1	-	50.000	-	MHz
Output Duty Cycle	DC1	REFCLK, CLK1/2 and SSCLK1/2	45	50	55	%
Clock Accuracy	PPM	All clocks (Pins 3, 11, 14, 16, 19)	-1	0	1	ppm
Rise/Fall Time	Tr/f-1	REFOUT, Pin 11, CL=10pF, VDD=3.3V	-	1.4	4.0	ns
Rise/Fall Time	Tr/f-2	CLK1, Pin 19, CL=10pF, VDD02=3.3V	-	0.8	1.5	ns
Rise/Fall Time	Tr/f-3	CLK2, Pin 3, CL=10pF, VDD02=3.3V	-	0.9	1.6	ns
Rise/Fall Time	Tr/f-4	SSCLK1, Pin 14, CL=10pF, VDD01=3.3V	-	0.8	1.6	ns
Rise/Fall Time	Tr/f-5	SSCLK2, Pin 16, CL=10pF, VDD03=3.3V	-	1.6	2.4	ns
Cycle-to-Cycle Jitter	CCJ1	REFOUT=25.000MHz, CL=10pF, Pins 11	-	40	-	ps-rms
Cycle-to-Cycle Jitter	CCJ2	CLK1=12.000MHz, CL=10pF Pin 19	-	22	-	ps-rms
Cycle-to-Cycle Jitter	CCJ3	CLK2=125.000MHz, CL=10pF Pin 3	-	18	-	ps-rms
Cycle-to-Cycle Jitter	CCJ4	SSCLK2=50.000MHz, SSON=1, CL=10pF, Pin 16	-	40	-	ps-rms
Power-down Time	t_{PD}	Time from PD# falling edge to Hi-Z at outputs (Asynchronous)	-	150	350	ns
Power-up Time (Crystal)	t_{PU1}	Time from VDD=3.3V rising edge to valid output frequency (Asynchronous)	-	5.0	8.0	ms
Power-up time (PD#)	t_{PU2}	Time from PD# rising edge to valid frequency at outputs (Asynchronous)		0.25	2.0	ms
Output Enable Time	t_{OE}	Time from OE rising edge to valid clock at Pin-19 (Asynchronous)	-	250	400	ns
Output Disable Time	t_{OD}	Time from OE falling edge to Hi-Z at Pin-19 (Asynchronous)	-	200	350	ns

Power Supply Ramp	t_{PSR}	Time for VDD and VDDO reaching minimum specified value and monolithic power supply ramp	0	-	12	ms
Spread Percent	SPR1	Center Spread, SSCLK1, Pin 14 SSON=1 and PD#=1	-	+/-0.25	-	%
Spread Percent	SPR1	Up Spread, SSCLK2, Pin 16 SSON=1 and PD#=1	-	+0.5	-	%
Spread Percent Variation	ΔSS%	Variation of programmed Spread %	15	-	15	%
Modulation Frequency	FMOD	All spread spectrum clocks when spread is on	-	38.6	-	kHz

External Components & Design Considerations

Decoupling Capacitor: A decoupling capacitor of 0.1µF must be used between all VDD or VDDO and VSS pins on PCB. Place the capacitor on the component side of the PCB as close to the VDD or VDDO pins as possible. The PCB trace to the VDD or VDDO pins and to the GND via should be kept as short as possible Do not use vias between the decoupling capacitor and the VDD or VDDO pins.

Series Termination Resistor: A series termination resistor is recommended if the distance between the outputs (SSCLK, CLK or REFCLK pins) and the load is over 1 ½ inch. The nominal impedance of the all clock outputs are about 25 Ω. Use 20 Ω resistor in series with the output to terminate 50Ω trace impedance and place 20 Ω resistor as close to the SSCLK output as possible.

Crystal and Crystal Load: Use only parallel resonant fundamental crystals. DO NOT USE higher overtone crystals. To meet the crystal initial accuracy specification (in ppm); the internal on-chip programmable capacitors PCin and PCout must be programmed to match the crystal load requirement. These values are given by the formula below:

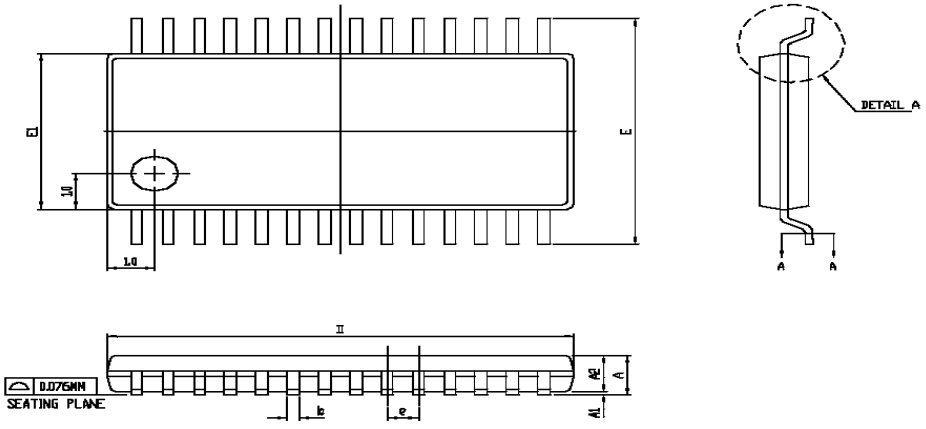
$$PCin(pF) = PCout(pF) = [(CL(pF) - Cp(pF)/2)] \times 2$$

Where CL is crystal load capacitor as given by the crystal datasheet and Cp(pF) is the compensation factor for the total parasitic capacitance at XIN or XOUT pin including PCB related parasitic capacitance.

As an example; if a crystal with CL=18pF is used and Cp=2pF, by using the above formula, PCin=PCout=[(18-(2/2)] x 2 = 34pF. Programming PCin and PCout to 34pF assures that this crystal sees an equivalent load of 18pF and no other external crystal load capacitor is needed. Deviating from the crystal load specification could cause an increase in frequency accuracy in ppm.

Package Outline and Package Dimensions

28-Pin TSSOP Package



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.20			.047
A1	0.05		0.15	.002		.006
A2	0.80	0.90	1.05	.031	.035	.041
L	0.45	0.60	0.75	.018	.024	.030
D	9.60	9.70	9.80	.378	.382	.386
E	6.30	6.40	6.50	.248	.252	.256
E1	4.30	4.40	4.50	.169	.173	.177
R	0.09			.004		
R1	0.09			.004		
b	0.19		0.30	.007		.012
b1	0.19	0.22	0.25	.007	.009	.010
c	0.09		0.20	.004		.008
c1	0.09		0.16	.004		.006
L1	1.0 REF.			.039 REF.		
e	0.65 BSC.			.026 BSC.		
θ1	0		8	0		8
θ2	12 REF.			12 REF.		
θ3	12 REF.			12 REF.		
N	28					
REF	JEDEC MO-153 VAR. AE					

Ordering Information [1]

Ordering Number [2]	Marking	Shipping Package	Package	Temperature
SL38000ZC-15AH	SL38000ZC-15AH	Tube	28-pin TSSOP	0 to 70°C
SL38000ZC-15AHT	SL38000ZC-15AH	Tape and Reel	28-pin TSSOP	0 to 70°C
SL38000ZI-15AH	SL38000ZI-15AH	Tube	28-pin TSSOP	-40 to 85°C
SL38000ZI-15AHT	SL38000ZI-15AH	Tape and Reel	28-pin TSSOP	-40 to 85°C

Note:

1. All SLI products are RoHS compliant.
2. “SL38000ZC/I-15AH” is “Hard Coded” version of SL38000ZC/I-15A programmable product.