



General Purpose Frequency Timing Generator

Recommended Application:

General Purpose Clock Generator

Output Features:

- 17 - PCI clocks selectable, either 33.33MHz or 66.6MHz @ 3.3V
- 1 - 48MHz @ 3.3V
- 1 - REF @ 3.3V, 14.318MHz.

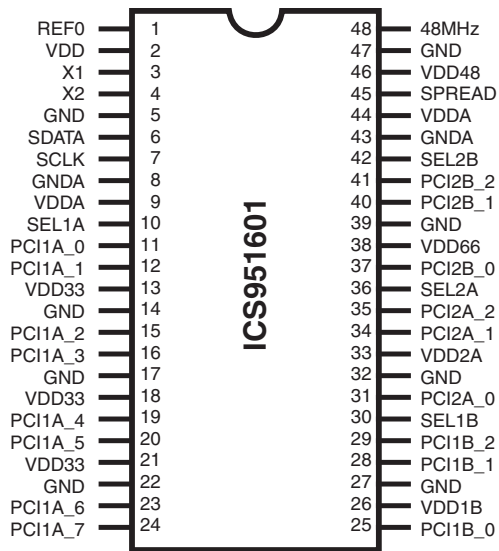
Features:

- Programmable Spread spectrum percentage for EMI control
- Uses external 14.318MHz crystal
- Select pins for frequency select

Key Specifications:

- PCI – PCI output skew within same bank @ 33MHz: <170ps
- PCI – PCI output skew within same bank @ 66MHz: <340ps
- Cycle to Cycle Jitter PCI @ 33MHz: <200ps
- Cycle to Cycle Jitter PCI @ 66MHz: <200ps
- Cycle to Cycle Jitter 48MHz: <350ps
- Cycle to Cycle Jitter REF: <500ps
- Slew Rate: 1.5 - 4 V/ns. (PCI spec.)

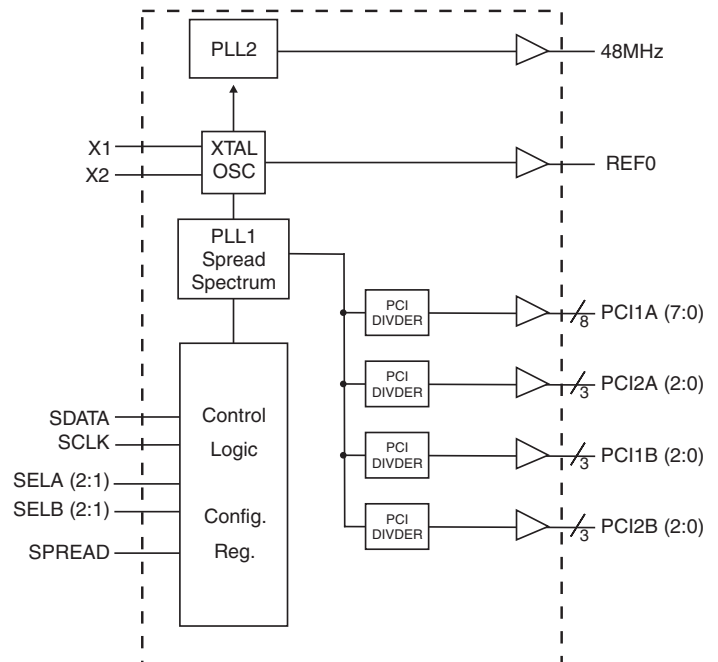
Pin Configuration



48-pin SSOP

*120K ohm pull-up to VDD on indicated inputs.

Block Diagram



Power Groups:

VDDA = Analog Power
GNDA = Analog Ground

ICS951601

Preliminary Product Preview



Pin Descriptions

| Pin number | Pin name | Type | Description |
|------------------------------------|-------------|------|---|
| 1 | REF0 | OUT | Reference output |
| 2, 13, 18, 21, 26, 33, 38, 46 | VDD | PWR | 3.3V Power supply |
| 3 | X1 | IN | Crystal input, nominally 14.318MHz. |
| 4 | X2 | OUT | Crystal output, nominally 14.318MHz. |
| 9, 44 | VDDA | PWR | Analog 3.3V Power supply |
| 10, 30, 36, 42 | SELxx | IN | Real time PCI output frequency selection pins |
| 5, 14, 17, 22, 27, 32, 39, 47 | GND | PWR | Ground pins |
| 6 | SDATA | I/O | Data pin for I ² C circuitry 5V tolerant |
| 7 | SCLK | IN | Clock input of I ² C input |
| 8, 43 | GNDA | PWR | Analog ground pins |
| 24, 23, 20, 19, 16, 15, 12, 11, | PCI1A (7:0) | OUT | PCI clock outputs, selectable to be either 33.33 or 66.66MHz at 3.3V. |
| 29, 28, 25 | PCI1B (2:0) | OUT | PCI clock outputs, selectable to be either 33.33 or 66.66MHz at 3.3V. |
| 35, 34, 31 | PCI2A (2:0) | OUT | PCI clock outputs, selectable to be either 33.33 or 66.66MHz at 3.3V. |
| 41, 40, 37 | PCI2B (2:0) | OUT | PCI clock outputs, selectable to be either 33.33 or 66.66MHz at 3.3V. |
| 45 | SPREAD | IN | Enables Spread Spectrum, default is on. |
| 48 | 48MHz | OUT | Fixed 48MHz clock output for USB. |



General I²C serial interface information

The information in this section assumes familiarity with I²C programming.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends a dummy command code
- ICS clock will **acknowledge**
- Controller (host) sends a dummy byte count
- ICS clock will **acknowledge**
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will **acknowledge** each byte **one at a time**.

| How to Write: | |
|---------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D2 _(H) | |
| | ACK |
| Dummy Command Code | |
| | ACK |
| Dummy Byte Count | |
| | ACK |
| Byte 0 | |
| | ACK |
| Byte 1 | |
| | ACK |
| Byte 2 | |
| | ACK |
| Byte 3 | |
| | ACK |
| Byte 4 | |
| | ACK |
| Byte 5 | |
| | ACK |
| Stop Bit | |

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will **acknowledge**
- ICS clock will send the **byte count**
- Controller (host) acknowledges
- ICS clock sends first byte (**Byte 0**) through **byte 5**
- Controller (host) will need to acknowledge each byte

| How to Read: | |
|---------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D3 _(H) | |
| | ACK |
| | Byte Count |
| ACK | |
| | Byte 0 |
| ACK | |
| | Byte 1 |
| ACK | |
| | Byte 2 |
| ACK | |
| | Byte 3 |
| ACK | |
| | Byte 4 |
| ACK | |
| | Byte 5 |
| ACK | |
| Stop Bit | |

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

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Serial Configuration Command Bitmap

Byte 0: Functionality and frequency select register (Default = 0)

| Bit | Bit2 | Bit7 | Bit6 | Bit5 | Bit4 | 66MHZ | 33MHZ | FEATURES | PWD |
|--------------|--|------|------|------|------|-------|-----------------------|-----------------------|-------|
| | FS4 | FS3 | FS2 | FS1 | FS0 | | | | |
| Bit 2,7:4 | 0 | 0 | 0 | 0 | 0 | 66 | 33 | -0.25 % down spread | 00000 |
| | 0 | 0 | 0 | 0 | 1 | 66 | 33 | -0.5 % down spread | |
| | 0 | 0 | 0 | 1 | 0 | 66 | 33 | -1.0 % down spread | |
| | 0 | 0 | 0 | 1 | 1 | 66 | 33 | -1.5 % down spread | |
| | 0 | 0 | 1 | 0 | 0 | 66 | 33 | ±0.25 % center spread | |
| | 0 | 0 | 1 | 0 | 1 | 66 | 33 | ±0.5 % center spread | |
| | 0 | 0 | 1 | 1 | 0 | 66 | 33 | ±1.0 % center spread | |
| | 0 | 0 | 1 | 1 | 1 | 66.6 | 33.3 | ±1.5 % center spread | |
| | 0 | 1 | 0 | 0 | 0 | 67.32 | 33.66 | 2% over-clocking | |
| | 0 | 1 | 0 | 0 | 1 | 68.64 | 34.32 | 4% over-clocking | |
| | 0 | 1 | 0 | 1 | 0 | 69.96 | 34.98 | 6% over-clocking | |
| | 0 | 1 | 0 | 1 | 1 | 72.6 | 36.3 | 10% over-clocking | |
| | 0 | 1 | 1 | 0 | 0 | 65.27 | 32.63 | 2% under- clocking | |
| | 0 | 1 | 1 | 0 | 1 | 63.96 | 31.97 | 2% under- clocking | |
| | 0 | 1 | 1 | 1 | 0 | 62.6 | 31.3 | 2% under- clocking | |
| | 0 | 1 | 1 | 1 | 1 | 60 | 30 | 2% under- clocking | |
| | 1 | 0 | 0 | 0 | 0 | 66.6 | 33.3 | -1.4 % down spread | |
| | 1 | 0 | 0 | 0 | 1 | 66.6 | 33.3 | -1.6 % down spread | |
| | 1 | 0 | 0 | 1 | 0 | 66.6 | 33.3 | -1.8 % down spread | |
| | 1 | 0 | 0 | 1 | 1 | 66.6 | 33.3 | -2.0 % down spread | |
| 1 | 0 | 1 | 0 | 0 | 66.6 | 33.3 | ± 1.4 % center spread | | |
| 1 | 0 | 1 | 0 | 1 | 66.6 | 33.3 | ± 1.6 % center spread | | |
| 1 | 0 | 1 | 1 | 0 | 66.6 | 33.3 | ±1.8 % center spread | | |
| 1 | 0 | 1 | 1 | 1 | 66.6 | 33.3 | ± 2.0 % center spread | | |
| Bit3 | 0-Frequency and Spread is selected by hardware select. Latched input 1-Frequency is selected by Bit2, 7:4 | | | | | | | | 0 |
| Bit1 | 0-Normal 1-Spread spectrum Enabled | | | | | | | | 0 |
| Bit0 | 0-Running 1-Tristate all outputs | | | | | | | | 0 |



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Byte 1: PCI1A Stop Clocks Register (1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------|-----|-------------|
| Bit 7 | 24 | 1 | PCI1A_7 |
| Bit 6 | 23 | 1 | PCI1A_6 |
| Bit 5 | 20 | 1 | PCI1A_5 |
| Bit 4 | 19 | 1 | PCI1A_4 |
| Bit 3 | 16 | 1 | PCI1A_3 |
| Bit 2 | 15 | 1 | PCI1A_2 |
| Bit 1 | 12 | 1 | PCI1A_1 |
| Bit 0 | 11 | 1 | PCI1A_0 |

Byte 2: PCI2A Stop Clocks Register (1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------|-----|-------------|
| Bit 7 | 35 | 1 | PCI2A_2 |
| Bit 6 | 34 | 1 | PCI2A_1 |
| Bit 5 | 31 | 1 | PCI2A_0 |
| Bit 4 | 29 | 1 | PCI1B_2 |
| Bit 3 | 28 | 1 | PCI1B_1 |
| Bit 2 | 25 | 1 | PCI1B_0 |
| Bit 1 | - | X | Reserved |
| Bit 0 | - | X | Reserved |

Byte 3: PCI2B Stop Clocks Register (1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------|-----|-------------|
| Bit 7 | 41 | 1 | PCI2B_2 |
| Bit 6 | 40 | 1 | PCI2B_1 |
| Bit 5 | 37 | 1 | PCI2B_0 |
| Bit 4 | - | X | Reserved |
| Bit 3 | - | X | Reserved |
| Bit 2 | - | X | Reserved |
| Bit 1 | - | X | Reserved |
| Bit 0 | - | X | Reserved |

Byte 4: Reserved Register (1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------|-----|-------------|
| Bit 7 | 48 | 1 | 48MHz |
| Bit 6 | 1 | 1 | REF0 |
| Bit 5 | - | X | Reserved |
| Bit 4 | - | X | Reserved |
| Bit 3 | - | X | Reserved |
| Bit 2 | - | X | Reserved |
| Bit 1 | - | X | Reserved |
| Bit 0 | - | X | Reserved |

Byte 5: Latched Input Read Back Register (1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|------|-------|-----|-------------|
| Bit7 | - | X | SEL2B |
| Bit6 | - | X | SEL1B |
| Bit5 | - | X | SEL2A |
| Bit4 | - | X | SEL1A |
| Bit3 | - | X | Reserved |
| Bit2 | - | X | Reserved |
| Bit1 | - | X | Reserved |
| Bit0 | - | X | Reserved |

Note: PWD = Power-Up Default

Byte 6: Reserved for Byte Count Register (1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|------|-------|-----|------------------------------|
| Bit7 | - | 0 | Reserved for read byte count |
| Bit6 | - | 0 | Reserved |
| Bit5 | - | 0 | Reserved |
| Bit4 | - | 0 | Reserved |
| Bit3 | - | 0 | Reserved |
| Bit2 | - | 1 | Reserved |
| Bit1 | - | 1 | Reserved |
| Bit0 | - | 0 | Reserved |

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Preliminary Product Preview



Absolute Maximum Ratings

| | |
|-------------------------------|--------------------------------------|
| Supply Voltage | 5.5 V |
| Logic Inputs | GND -0.5 V to V _{DD} +0.5 V |
| Ambient Operating Temperature | 0°C to +70°C |
| Storage Temperature | -65°C to +150°C |
| Case Temperature | 115°C |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; V_{DD}, V_{DDL} = 3.3 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|-------------------------|---|-----------------------|--------|-----------------------|-------|
| Input High Voltage | V _{IH} | | 2 | | V _{DD} + 0.3 | V |
| Input Low Voltage | V _{IL} | | V _{SS} - 0.3 | | 0.8 | V |
| Input High Current | I _{IH} | V _{IN} = V _{DD} | | | 5 | mA |
| Input Low Current | I _{IL1} | V _{IN} = 0 V; Inputs with no pull-up resistors | -5 | | | mA |
| Input Low Current | I _{IL2} | V _{IN} = 0 V; Inputs with pull-up resistors | -200 | | | mA |
| Operating Supply Current | I _{DD3.30P100} | C _L = 0 pF; Select @ 100 MHz | | | 160 | mA |
| | I _{DD3.30P133} | C _L = 0 pF; Select @ 133 MHz | | | 160 | mA |
| Input frequency | F _i | V _{DD} = 3.3 V; | 11 | 14.318 | 16 | MHz |
| Input Capacitance ¹ | C _{IN} | Logic Inputs | | | 5 | pF |
| | C _{INX} | X1 & X2 pins | 27 | | 45 | pF |
| Transition Time ¹ | T _{trans} | To 1st crossing of target Freq. | | | 3 | ms |
| Settling Time ¹ | T _s | From 1st crossing to 1% target Freq. | | | 3 | ms |
| Clk Stabilization ¹ | T _{STAB} | From V _{DD} = 3.3 V to 1% target Freq. | | | 3 | ms |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------|-------------------------|---|-----|-----|-----|-------|
| Operating Supply Current | I _{DD2.50P100} | C _L = 0 pF; Select @ 100 MHz | | 16 | 75 | mA |
| | I _{DD2.50P133} | C _L = 0 pF; Select @ 133 MHz | | 19 | 90 | mA |
| Power Down Supply Current | I _{DD2.5PD} | C _L = 0 pF; PWRDWN# = 0 | | 0.1 | 100 | μA |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - PCI

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 30\text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|----------------|---|-----|-----|-----|-------|
| Output High Voltage | V_{OH1} | $I_{OH} = -11\text{ mA}$ | 2.4 | | | V |
| Output Low Voltage | V_{OL1} | $I_{OL} = 9.4\text{ mA}$ | | | 0.4 | V |
| Output High Current | I_{OH1} | $V_{OH} = 2.0\text{ V}$ | | | -22 | mA |
| Output Low Current | I_{OL1} | $V_{OL} = 0.8\text{ V}$ | 16 | | | mA |
| Rise Time ¹ | t_{r1} | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$ | | | 2 | ns |
| Fall Time ¹ | t_{f1} | $V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$ | | | 2 | ns |
| Duty Cycle ¹ | d_{t1} | $V_T = 1.5\text{ V}$ | 45 | | 55 | % |
| Skew ¹ | t_{sk1} | $V_T = 1.5\text{ V} @ 33.33$ | | | 170 | ps |
| Skew ¹ | t_{sk2} | $V_T = 1.5\text{ V} @ 66.66$ | | | 340 | ps |
| Jitter, Cycle-to-cycle ¹ | $T_{jcc-cyc1}$ | $V_T = 1.5\text{ V}$ | | | 500 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 48 MHz

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$; $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 20\text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|----------------|---|-----|-----|-----|-------|
| Output High Voltage | V_{OH5} | $I_{OH} = -16\text{ mA}$ | 2.4 | | | V |
| Output Low Voltage | V_{OL5} | $I_{OL} = 9\text{ mA}$ | | | 0.4 | V |
| Output High Current | I_{OH5} | $V_{OH} = 2.0\text{ V}$ | | | -22 | mA |
| Output Low Current | I_{OL5} | $V_{OL} = 0.8\text{ V}$ | 16 | | | mA |
| Rise Time ¹ | t_{r5} | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$ | | | 4 | ns |
| Fall Time ¹ | t_{f5} | $V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$ | | | 4 | ns |
| Duty Cycle ¹ | d_{t5} | $V_T = 1.5\text{ V}$ | 45 | | 55 | % |
| Jitter, Cycle-to-cycle ¹ | $T_{jcc-cyc5}$ | $V_T = 1.5\text{ V}$ | | | 350 | ps |

¹Guaranteed by design, not 100% tested in production.

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Electrical Characteristics - REF

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 20\text{ pF}$ (unless otherwise stated)

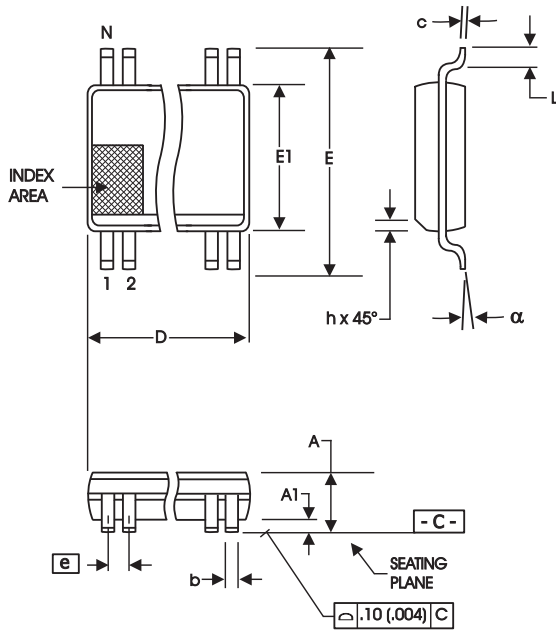
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|----------------|---|-----|-----|-----|-------|
| Output High Voltage | V_{OH5} | $I_{OH} = -16\text{ mA}$ | 2.4 | | | V |
| Output Low Voltage | V_{OL5} | $I_{OL} = 9\text{ mA}$ | | | 0.4 | V |
| Output High Current | I_{OH5} | $V_{OH} = 2.0\text{ V}$ | | | -22 | mA |
| Output Low Current | I_{OL5} | $V_{OL} = 0.8\text{ V}$ | 16 | | | mA |
| Rise Time ¹ | t_{r5} | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$ | | | 4 | ns |
| Fall Time ¹ | t_{f5} | $V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$ | | | 4 | ns |
| Duty Cycle ¹ | d_{t5} | $V_T = 1.5\text{ V}$ | 45 | | 55 | % |
| Jitter, Cycle-to-cycle ¹ | $T_{jyc-cyc5}$ | $V_T = 1.5\text{ V}$ | | | 500 | ps |

¹Guaranteed by design, not 100% tested in production.

TARGIFICATION
SUBJECT TO CHANGE
WITH FULL
PRODUCT
CHARACTERIZATION



ICS951601 Preliminary Product Preview



300 mil SSOP Package

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|--------|-------------------------------------|-------|--------------------------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 2.41 | 2.80 | .095 | .110 |
| A1 | 0.20 | 0.40 | .008 | .016 |
| b | 0.20 | 0.34 | .008 | .0135 |
| c | 0.13 | 0.25 | .005 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 10.03 | 10.68 | .395 | .420 |
| E1 | 7.40 | 7.60 | .291 | .299 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| h | 0.38 | 0.64 | .015 | .025 |
| L | 0.50 | 1.02 | .020 | .040 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| alpha | 0° | 8° | 0° | 8° |

VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|-------|----------|------|
| | MIN | MAX | MIN | MAX |
| 48 | 15.75 | 16.00 | .620 | .630 |

Reference Doc.: JEDEC Publication 95, MO-18

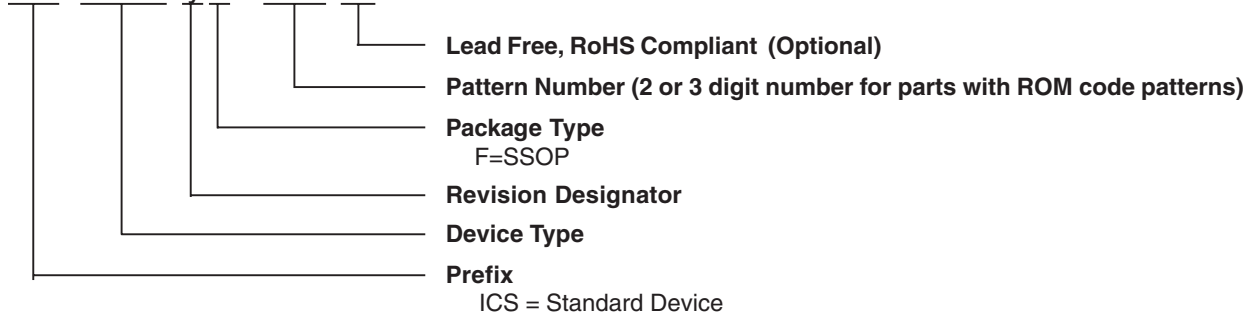
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Ordering Information

ICS951601yFLF

Example:

ICS XXXX y F - PPP LF



0663C—10/04/05

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Revision History

| Rev. | Issue Date | Description | Page # |
|------|------------|----------------------------------|--------|
| C | 10/4/2005 | Added LF to Ordering Information | 9 |
| | | | |
| | | | |
| | | | |