Preliminary

DESCRIPTION

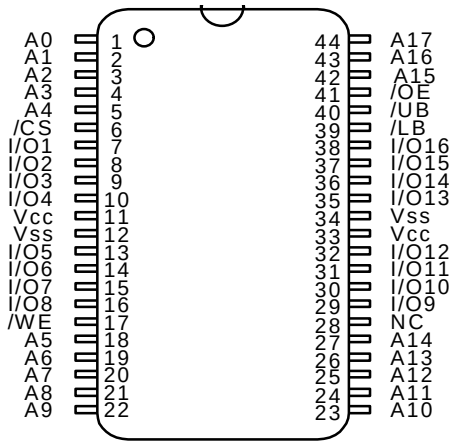
The HY63V16400A is a 4,194,304-bit high-speed SRAM organized as 262,144 words by 16 bits. The HY63V16400A uses sixteen common input and output lines and has an output enable pin which operates faster than address access time at a read cycle. Also it allows that lower and upper byte access by data byte control (/UB, /LB). The device is fabricated using HYUNDAI's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for being used in high-density and low power system applications.

FEATURES

- Single 3.3V±0.3V Power Supply
- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Data Byte Control
  - /LB : I/O1 ~ I/O8, /UB : I/O9 ~ I/O16
- Low data Retention Voltage:
  - 2.0V(min) : L-ver.Only
- Center Power/Ground Pin Configuration
- Standard pin configuration
  - 44pin 400mil SOJ
  - 44pin 400mil TSOP-II

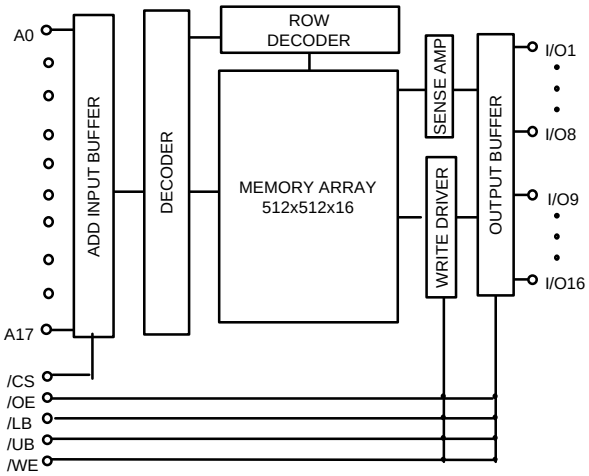
Product No.	Voltage (V)	Speed (ns)	Operation Current/Icc(mA)	Standby Current(uA)	
					L
HY63V16400A	3.3	10	240	10	1
		12	230	10	1
		15	220	10	1

PIN CONNECTION (Top View)



SOJ/TSOPII

BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Function	Pin Name	Pin Function
/CS	Chip Select	I/O1~I/O16	Data Input/Output
/WE	Write Enable	A0~A17	Address Input
/OE	Output Enable	Vcc	Power(+3.3V)
/LB	Low Byte Control(I/O1~I/O8)	Vss	Ground
/UB	Upper Byte Control(I/O9~I/O16)	NC	No Connection

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating	Unit
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to Vss	-0.5 to 4.6	V
Vcc	Voltage on Vcc Supply Relative to Vss	-0.5 to 5.5	V
T_A	Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-65 to 150	°C
P_D	Power Dissipation	1.0	W

Note
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

TRUTH TABLE

/CS	/WE	/OE	/LB	/UB	MODE	I/O Pin		Supply Current
						I/O1 - I/O8	I/O9 - I/O16	
H	X	X	X	X	Not Select	High-Z	High-Z	Standby
L	H	H	X	X	Output Disable	High-Z	High-Z	Active
L	X	X	H	H				
L	H	L	L	H	Read	Dout	High-Z	Active
			H	L		High-Z	Dout	
			L	L		Dout	Dout	
L	L	X	L	H	Write	Din	High-Z	Active
			H	L		High-Z	Din	
			L	L		Din	Din	

Note
1.H=V_{IH}, L=V_{IL}, X=Don' t Care.

DC ELECTRICAL CHARACTERISTICS

Vcc = 3.3V±0.3V, T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	Vss ≤ V_{IN} ≤ Vcc		-2	-	2	uA
I_{LO}	Output Leakage Current	Vss ≤ V_{OUT} ≤ Vcc, /CS = V_{IH} or /OE = V_{IH} or /WE = V_{IL}		-2	-	2	uA
Icc	Operating Power Supply Current	/CS = V_{IL}, V_{IN} = V_{IH}, $I_{I/O}$ = 0mA Min. Duty Cycle = 100%	10ns	-	-	240	mA
			12ns	-	-	230	mA
			15ns	-	-	220	mA
I_{SB}	TTLStandbyCurrent (TTL Input)	/CS = V_{IH}, V_{IN} = V_{IH} or V_{IL}, Min. Cycle		-	-	60	mA
I_{SB1}	CMOS Standby Current (CMOS Input)	/CS ≥ Vcc - 0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V, f =0Mhz		-	-	10	mA
			L	-	-	1	mA
V_{OL}	Output Low Voltage	I_{OL} = 8.0mA		-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4.0mA		2.4	-	-	V

Note : Typical values are at Vcc = 3.3V, T_A = 25°C

RECOMMENDED DC OPERATING CONDITION (T_A=0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	3.0	3.3	3.6	V
Vss	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	-	Vcc+0.3(2)	V
V_{IL}	Input Low Voltage	-0.3(1)	-	0.8	V

Note
1. V_{IL}(min) = -2.0V a.c(pulse width ≤ 8ns) for I ≤ 20mA
2. V_{IH}(max) = Vcc + 2.0V a.c(pulse width ≤ 8ns) for I ≤ 20mA

CAPACITANCE

(Temp = 25°C, f = 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

Note : These parameters are sampled and not 100% tested

AC CHARACTERISTICS

Vcc = 3.3V±0.3V, T_A= 0°C to 70°C, unless otherwise specified

#	Symbol	Parameter	10ns		12ns		15ns		Unit
			Min	Max	Min	Max	Min	Max	
READ CYCLE									
1	tRC	Read Cycle Time	10	-	12	-	15	-	ns
2	tAA	Address Access Time	-	10	-	12	-	15	ns
3	tACS	Chip Select Access Time	-	10	-	12	-	15	ns
4	tOE	Output Enable to Output Valid	-	5	-	6	-	7	ns
5	tBA	/UB,/LB Access Time	-	5	-	6	-	7	ns
6	tCLZ	Chip Select to Output in Low Z	3	-	3	-	3	-	ns
7	tOLZ	Output Enable to Output in Low Z	0	-	0	-	0	-	ns
8	tBLZ	/UB,/LB Enable to Low-Z Output	0	-	0	-	0	-	ns
9	tCHZ	Chip Deselecting to Output in High Z	0	5	0	6	0	7	ns
10	tOHZ	Out Disable to Output in High Z	0	5	0	6	0	7	ns
11	tBHZ	/UB,/LB Disable to High-Z Output	0	5	0	6	0	7	ns
12	tOH	Output Hold from Address Change	3	-	3	-	3	-	ns
WRITE CYCLE									
13	tWC	Write Cycle Time	10	-	12	-	15	-	ns
14	tCW	Chip Select to End of Write	7	-	8	-	10	-	ns
15	tAW	Address Valid to End of Write	7	-	8	-	10	-	ns
16	tAS	Address Set-up Time	0	-	0	-	0	-	ns
17	tWP	Write Pulse Width(/OE High)	7	-	8	-	10	-	ns
18	tWP1	Write Pulse Width(/OE Low)	10	-	12	-	15	-	ns
19	tWR	Write Recovery Time	0	-	0	-	0	-	ns
20	tWHZ	Write to Output in High Z	0	5	0	6	0	7	ns
21	tDW	Data to Write Time Overlap	5	-	6	-	7	-	ns
22	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
23	tOW	Output Active from End of Write	3	-	3	-	3	-	ns

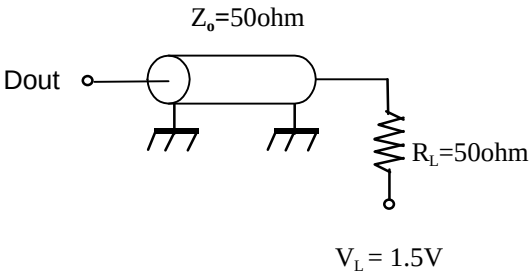
AC TEST CONDITIONS

Vcc = 3.3V±0.3V, T_A = 0°C to 70°C, unless otherwise specified

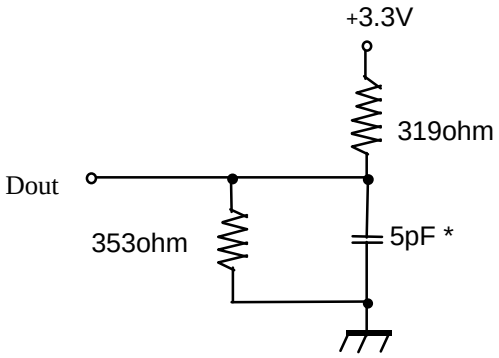
PARAMETER	Value
Input Pulse Level	0V to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Level	1.5V
Output Load	See below

AC TEST LOADS

Output Load(A)



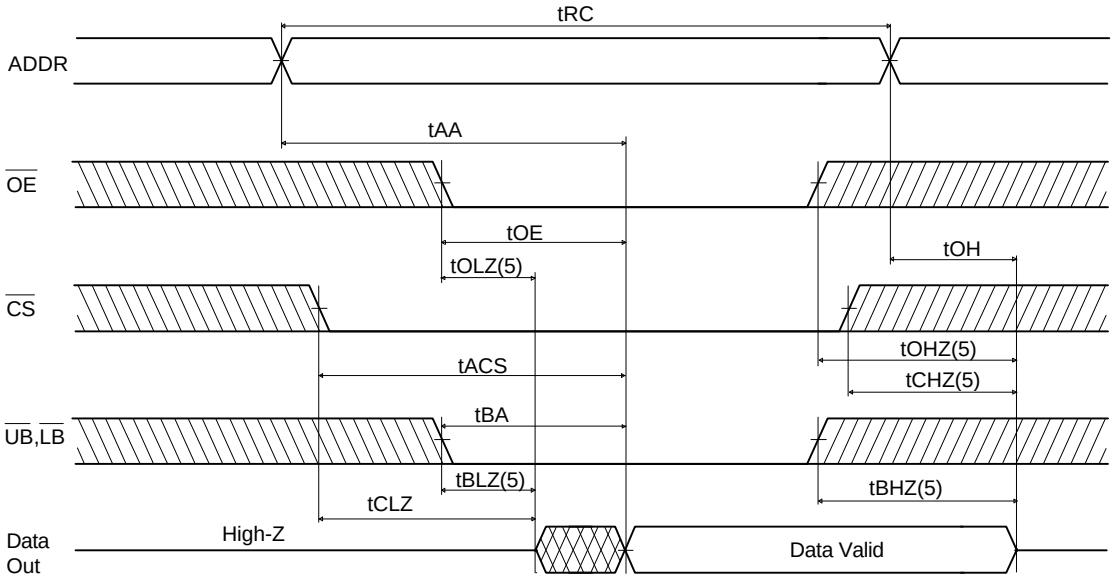
Output Load(B)
(for tCHZ, tCLZ, tOHZ, tOLZ, tWHZ & tOW)



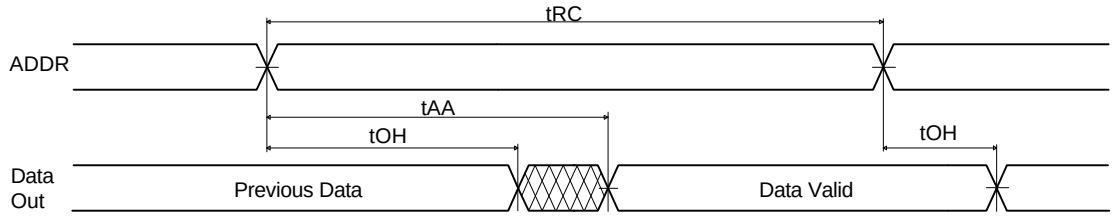
Note : *Including jig and scope capacitance

TIMING DIAGRAM

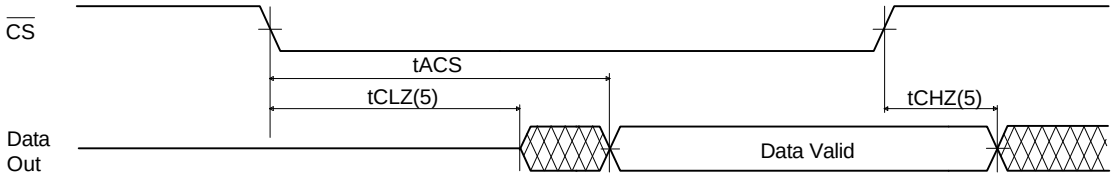
READ CYCLE 1(Note 1)



READ CYCLE 2(Note 1,2,4)

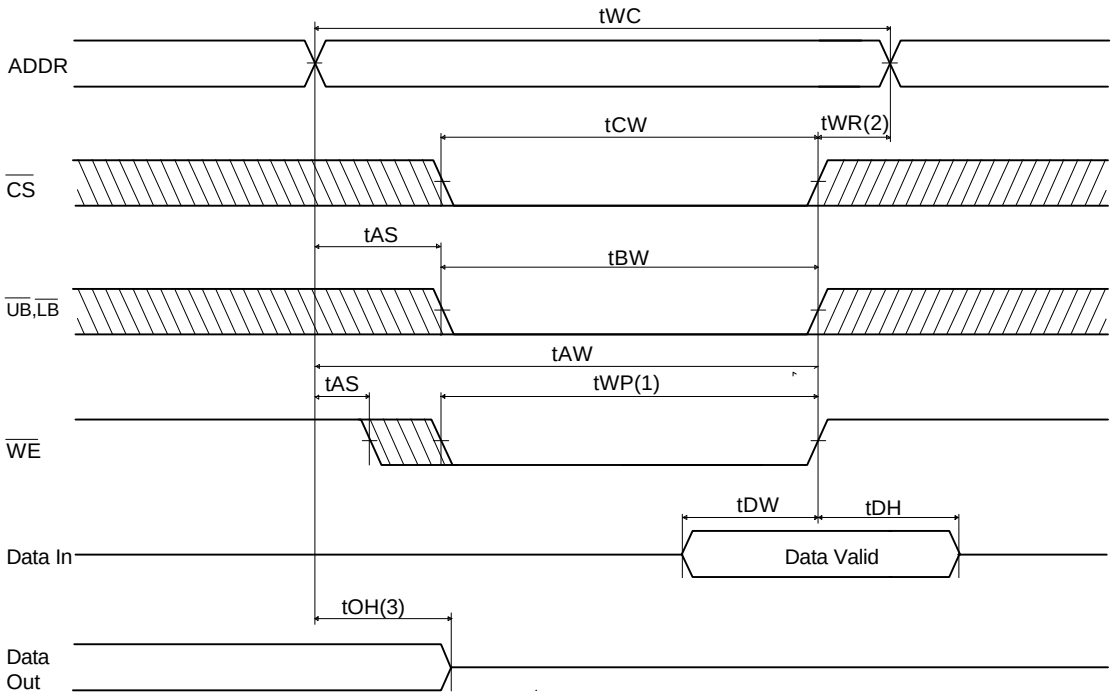


READ CYCLE 3(Note 1,3,4)

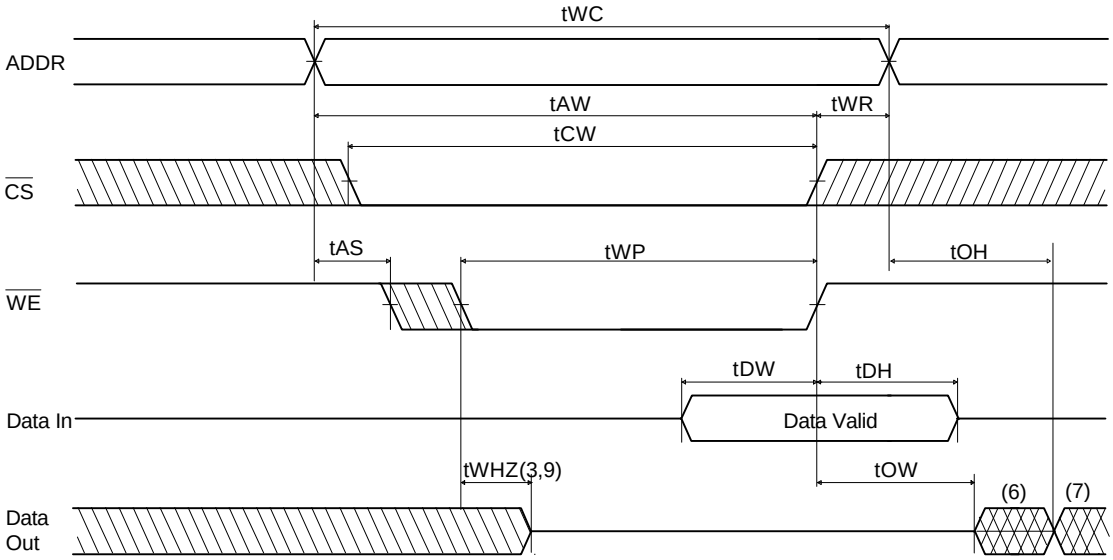


Notes:
1. /WE is high for the Read Cycle.
2. Device is continuously selected. /CS = V_{IL}
3. Address valid is prior to or coincident with /CS transition low
4. /OE = V_{IL}
5. Transition is measured ± 200mV from steady state voltage

WRITE CYCLE 1



WRITE CYCLE 2 (Note 5)



Notes:
1. A write occurs during the overlap(tWP) of a low /CS and low /WE .
2. tWR is measured from the earlier of /CS, /LB, /UB, or /WE going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the /CS, /LB and /UB low transition occur simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
5. /OE is continuously low(/OE=V_{IL})

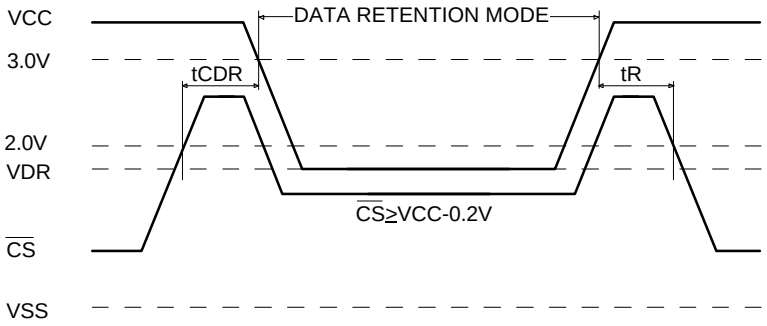
6. Q(data out) is the same phase with the write data of this write cycle.
7. Q(data out) is the read data of the next address.
8. If /CS is low during this period, I/O pins are in the output state.
   Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state.

DATA RETENTION ELECTRIC CHARACTERISTIC(L-Version)

T_A= 0°C to 70°C

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DR}	Vcc for Data Retention	/CS ≥Vcc - 0.2V	2.0	-	3.6	V
I_{DR}	Data Retention Current	Vcc = 3.0V, /CS ≥Vcc - 0.2V V_{IN} ≥Vcc-0.2V or V_{IN}≤0.2V	-	-	0.9	mA
		Vcc = 2.0V, /CS ≥Vcc - 0.2V V_{IN} ≥ Vcc-0.2V or V_{IN}≤0.2V	-	-	0.7	
tCDR	Data Retention Set-Up Time		0	-	-	ns
tR	Recovery Time		5	-	-	ms

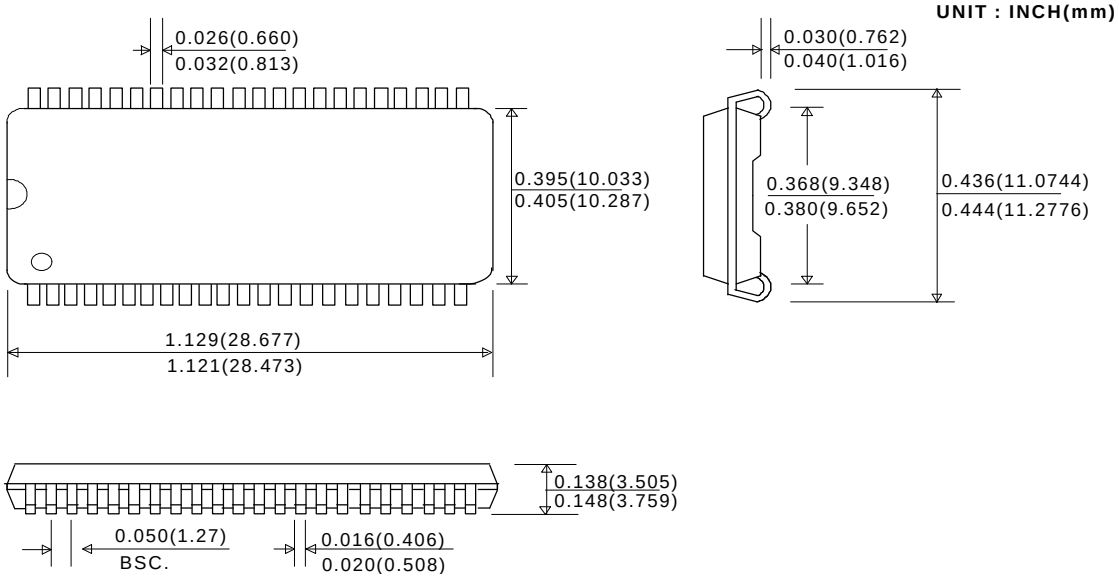
DATA RETENTION TIMING DIAGRAM



PACKAGE INFORMATION

44pin 400mil Small Outline J-Form Package(J)

UNIT : INCH(mm)



44pin 400mil Thin Small Outline Package(T2)

UNIT : INCH(mm) Max. / Min.