

DESCRIPTION

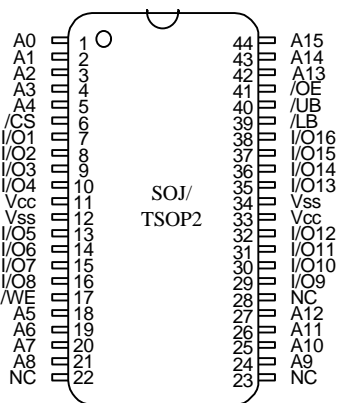
The HY63V16100A is a 1,048,576-bit high-speed, SRAM organized as 65,536 words by 16 bits. The HY63V16100A uses sixteen common input and output lines and has an output enable pin which operates faster than address access time at a read cycle. Also it allows that lower and upper byte access by data byte control (/UB, /LB). The device is fabricated using HYUNDAI's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for being used in high-density and low power system applications.

FEATURES

- Single 3.3V ± 0.3V Power Supply
- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Data Byte Control
 - LB : I/O1 ~ I/O8, UB : I/O9 ~ I/O16
- Low data Retention Voltage:
 - 2.0V(min)-L-ver.Only
- Center Power/Ground Pin Configuration
- Standard pin configuration
 - 44pin 400mil SOJ/TSOP-II

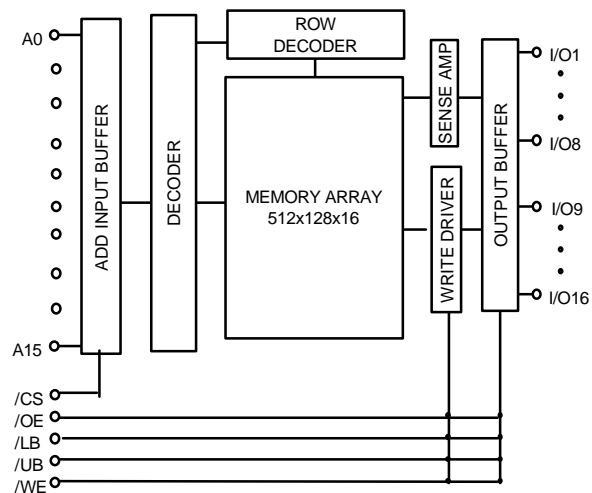
Product No.	Supply Voltage(V)	Speed (ns)	Operation Current(mA)	Standby Current(mA)	
					L
HY63V16100A	3.3	8	240	5	0.5
HY63V16100A	3.3	10	230	5	0.5
HY63V16100A	3.3	12	220	5	0.5

PIN CONNECTION (Top View)



SOJ/TSOP2

BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Function	Pin Name	Pin Function
/CS	Chip Select	I/O1~I/O16	Data Input/Output
/WE	Write Enable	A0~A15	Address Input
/OE	Output Enable	Vcc	Power(+3.3V)
/LB	Low Byte Control(I/O1~I/O8)	Vss	Ground
/UB	Upper Byte Control(I/O9~I/O16)	N.C	No Connection

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Rating	Unit
V _{IN} , V _{OUT}	Voltage on Any Pin Relative to V _{SS}	-0.5 to 4.6	V
V _{CC}	Voltage on V _{CC} Supply Relative to V _{SS}	-0.5 to 5.5	V
T _A	Operating Temperature	Commercial	0 to 70 °C
		Industrial	-40 to 85 °C
T _{STG}	Storage Temperature	-65 to 150	°C
P _D	Power Dissipation	1.0	W

Note

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0°C to 70°C)

Symbol	Parameter	Min.	Type	Max.	Unit
V _{CC}	Supply Voltage	3.0	3.3	3.6	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.0	-	V _{CC} +0.3(2)	V
V _{IL}	Input Low Voltage	-0.3(1)	-	0.8	V

Note

- V_{IL} (min) = -2.0V a.c(pulse width less than 8ns) for I ≤ 20 mA
- V_{IH} (max) = V_{CC} + 2.0V a.c(pulse width less than 8ns) for I ≤ 20 mA

DC ELECTRICAL CHARACTERISTICS

 (V_{CC} = 3.3V±0.3V, T_A = 0°C to 70°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	
I _{LI}	Input Leakage Current	V _{SS} ≤ V _{IN} ≤ V _{CC}	-2	-	2	uA	
I _{LO}	Output Leakage Current	V _{SS} ≤ V _{OUT} ≤ V _{CC} , /CS = V _{IH} or /OE = V _{IH} or /WE = V _{IL}	-2	-	2	uA	
I _{CC}	Operating Current	/CS = V _{IL} , V _{IN} = V _{IH} , I _{I/O} = 0mA	8ns	-	-	240	mA
			10ns	-	-	230	mA
			12ns	-	-	220	mA
I _{SB}	TTL Standby Current (TTL Inputs)	/CS = V _{IH} , V _{IN} =V _{IH} or V _{IL} Min. Cycle	-	-	60	mA	
I _{SB1}	CMOS Standby Current (CMOS Inputs)	/CS ≤ V _{CC} -0.2V, V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V		-	-	5	mA
			L	-	-	0.5	mA
V _{OL}	Output Low Voltage	I _{OL} = 8.0mA	-	-	0.4	V	
V _{OH}	Output High Voltage	I _{OH} = -4.0mA	2.4	-	-	V	

 Note : Typical values are at V_{CC} = 3.3V, T_A = 25°C

AC CHARACTERISTICS

 (V_{CC} = 3.3V ± 0.3V, T_A = 0°C to 70°C, unless otherwise specified.)

#	Symbol	Parameter	8ns		10ns		12ns		unit
			Min	Max	Min	Max	Min	Max	
READ CYCLE									
1	t _{RC}	Read Cycle Time	8	-	10	-	12	-	ns
2	t _{AA}	Address Access Time	-	8	-	10	-	12	ns
3	t _{ACS}	Chip Select Access Time	-	8	-	10	-	12	ns
4	t _{OE}	Output Enable to Output Valid	-	4	-	5	-	6	ns
5	t _{BA}	/UB,/LB Access Time	-	4	-	5	-	6	ns
6	t _{CLZ}	Chip Select to Output in Low Z	3	-	3	-	3	-	ns
7	t _{OLZ}	Output Enable to Output in Low Z	0	-	0	-	0	-	ns
8	t _{BLZ}	/UB,/LB Enable to Low-Z Output	0	-	0	-	0	-	ns
9	t _{CHZ}	Chip Deselecting to Output in High Z	0	4	0	5	0	6	ns
10	t _{OHZ}	Out Disable to Output in High Z	0	4	0	5	0	6	ns
11	t _{BHZ}	/UB,/LB Disable to High-Z Output	0	4	0	5	0	6	ns
12	t _{OH}	Output Hold from Address Change	3	-	3	-	3	-	ns
WRITE CYCLE									
13	t _{WC}	Write Cycle Time	8	-	10	-	12	-	ns
14	t _{CW}	Chip Select to End of Write	6	-	7	-	8	-	ns
15	t _{AW}	Address Valid to End of Write	6	-	7	-	8	-	ns
16	t _{AS}	Address Set-up Time	0	-	0	-	0	-	ns
17	t _{WP}	Write Pulse Width(/OE High)	6	-	7	-	8	-	ns
18	t _{WP1}	Write Pulse Width(/OE Low)	8	-	10	-	12	-	ns
19	t _{BW}	/UB, /LB Valid to End of Write	6	-	7	-	8	-	ns
20	t _{WR}	Write Recovery Time	0	-	0	-	0	-	ns
21	t _{WHZ}	Write to Output in High Z	0	4	0	5	0	6	ns
22	t _{DW}	Data to Write Time Overlap	4	-	5	-	6	-	ns
23	t _{DH}	Data Hold from Write Time	0	-	0	-	0	-	ns
24	t _{OW}	Output Active from End of Write	3	-	3	-	3	-	ns

NOTE : Above parameters are also guaranteed at industrial temperature range.

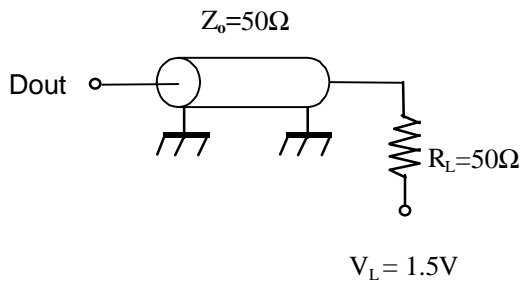
AC TEST CONDITIONS

(V_{CC} = 3.3V±0.3V, T_A = 0°C to 70°C, unless otherwise specified.)

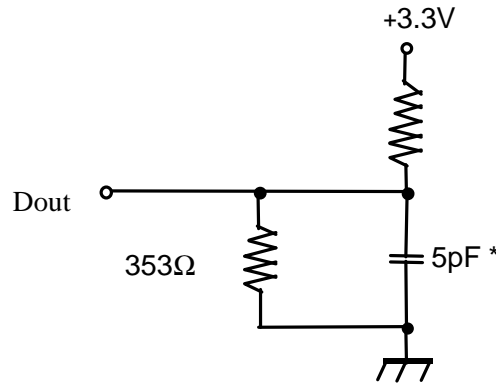
Parameter	Value
Input Pulse Level	0V to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Level	1.5V
Output Load	See below

AC TEST CONDITIONS

Output Load (A)



Output Load (B)
(for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} & t_{OZ})



Note : *Including jig and scope capacitance

CAPACITANCE

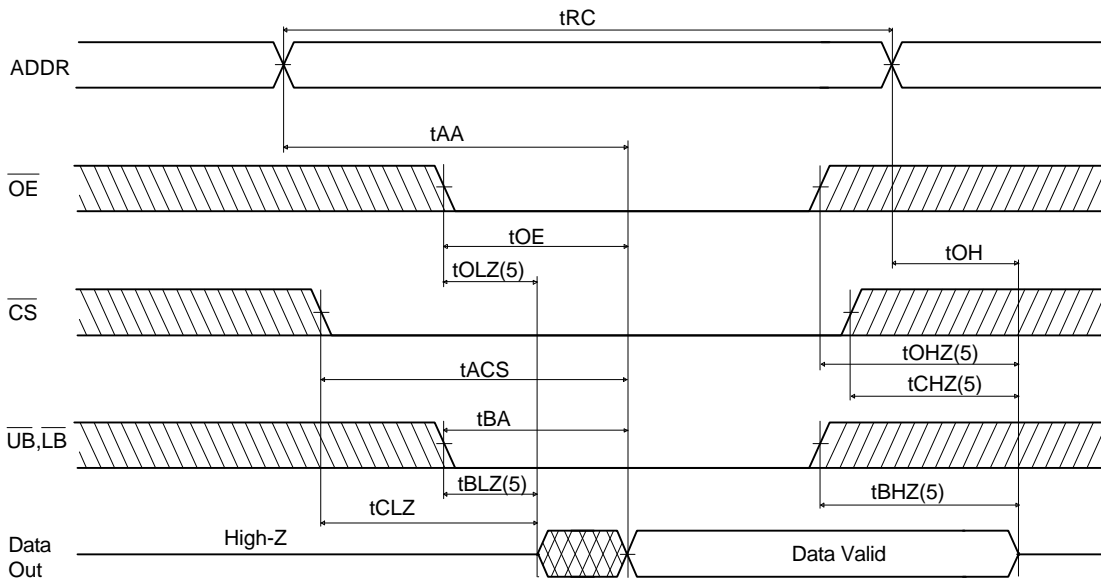
Temp = 25°C, f = 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	7	pF
C _{I/O}	Input/Output Capacitance	V _{I/O} = 0V	8	pF

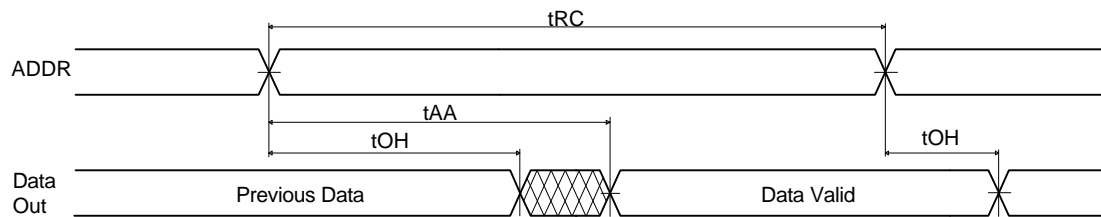
Note : This parameter is sampled and not 100% tested

TIMING DIAGRAM

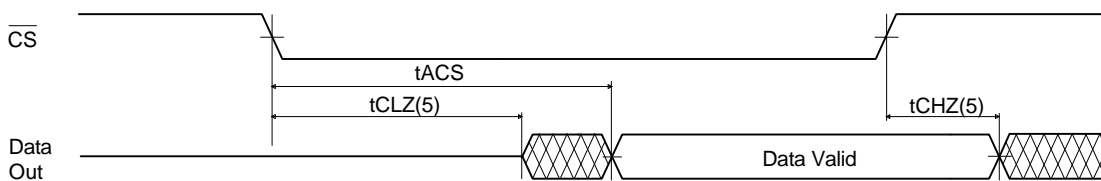
READ CYCLE 1(Note 1)



READ CYCLE 2(Note 1,2,4)



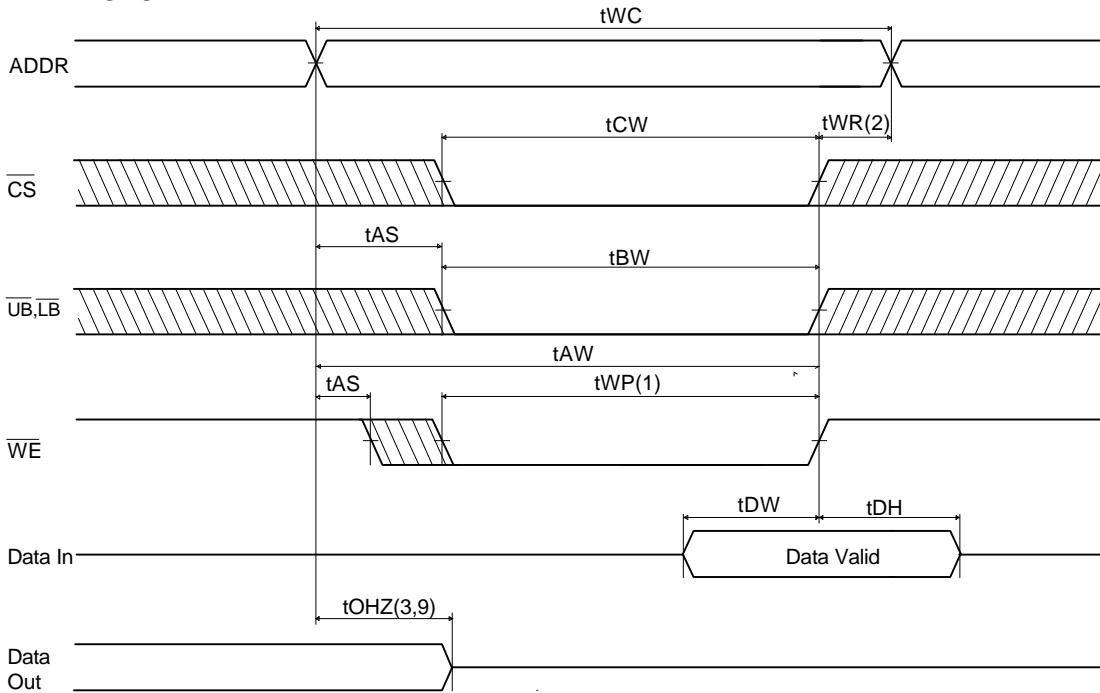
READ CYCLE 3(Note 1,3,4)



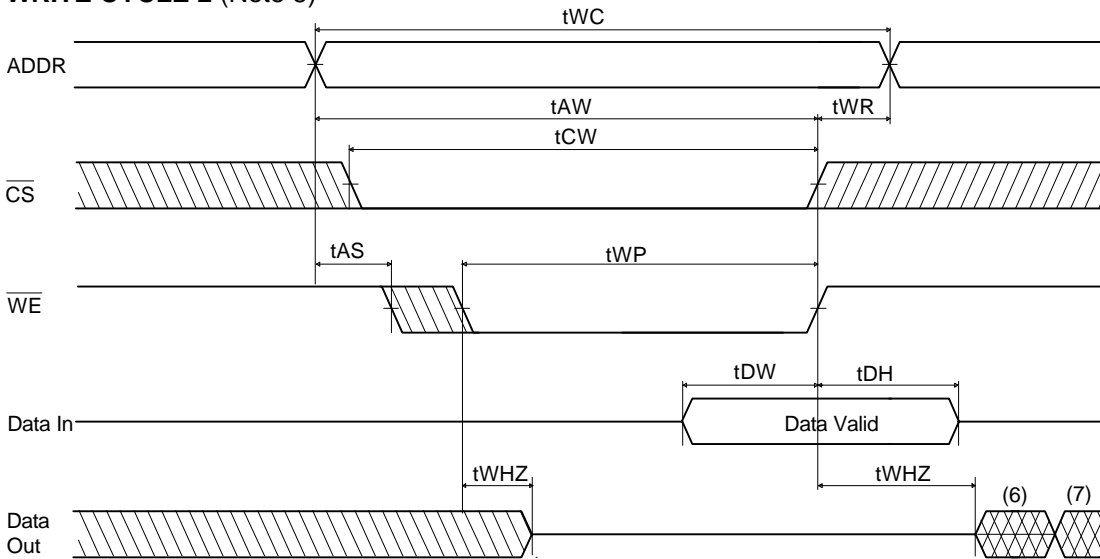
Notes:

1. \overline{WE} is high for the Read Cycle.
2. Device is continuously selected. $\overline{CS} = V_{IL}$
3. Address valid is prior to or coincident with \overline{CS} transition low
4. $\overline{OE} = V_{IL}$
5. Transition is measured + 200mV from steady state voltage.
This parameter is sampled and not 100% tested.

WRITE CYCLE 1



WRITE CYCLE 2 (Note 5)



Notes:

1. A write occurs during the overlap(t_{WP}) of a low \overline{CS} and low \overline{WE} .
2. t_{WR} is measured from the earlier of \overline{CS} , \overline{LB} , \overline{UB} , or \overline{WE} going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the \overline{CS} , \overline{LB} and \overline{UB} low transition occur simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, outputs remain in a high impedance state.
5. \overline{OE} is continuously low($\overline{OE}=V_{IL}$)
6. Q(data out) is the same phase with the write data of this write cycle.
7. Q(data out) is the read data of the next address.
8. If \overline{CS} is low during this period, I/O pins are in the output state.
Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured +200mV from steady state.
This parameter is sampled and not 100% tested.

FUNCTIONAL DESCRIPTION

/CS	/WE	/OE	/LB	/UB	MODE	I/O Pin		Supply Current
						I/O1 - I/O8	I/O9 - I/O16	
H	X	X*	X	X	Not Select	High-Z	High-Z	I _{sb} , I _{sb1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I _{cc}
L	X	X	H	H				
L	H	L	L	H	Read	Dout	High-Z	I _{cc}
			H	L		High-Z	Dout	
			L	L		Dout	Dout	
L	L	X	L	H	Write	Din	High-Z	I _{cc}
			H	L		High-Z	Din	
			L	L		Din	Din	

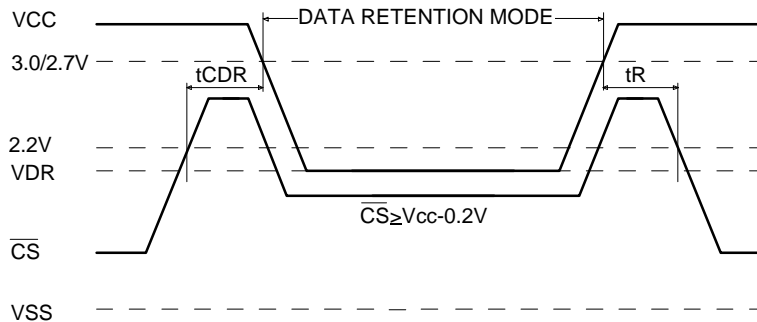
* NOTE : X means Don,t Care

DATA RETENTION ELECTRIC CHARATERISTIC

(TA = 0°C to 70°C)

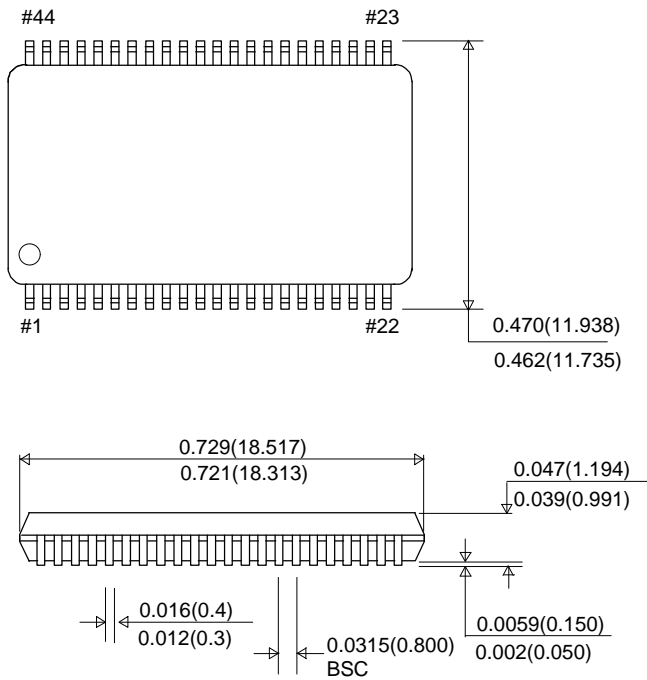
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDR	V _{cc} for Data Retention	/CS ≥ V _{cc} - 0.2V	2.0	-	3.6	V
IDR	Data Retention Current	V _{cc} = 3.0V, /CS ≥ V _{cc} - 0.2V VIN ≥ V _{cc} -0.2V or VIN ≤ 0.2V	-	-	0.9	mA
		V _{cc} = 2.0V, /CS ≥ V _{cc} - 0.2V VIN ≥ V _{cc} -0.2V or VIN ≤ 0.2V	-	-	0.7	
tCDR	Data Retention Set-Up Time		0	-	-	ns
tR	Recovery Time		5	-	-	ms

DATA RETENTION TIMING DIAGRAM



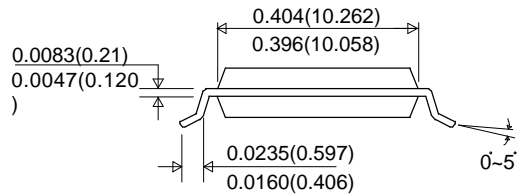
PACKAGE INFORMATION

44pin 400mil Thin Small Outline Package (T2)

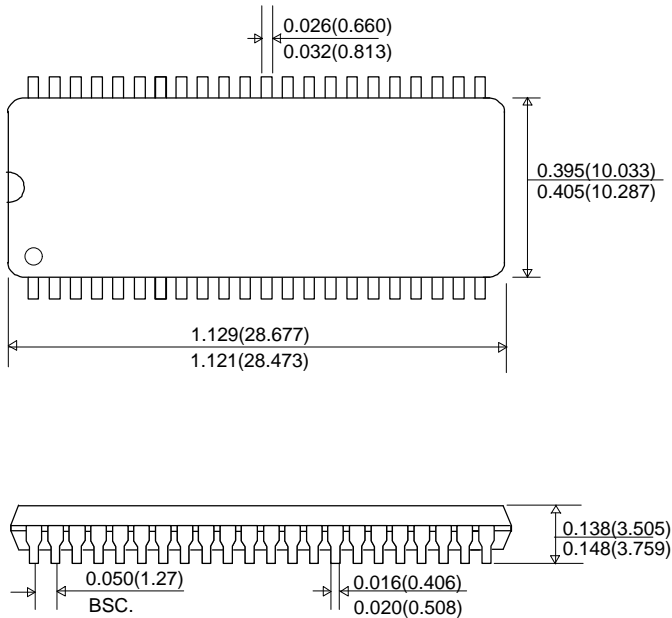


UNIT : INCH(mm)

	0.10MAX
	0.004MAX



44pin 400mil Small Outline J-Form Package (J)



UNIT : INCH(mm)

