CY7B185
CY7B186

CYPRESS SEMICONDUCTOR

8K x 8 Static RAM

Features

- **BiCMOS for optimum speed/power**
- **Ultra high speed**
  — **9 ns**
- **Low active power**
  — **750 mW**
- **Low standby power**
  — **250 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

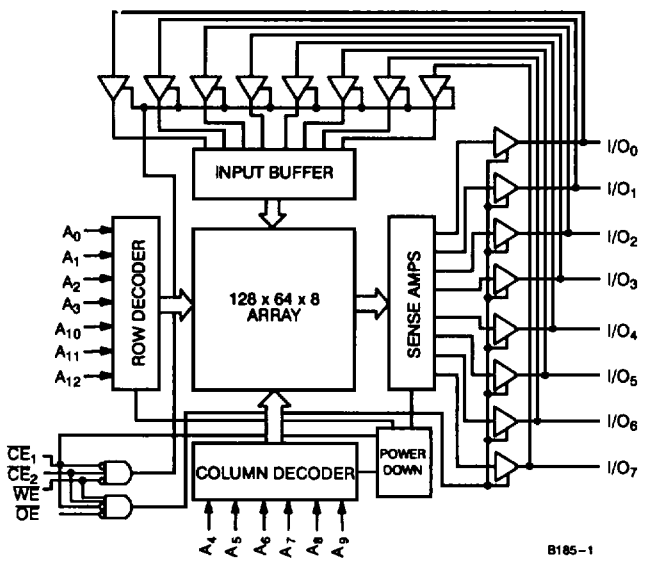
Functional Description

The CY7B185 and CY7B186 are high-performance BiCMOS static RAMs organized as 8K words by 8 bits. These RAMs are developed by Aspen Semiconductor Corporation, a subsidiary of Cypress Semiconductor. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE_1}$), an active HIGH chip enable (CE_2), and active LOW output enable ($\overline{OE}$) and three-state drivers. Both devices have a power-down feature ($\overline{CE_1}$) that reduces the power consumption by 67% when deselected. The CY7B185 is in the space saving 300-mil-wide DIP and SOJ package and leadless chip carrier. The CY7B186 is in the standard 600-mil-wide package.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE_1}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE_1}$ and $\overline{OE}$ active LOW, CE_2 active HIGH, while $\overline{WE}$ remains HIGH. Under these conditions, the contents of the location addressed by the information on the address pins is present on the eight data input/output pins.

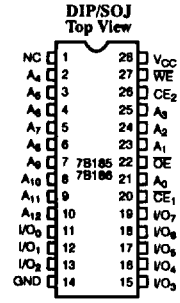
The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram

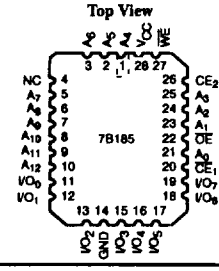


Pin Configurations

DIP/SOJ
Top View



LCC
Top View



Selection Guide

		7B185–9	7B185–10	7B185–12 7B186–12	7B185–15 7B186–15
Maximum Access Time (ns)		9	10	12	15
Maximum Operating Current (mA)	Commercial	150	145	140	135
	Military		155	150	145
Maximum Standby Current (mA)	Commercial	50	45	40	40
	Military		60	55	50

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

Input Voltage[1] ..... − 3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... > 2001V (Per MIL-STD-883 Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameters	Description	Test Conditions			7B185−9 Min.	7B185−9 Max.	7B185−10 Min.	7B185−10 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = − 4.0 mA	Com'l	2.4		2.4		V
			I_{OH} = − 2.0 mA	Mil	2.4		2.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4	V
V_{IH}	Input HIGH Level				2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]				− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			− 10	+10	− 10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled			− 10	+10	− 10	+10	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f max.		Com'l		150		145	mA
				Mil				155	mA
I_{SB}	$\overline{CE}_1$ Power-Down Current	$\overline{CE}_1$ ≥ V_{IH}, I_{OH} = mA		Com'l		50		45	mA
				Mil				60	mA

Parameters	Description	Test Conditions			7B185−12 7B186−12 Min.	7B185−12 7B186−12 Max.	7B185−15 7B186−15 Min.	7B185−15 7B186−15 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = − 4.0 mA	Com'l	2.4		2.4		V
			I_{OH} = − 2.0 mA	Mil	2.4		2.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4	V
V_{IH}	Input HIGH Level				2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]				− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			− 10	+10	− 10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled			− 10	+10	− 10	+10	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f max.		Com'l		140		135	mA
				Mil		150		145	mA
I_{SB}	$\overline{CE}_1$ Power-Down Current	$\overline{CE}_1$ ≥ V_{IH}, I_{OH} = mA		Com'l		40		40	mA
				Mil		55		50	mA

Shaded area contains preliminary information.

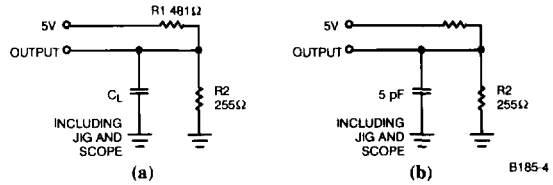
Capacitance[4]

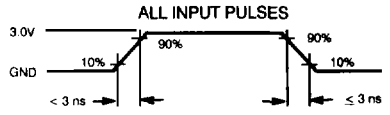
Parameters	Description	Test Conditions	Max.[5]	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{OUT}	Output Capacitance		6	pF

Notes:

1. V_{IL} (min.) = − 3.0V for pulse width < 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Tested initially and after any design or process changes that may affect these parameters.
5. For all packages except CERDIP (D16, D22), which has maximums of C_{IN} = 9.5 pF, C_{OUT} = 9 pF.

AC Test Loads and Waveforms





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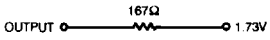
Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3,6]

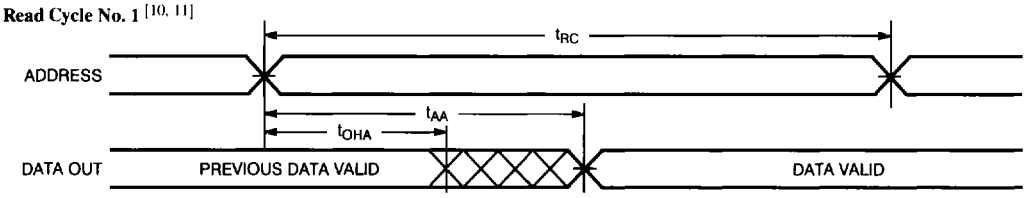
Parameters	Description	7B185–9		7B185–10		7B185–12 7B186–12		7B185–15 7B186–15		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	9		10		12		15		ns
t_{AA}	Address to Data Valid		9		10		12		15	ns
t_{OHA}	Data Hold from Address Change	2.5		3		3		3		ns
t_{ACE1}	$\overline{CE}_1$ LOW to Data Valid		9		10		12		15	ns
t_{ACE2}	CE_2 HIGH to Data Valid		9		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		4.5		5		6		8	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[7]	1.5		2		2		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]		4		5		6		7	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low Z[8]	2		2		2		3		ns
t_{LZCE2}	CE_2 HIGH to Low Z[8]	2		2		2		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z[7] CE_2 LOW to High Z		4		5		6		7	ns
WRITE CYCLE[9]										
t_{WC}	Write Cycle Time	9		10		12		15		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	8		8		8		10		ns
t_{SCE2}	CE_2 HIGH to Write End	8		8		8		10		ns
t_{AW}	Address Set-Up to Write End	8		8		8		10		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		8		10		ns
t_{SD}	Data Set-Up to Write End	4.5		5		6		7		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7]	0	4	0	5	0	6	0	7	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6,7]	2		2		2		3		ns

Notes:

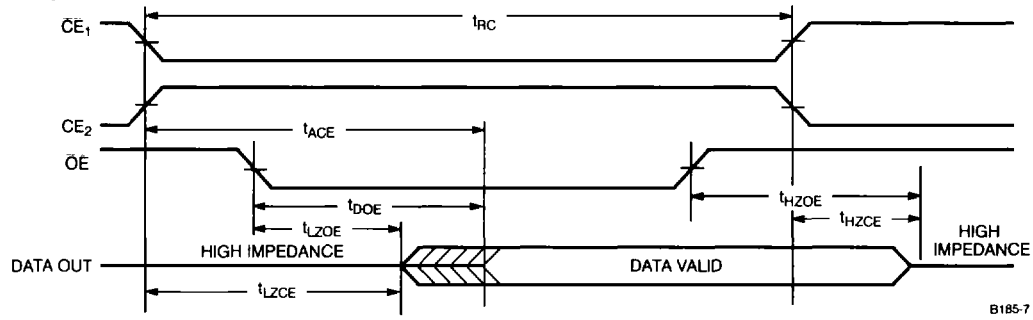
6. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and C_L = 20 pF.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage. This parameter is guaranteed and not 100% tested.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. This parameter is guaranteed and not 100% tested.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write. All three signals must be active to initiate a write, and either signal can terminate a write by going inactive.

Switching Waveforms

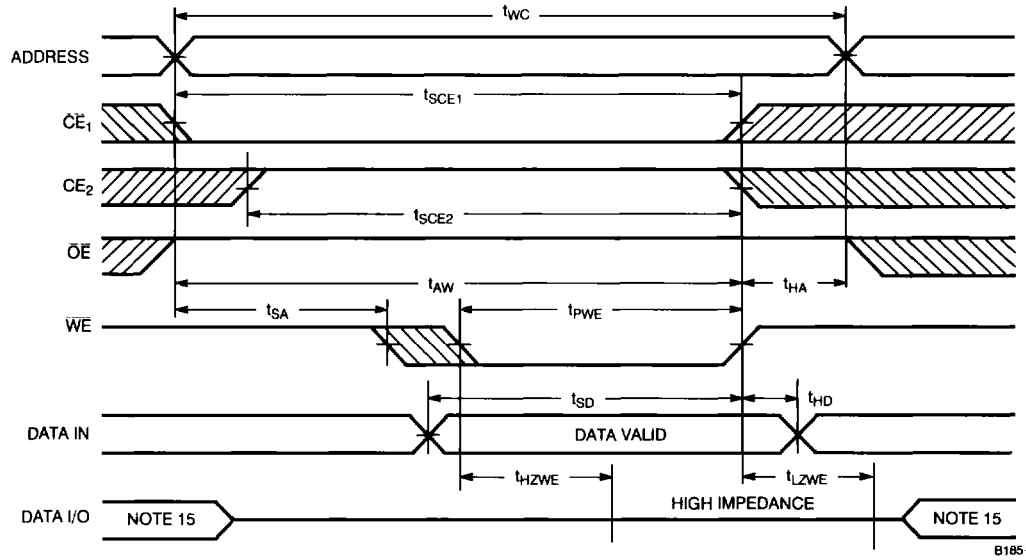
Read Cycle No. 1 [10, 11]



Read Cycle No. 2 [10, 11, 12]



Write Cycle No. 1 ($\overline{WE}$ Controlled) [8, 13, 14]

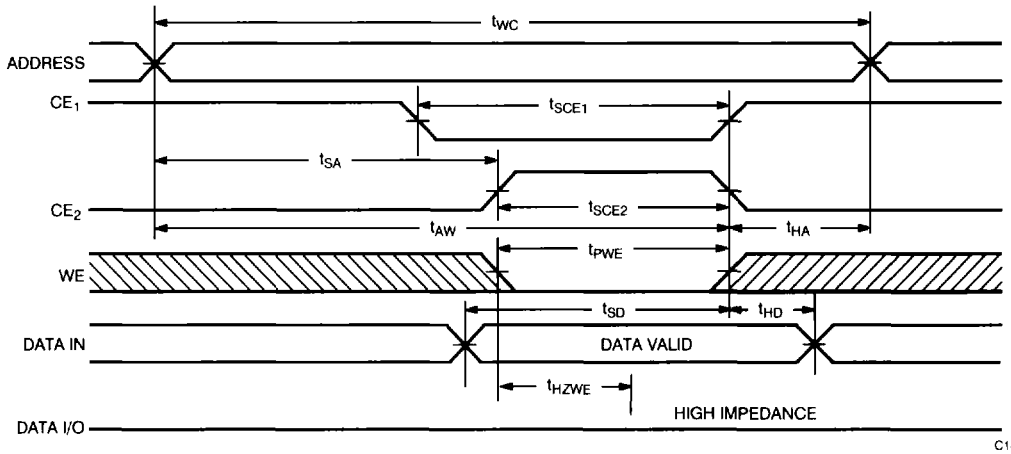


Notes:

10. Device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, CE_2 = V_{IH}.
11. $\overline{WE}$ is HIGH for read cycle.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. Data I/O is HIGH impedance if $\overline{OE}$ = V_{IH}.
14. When data input is applied to the device I/O, the device output should be in the high-impedance state.
15. During this period, the I/Os are in the output state and input signals should not be applied.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled) [8, 12, 14, 16]



Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
9	CY7B185–9DC	D22	Commercial
	CY7B185–9PC	P21	
	CY7B185–9VC	V21	
10	CY7B185–10DC	D22	Commercial
	CY7B185–10PC	P21	
	CY7B185–10VC	V21	
	CY7B185–10DMB	D22	Military
	CY7B185–10LMB	L54	
12	CY7B185–12DC	D22	Commercial
	CY7B185–12PC	P21	
	CY7B185–12VC	V21	
	CY7B185–12DMB	D22	Military
	CY7B185–12LMB	L54	
15	CY7B185–15DC	D22	Commercial
	CY7B185–15PC	P21	
	CY7B185–15VC	V21	
	CY7B185–15DMB	D22	Military
	CY7B185–15LMB	L54	

Shaded area contains preliminary information.

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7B186–12PC	P15	Commercial
15	CY7B186–15PC	P15	Commercial
	CY7B186–15DMB	D16	Military

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