Ordering number : ENA0797

SANYO Semiconductors
DATA SHEET

LA6261D — Monolithic Linear IC For Optical Disk Applications 6-chnnel Driver

Overview

The LA6261D is a 6-channel driver (BTL: 4ch, H-bridge: 2ch) developed for use in optical disk applications.

Functions

- Power amplifier 4-channel (BTL), 2-channel (H-bridge) built-in
- I_O max 700mA (Each channel)
- Level shift circuit built-in (BTL AMP)
- Overheat protection circuit (thermal shutdown) built-in
- Separate power supply for H-bridge (2ch)
- 3.3V regulator controller incorporated (output transistor provided externally)
- With each H-bridge output control pin

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		14	V
Maximum output current	I_O max	Each channel for ch1 to ch6	0.7	A
Maximum input voltage	$V_{IN}B$		13	V
Mute pin voltage	V_{MUTE}		13	V
Allowable power dissipation	Pd max	Independent IC	1.2	W
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		5.6 to 13	V

Electrical Characteristics at Ta = 25°C, $V_{CC}1=V_{CC}2=8V$, VREF=1.65V, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
All Blocks						
No-load current drain ON	I_{CC}-ON	All outputs ON *1 FWD = REV = 0V		30	50	mA
VREF Input voltage range	VREF-IN		1		VCC-1.5	V
BTL AMP Block						
Output offset voltage	V_{OFF}	Voltage difference between channels	-50		50	mV
Input voltage range	V_{IN}	Input to V_{IN}1,2,3 and 4	0		VCC	V
Output voltage (Saturated)	V_O	Voltage between each V_O^+ and V_O^- with R_L = 8Ω	4	5		V
Closed-circuit voltage gain	VG	Gain between input and output		4		Times
Input voltage for MUTE ON	V_{MT}ON	*3	2		SVCC	V
Input voltage for MUTE OFF	V_{MT}OFF	*3	0		0.5	V
Slew rate	SR	×2 between the amp and output		0.5		V/μs
H Bridge Block						
Output voltage (Saturated)	V_O-LOAD	Voltage between each V_O^+ and V_O^- with R_L=10Ω *2	6.2	6.7		V
Input low-level	V_{IN}-L		0		1	V
Input high-level	V_{IN}-H		2		SVCC	V
Output voltage (Controlled)	V_{CONT}	Voltage between each V_O^+ and V_O^- with V_{CONT} = 3V and R_L = 10Ω		2.8		V
Regulator Block						
Output voltage	Vreg	I_L = 100mA	3.05	3.3	3.55	V
Fluctuating output load	ΔV_{RL}	I_L = 0 to 200mA	-50	0	10	mV
Fluctuating supply voltage	ΔVv_{CC}	V_{CC} = 6 to 12V, I_L = 100mA	-15	21	60	mV

*1 Total current dissipation of SV_{CC}, $PV_{CC}1$ and $PV_{CC}2$ at no load.

*2 Output in the saturated condition.

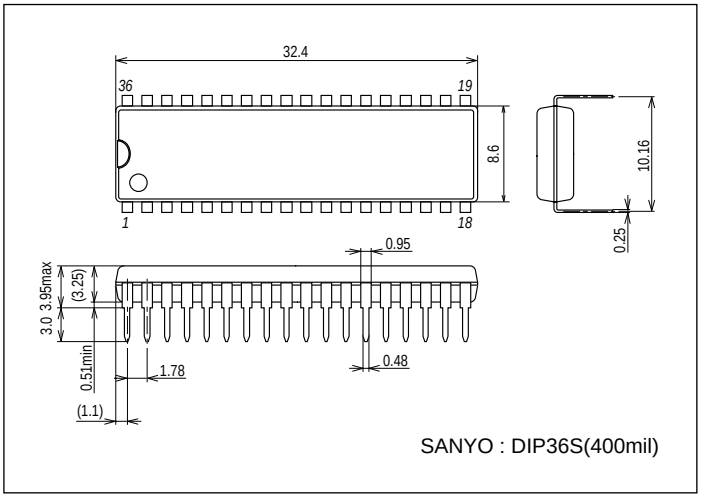
*3 BTL output ON with MUTE: [H] and BTL output OFF (HI impedance) with MUTE: [L].

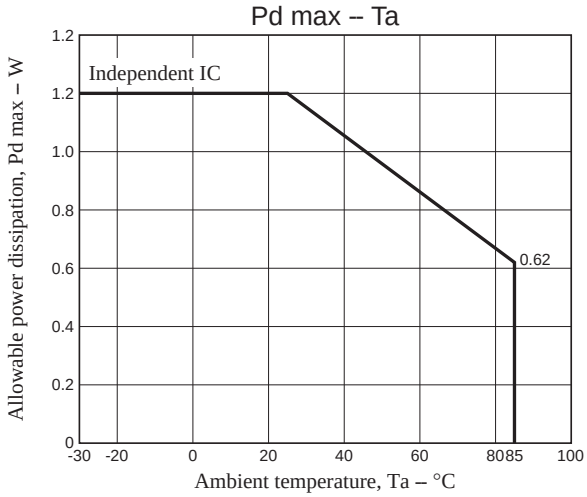
*4 Design value

Package Dimensions

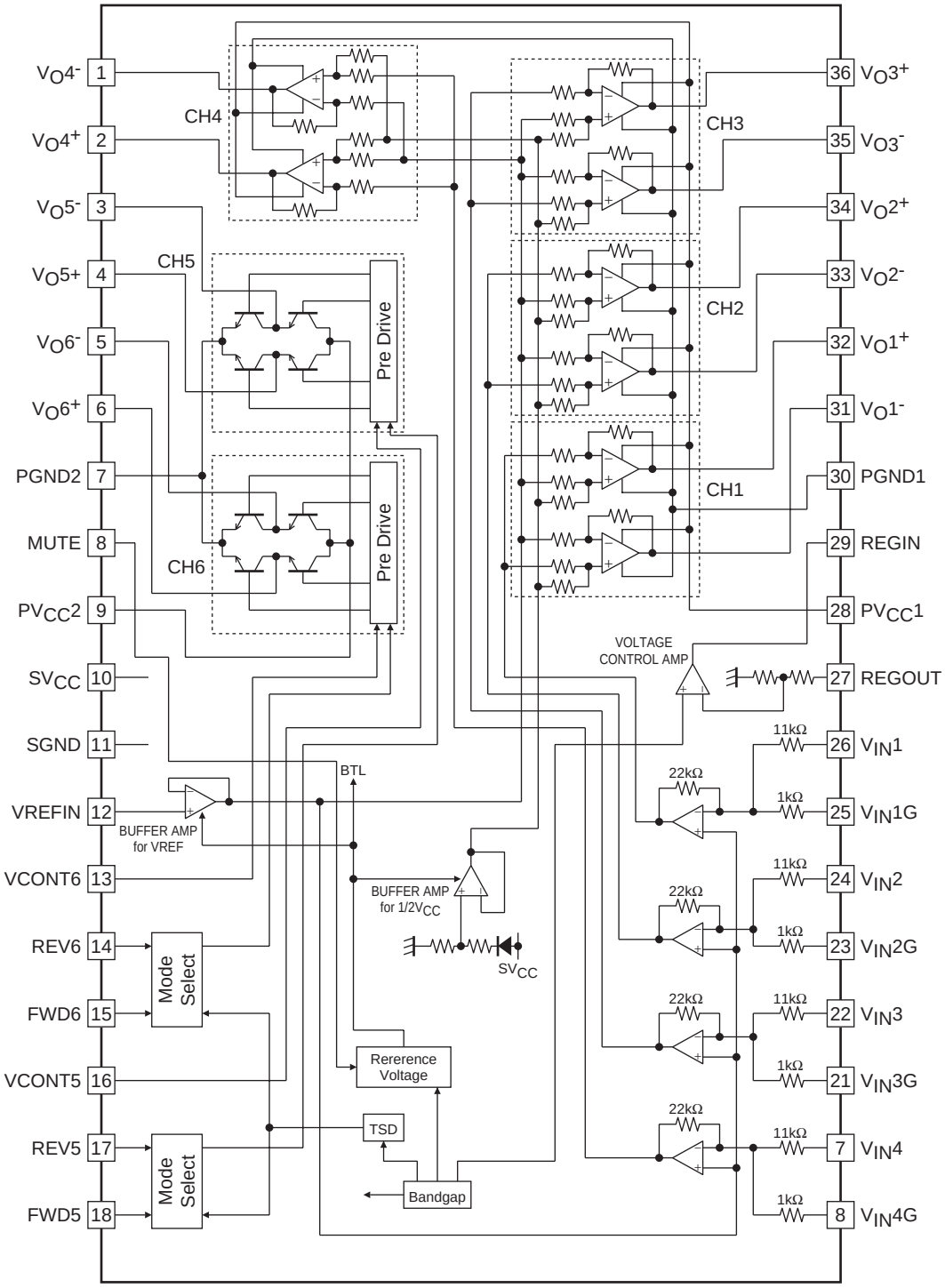
unit : mm (typ)

3170A

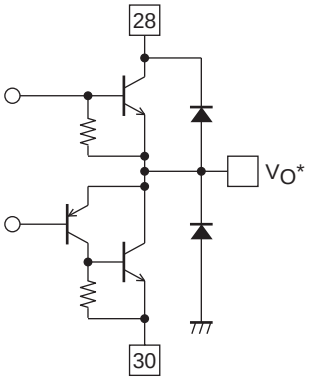
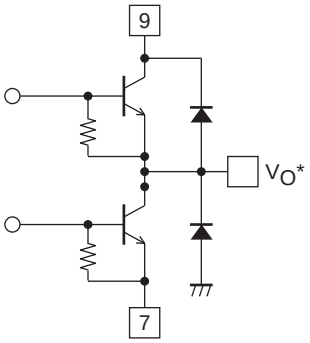
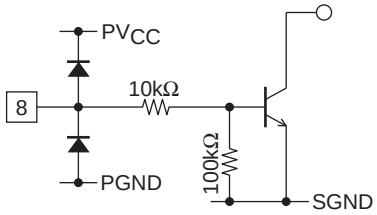
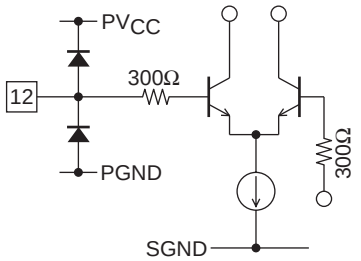
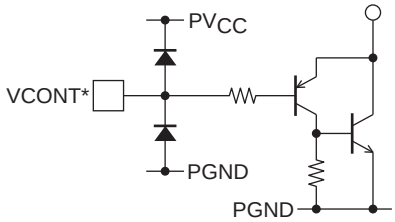
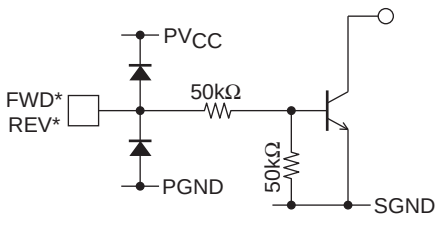




Block Diagram



Pin Function

Pin No.	Pin Name	function	Equivalent circuit
1 2 28 30 31 32 33 34 35 36	V_O4^- V_O4^+ $PV_{CC}1$ PGND1 V_O1^- V_O1^+ V_O2^- V_O2^+ V_O3^- V_O3^+	BTL Output pin (-) for channel 4 BTL Output pin (+) for channel 4 Power for channels 1,2,3 and 4 (BTL), (SV_{CC} short-circuited) Power GND for channels 1,2,3 and 4 (BTL) BTL Output pin (-) for channel 1 BTL Output pin (+) for channel 1 BTL Output pin (-) for channel 2 BTL Output pin (+) for channel 2 BTL Output pin (-) for channel 3 BTL Output pin (+) for channel 3	
3 4 5 6 7 9	V_O5^- V_O5^+ V_O6^- V_O6^+ PGND2 $PV_{CC}2$	H-bridge Output pin (-) for channel 5 H-bridge Output pin (+) for channel 5 H-bridge Output pin (-) for channel 6 H-bridge Output pin (+) for channel 6 Power GND for channels 5 and 6 (H-bridge) Power for channels 5 and 6 (H-bridge)	
8	MUTE	Input pin for BTL mute	
12	VREFIN	Reference voltage input pin	
13 16	VCONT6 VCONT5	Input pin for CH6 output voltage control Input pin for CH5 output voltage control	
14 15 17 18	REV6 FWD6 REV5 FWD5	CH6 Output change pin (REV), Logic input for H bridge CH6 Output change pin (FWD), Logic input for H bridge CH5 Output change pin (REV), Logic input for H bridge CH5 Output change pin (FWD), Logic input for H bridge	

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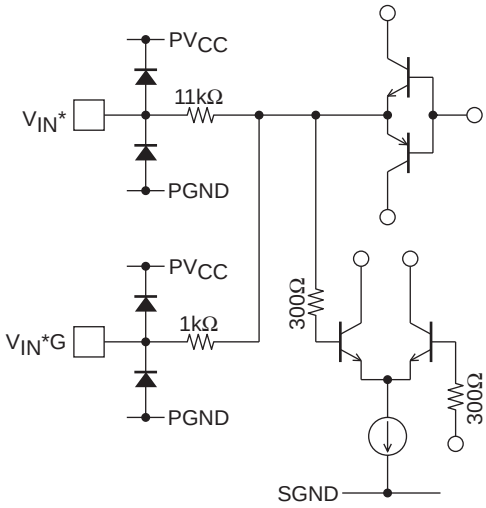
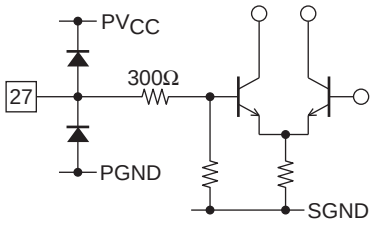
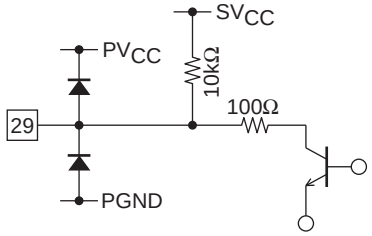
Pin No.	Pin Name	function	Equivalent circuit
19 20 21 22 23 24 25 26	$V_{IN}4G$ $V_{IN}4$ $V_{IN}3G$ $V_{IN}3$ $V_{IN}2G$ $V_{IN}2$ $V_{IN}1G$ $V_{IN}1$	Input pin for channel 4 (for gain control) Input pin for channel 4 Input pin for channel 3 (for gain control) Input pin for channel 3 Input pin for channel 2 (for gain control) Input pin for channel 2 Input pin for channel 1 (for gain control) Input pin for channel 1	
27	REGOUT	Regulator pin (External PNP collector)	
29	REGIN	Regulator pin (External PNP base)	

Truth Table (H Bridge)

INPUT		OUTPUT	
FWD5(6)	REV5(6)	$V_O5(6)^+$	$V_O5(6)^-$
L	L	Z	Z
L	H	H	L
H	L	L	H
H	H	L	L

Application Circuit Example