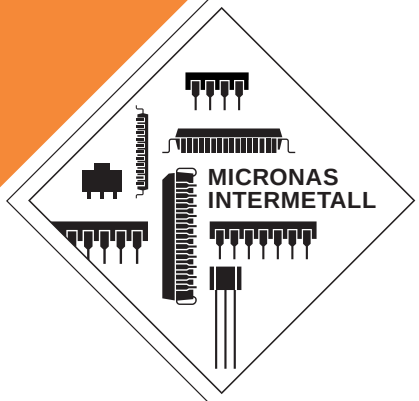

DMI 3110 A
Digital MAC Interface

Edition Nov. 8, 1996
6251-381-2DS

MICRONAS
INTERMETALL

Contents

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DMI 3110 A Digital MAC Interface

1. Introduction

The DMI 3110 A is a D2MAC interface implemented in CMOS technology and housed in a 68-pin PLCC package. It delivers analog RGB signals, a PAL-coded composite video signal (CVBS) and separate PAL-coded luminance and chrominance signals for SVHS. Also included is an 8-bit A/D converter for digitizing the analog D2MAC signal and a digital interface to the Intermetall D2MAC chip set. The main features are:

– 8-bit A/D converter with clamping and AGC

– Clock generation with digital PLL

– Teletext Transcoding MAC to PAL (VBI)

– PAL encoder with OSD and Teletext insertion

– 3 D/A converters for CVBS, Y, C

– 3 D/A converters for RGB or YUV with OSD insertion

– I^2C-Bus interface for communication with the CCU

2. Functional Description

The following text describes the functions of the DMI. The descriptions refer to the block diagram.

2.1. Clock Generation

The complete chip runs with a 20.25 MHz clock. This clock is produced by the clock generation circuitry. The clock generator comprises a 20.25 MHz crystal oscillator that is digitally controlled within ± 150 ppm with 9-bit resolution. The frequency will be controlled by two switched capacitors. The input signal for the control loop is generated in the D2MAC decoder IC. The clock output signal itself is fed to the D2MAC chips.

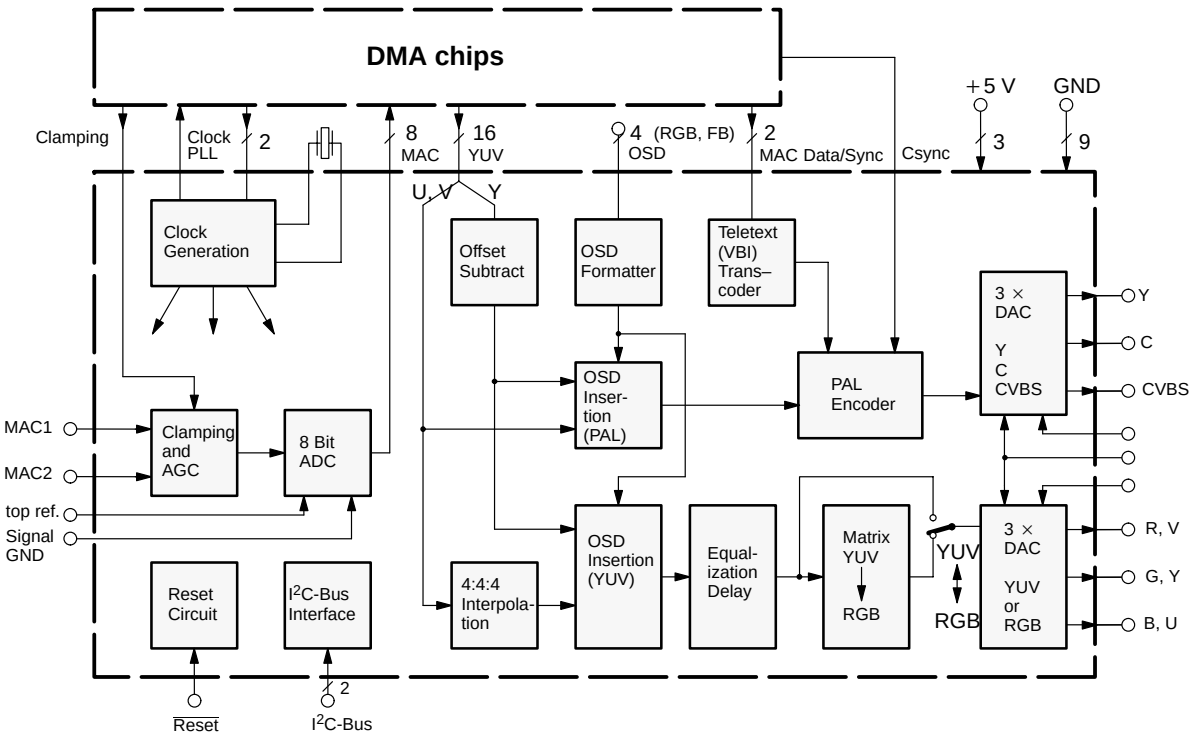


Fig. 2–1: DMI Block Diagram

2.2. Automatic Gain Control

The AGC circuit controls the gain for the analog input signal and feeds the controlled signal to the following A/D converter. The input voltage can vary in the range from 0.5 V_{pp} to 2 V_{pp} (1 $V_{pp} \pm 6$ dB). The amplitude of the A/D converter output signal will be measured in the D2MAC decoder circuit and read from a central control unit (CCU) over the I^2C-bus to calculate the gain control signal. The measurement will be done in line 624, therefore the digital baseband input signal for the D2MAC decoder should not be influenced by other circuits during this line.

The gain control itself is done by a digital gain controlled amplifier in front of the A/D converter. The gain range of ± 6 dB is logarithmically scaled in 64 steps with a step size of 0.19 dB. As the control algorithm is done by software in the CCU, features of the AGC, such as histories and backlash functions can also be provided easily.

2.3. Clamping

The clamping circuit clamps the analog input signal to a fixed level. The offset value of the digital MAC signal is measured in the D2MAC decoder and the clamping signal is fed to the DMI circuit as 4-bit PDM (Pulse Density Modulated) signal. In the DMI a clamping current is generated for the coupling capacitors at the MAC inputs. For proper functioning of the clamping it is required to connect no circuit with an extra clamping function between the digital MAC output of the DMI and the input of the D2MAC decoder.

2.4. A/D Converter

The A/D converter is an 8-bit two-step flash converter which runs at 20.25 MHz. The output signal is purely binary-coded and is fed to the D2MAC decoder. Optionally, the signal can be selected to become Gray code format. The reference voltage is internally generated and is connected to one pin for a decoupling capacitor. The A/D converter (and the D/A converters) are connected to extra 5V and ground pins for a supply with a separate low-noise supply voltage. The analog MAC input signal must be AC-coupled over a coupling capacitor.

2.5. PAL Encoder

The PAL encoder receives the digital 4:2:2 component signal (YUV) from the D2MAC decoder. The encoder is also connected to the on-screen display (OSD) formatter and to the Teletext transcoder. These signals will be coded into a composite video signal in the PAL standard. Three D/A converters produce the composite video signal, the chrominance signal and the luminance signal.

2.6. Teletext Transcoder

The DMI can handle D2MAC Teletext signals transmitted in the vertical blanking interval (VBI). In the transcoder, the Teletext signal is extracted from the D2MAC data signal. The data rate and signal timing are converted according to the WST Teletext standard. Teletext transcoding is active in TV lines 6 to 22 and 319 to 335 of the PAL signal. Thus not all lines that can carry Teletext in the D2MAC standard (2 to 22 and 314 to 334) are transcoded.

A generator in the transcoder generates the correct Teletext bit frequency. A programmable window for enabling the Teletext transcoding will be available. The start and stop times of this window can be programmed between lines 6 and 22 (319 and 335) to span all Teletext lines in the PAL standard. For proper synchronization the MAC Sync signal from the D2MAC decoder will be used.

2.7. OSD Formatter and Insertion

An external on-screen signal (e.g. from the TPU 2735) can be fed into the DMI. The signal is 3×1 bit RGB and Fast Blanking. These input signals are sampled with the double clock frequency and processed with a downsampling filter to the single clock frequency. In the OSD formatter the 3-bit RGB signals are converted to YUV component signals, 6 bit for Y, 5 bit for U and 5 bit for V. This is done in a user-programmable RAM with a size of 8×16 bit. Contrast, brightness and saturation of the OSD can be programmed in this way. The output signal of the OSD formatter is fed into the PAL encoder and into the RGB/YUV outputs. The OSD can be switched off separately for PAL and RGB/YUV.

2.8. Luminance Offset Subtracter

The digital luminance signal coming from the D2MAC decoder has an offset of + 16. This means that the black level is shifted to this value. At the luminance input of the DMI 3110 A a value of 16 can be subtracted from the luminance signal. Therefore, the range of the luminance signal is from 0 to 238. The D/A output range is set to 0.75 V for full-scale (255) input, hence the amplitude of 238 gives 0.7 V at the output.

2.9. Equalization Delay

The PAL encoder has a processing delay of some microseconds. For a time matching between the analog RGB signals and the Y, C and CVBS signals an equalization delay exists. This delay is adjustable because the encoder delay depends on the filter settings.

2.10. 4:4:4 Interpolation

The component signal from the D2MAC decoder is in 4:2:2 format. Before this signal is converted to RGB, the U and V components are upsampled to the full clock frequency of 20.25 MHz. This is done by demultiplexing the U and V signals and by interpolation of the signal with a FIR filter. The frequency response and step response are shown in Fig. 2–2.

2.11. Matrix

A digital matrix converts the 4:4:4 YUV signal to a RGB signal. The matrix can be switched off for outputting YUV signals. The matrix coefficients are fixed and have the following values:

$R = Y + 0 \times U + \quad 1.079 \times V$
$G = Y - 0.265 \times U - \quad 0.549 \times V$
$B = Y + 1.364 \times U + \quad 0 \times V$

2.12. D/A Converters

There are six D/A converters in the DMI. Three of them output the RGB or YUV signals, one is for the composite video signal, one for the chrominance signal and one for the luminance signal. The signal delay time of all converters is matched. The minimum load resistor for the nominal output voltages is 75 Ω .The converters consist of current sources from the analog supply voltage VSUPA. With a digital zero input all current sources are switched to ground and the maximal current flows internally. In this case the D/A converters have the maximal power dissipation. At maximal input signal all current sources are switched to the output pin and the current flows over the external load resistor to ground. The outputs are short-circuit protected.

The maximal output currents can be adjusted in a range from 25% to 100% of the values in the table below. The adjustment is done with two reference resistors. One of them is responsible for the RBG converters, the other one for the Y, C and CVBS converters. At 25% of the current the load resistance has to be 300 Ω to get the correct output voltage. The output voltage should not exceed a value of approx. 1.4 V because at higher values the D/A converter characteristic becomes nonlinear.

If all six D/A converters are used, the load resistance has to be 300 Ω in order to not exceed the maximum power dissipation of 1.325 W for the existing package.

For lower load resistances (higher power dissipation) the package has to be cooled.

For a lower power dissipation the unused group of D/A converters can be switched off by removing the corresponding reference resistor.

Table 2–1: Specifications of the D/A converters

Signal	Resolution	Max. Current	V_{OUTMAX} at 75 Ω
CVBS	9-bit	16.5 mA	1.24 V
Luma	9-bit	16.5 mA	1.24 V (1 V nominal)
Chroma	9-bit	16.5 mA	1.24 V (0.8 V_{pp} nominal)
R, G, B	8-bit	10.0 mA	0.75 V

2.13. I²C-Bus Interface

All parameters of the DMI 3110 A are programmed via an I²C-bus interface. The interface uses an IC address and one level of subaddress. The programming of the DMI 3110 is explained in detail in section 4.

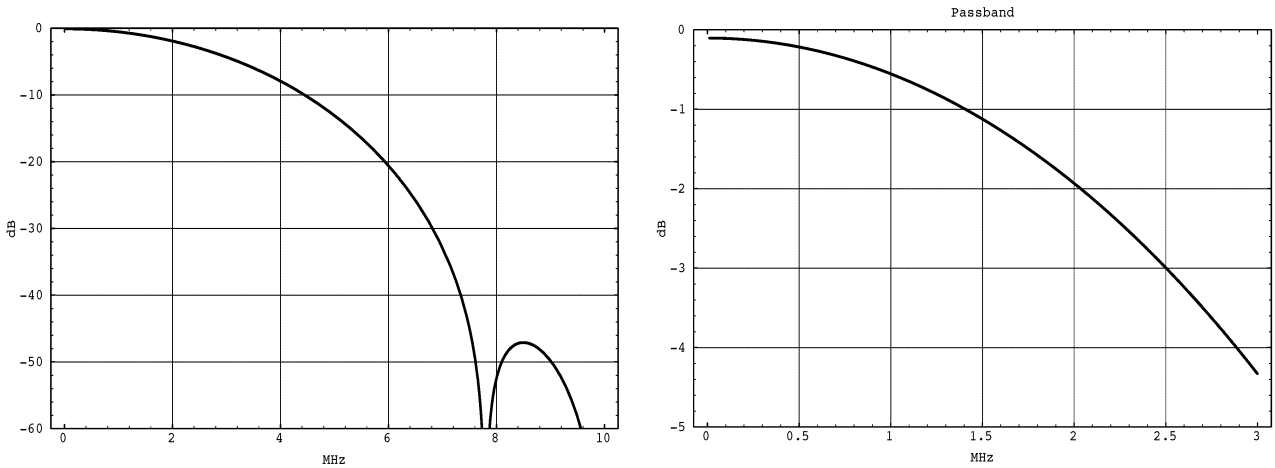


Fig. 2–2: 422 → 444 Chroma Interpolation Filter

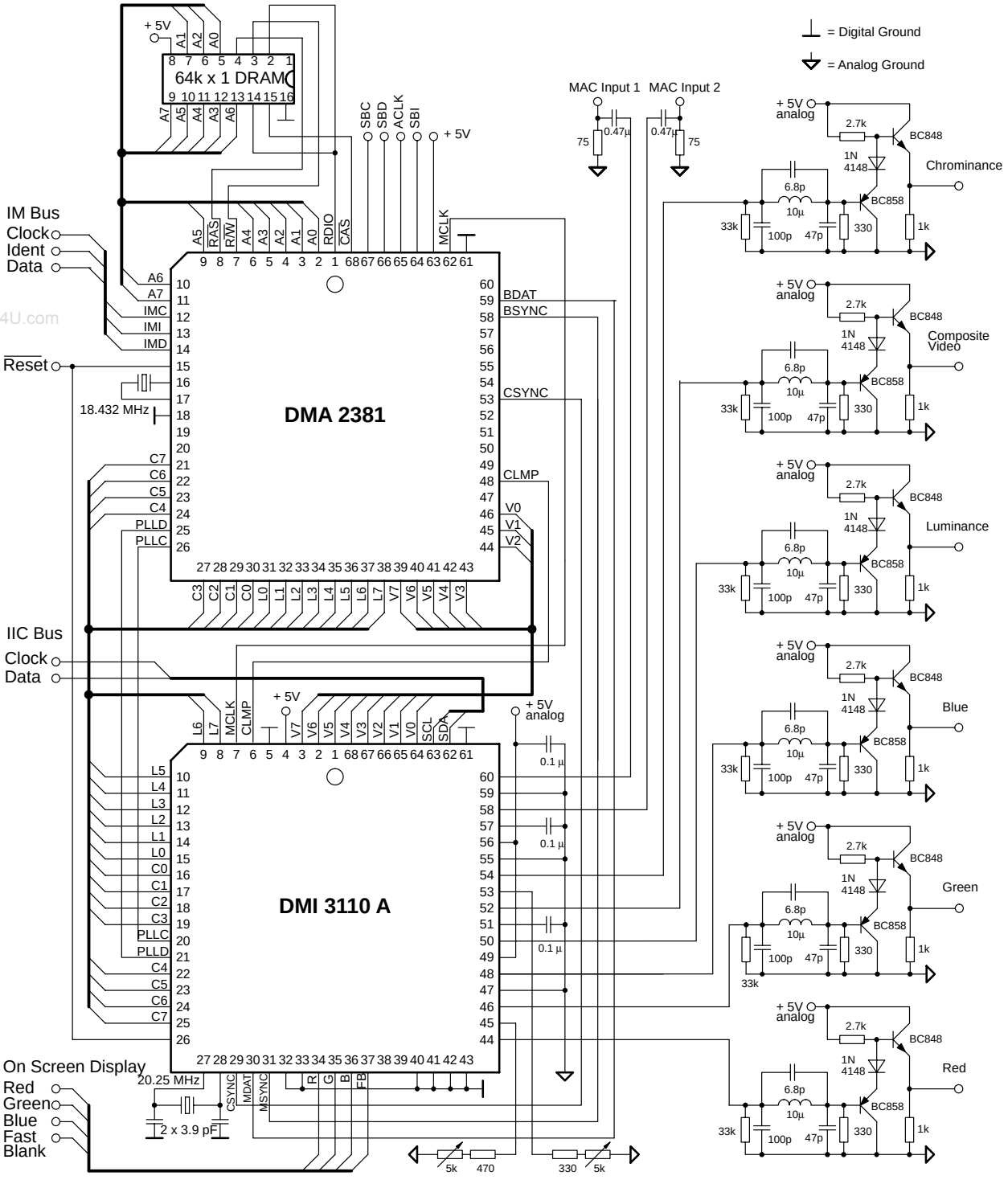
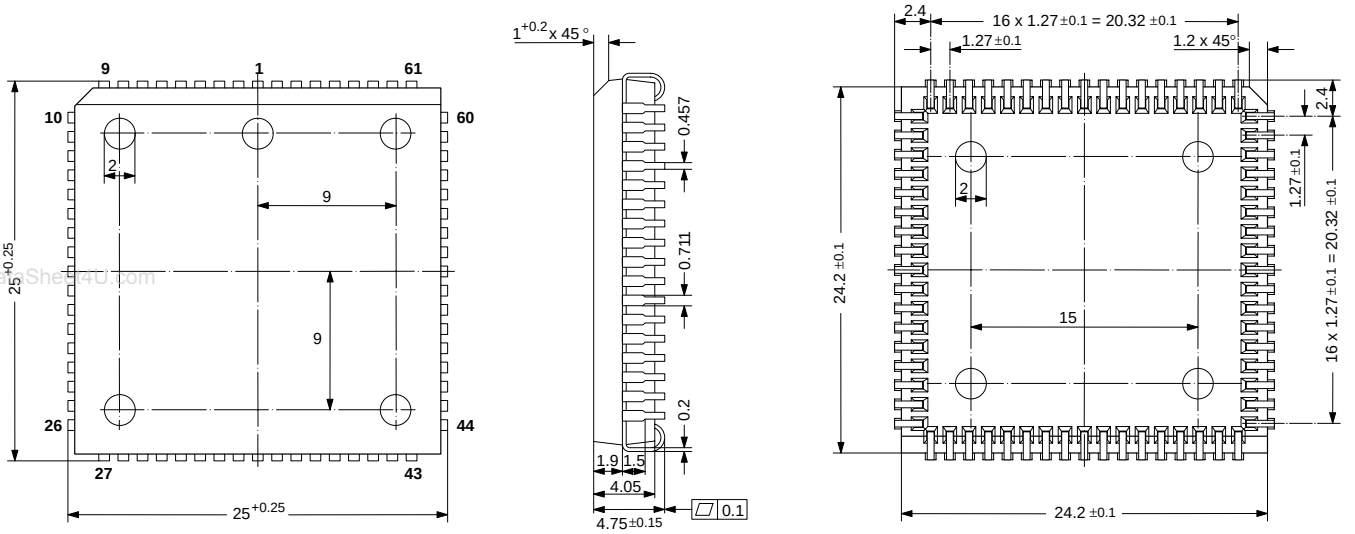


Fig. 2–3: Application circuit

3. Specifications

3.1. Outline Dimensions



70043/2

Fig. 3–1:
68-Pin Plastic Leaded Chip Carrier Package
(PLCC68)
Weight approximately 4.8 g
Dimensions in mm

3.2. Pin Connections and Short Descriptions

NC = not connected; leave vacant
LV = if not used, leave vacant
X = obligatory, connect as described in circuit diagram

Pin No. PLCC 68-pin	Connection (if not used)	Pin Name	Type	Short Description
1	LV	BO5	OUT	Digital Baseband Output 5
2	LV	BO6	OUT	Digital Baseband Output 6
3	LV	BO7	OUT	Digital Baseband Output 7 (MSB)
4	X	VSUPD	SUP	Digital Supply Voltage
5	X	GNDD	SUP	Digital Ground
6	GNDD	CLMP	IN	Clamping Input
7	LV	MCLK	OUT	Main Clock Output
8	GNDD	LI7	IN	Digital Luma Input 7 (MSB)
9	GNDD	LI6	IN	Digital Luma Input 6
10	GNDD	LI5	IN	Digital Luma Input 5
11	GNDD	LI4	IN	Digital Luma Input 4
12	GNDD	LI3	IN	Digital Luma Input 3
13	GNDD	LI2	IN	Digital Luma Input 2

Pin Connections and Short Descriptions, continued

Pin No.	Connection (if not used)	Pin Name	Type	Short Description
14	GNDD	LI1	IN	Digital Luma Input 1
15	GNDD	LI0	IN	Digital Luma Input 0 (LSB)
16	GNDD	CI0	IN	Digital Chroma Input 0 (LSB)
17	GNDD	CI1	IN	Digital Chroma Input 1
18	GNDD	CI2	IN	Digital Chroma Input 2
19	GNDD	CI3	IN	Digital Chroma Input 3
20	GNDD	PLLC	IN	PLL Tuning Clock Input
21	GNDD	PLLD	IN	PLL Tuning Data Input
22	GNDD	CI4	IN	Digital Chroma Input 4
23	GNDD	CI5	IN	Digital Chroma Input 5
24	GNDD	CI6	IN	Digital Chroma Input 6
25	GNDD	CI7	IN	Digital Chroma Input 7 (MSB)
26	X	RESQ	IN	$\overline{\text{Reset}}$ Input
27	X	XTAL1	OUT	Crystal 1 (Output)
28	X	XTAL2	IN	Crystal 2 (Input)
29	VSUPD	CSYNC	IN	Composite Sync Input
30	GNDD	MDAT	IN	MAC Data Input
31	VSUPD	MSYNC	IN	MAC Sync Input
32	X	TMODE	IN	Test Mode 1
33	X	TLAT	IN	Test Mode 2
34	GND	OSDR	IN	On-screen Display Red Input
35	GND	OSDG	IN	On-screen Display Green Input
36	GND	OSDB	IN	On-screen Display Blue Input
37	GND	OSDFB	IN	On-screen Display Fast Blank Input
38	X	TESTOP1	OUT	Test Mode 3
39	X	TESTOP2	OUT	Test Mode 4
40	X	CKMODE	IN	Test Mode 5
41	X	TCKIN	IN	Test Mode 6
42	X		–	Not Connected
43	X	GNDCON	SUPPLY	Ground Connection
44	GNDDA	ROUT	OUT	Analog Red or V-Component Output

Pin Connections and Short Descriptions, continued

Pin No.	Connection (if not used)	Pin Name	Type	Short Description
45	X	RREFR	REF	Reference R for RGB DACs
46	GNDDA	GOUT	OUT	Analog Green or Luminance Output
47	X	GNDDA	SUPPLY	Analog Ground D/A Converters
48	GNDDA	BOUT	OUT	Analog Blue or U-Component Output
49	X	VSUPDA	SUPPLY	Analog Supply Voltage DACs
50	GNDDA	YOUT	OUT	Analog Luminance Output
51	X	CREFDA	REF	Reference Capacitor for DACs
52	GNDDA	CVBSOUT	OUT	Analog Composite Video Output
53	X	RREFY	REF	Reference R for Y, C, CVBS DACs
54	GNDDA	COUT	OUT	Analog Chrominance Output
55	X	GNDAD	SUPPLY	Analog Ground A/D Converters
56	X	VSUPAD	SUPPLY	Analog Supply Voltage ADC
57	X	VREFT	REF	Top Reference Voltage ADC
58	VREFT	MAC2	IN	MAC Input 2
59	X	GNDSIG	IN	Signal Ground ADC
60	VREFT	MAC1	IN	MAC Input 1
61	X	GNDSUB	SUPPLY	Substrate Voltage
62	X	SDA	IN/OUT	I^2C-Bus Serial Data Input/Output
63	X	SCL	IN	I^2C-Bus Serial Clock Input
64	LV	BO0	OUT	Digital Baseband Output 0 (LSB)
65	LV	BO1	OUT	Digital Baseband Output 1
66	LV	BO2	OUT	Digital Baseband Output 2
67	LV	BO3	OUT	Digital Baseband Output 3
68	LV	BO4	OUT	Digital Baseband Output 4

3.3. Pin Descriptions

Pin 1 to 3 and 64 to 68 – Digital Baseband Outputs (Interface to DMA, see Fig. 3-9):
Via these pins the DMA circuits will be supplied with the digitized MAC baseband signal. The code of the signal is 8-bit pure binary.

Pin 4 – Digital Supply Voltage:
This pin supplies all digital stages and has to be connected with the positive supply voltage.

Pin 5 – Digital Ground:
This is the common ground connection of all digital stages and has to be connected with the ground of the power supply.

Pin 6 – Clamping Input (Interface to DMA, Fig. 3–3):
To this pin the DMA supplies a PDM (Pulse Density Modulated) signal for clamping the analog MAC baseband signal at the input of the AGC amplifier. This pin has to be connected to pin 48 of the DMA circuit.

Pin 7 – Main Clock Output (Supply of DMA and others, Fig. 3–10):
This pin is the output of the main clock generator. The clock generator drives all circuits with the synchronized clock signal. The clock frequency is 20.25 MHz.

Pin 8 to 15 – Digital Luma Inputs (Interface to DMA, Fig. 3–2):
Via these pins the DMI gets the digital luminance signal in 8-bit pure binary code from the DMA circuit. All bits equal to zero means black, all bits equal to one means white.

Pins 16 to 19 and 22 to 25 – Digital Chroma Inputs (Interface to DMA, Fig. 3–2):
Via these pins the DMI gets the digital chrominance signal from the DMA circuit. The code is 8-bit two's complement. The components U and V are multiplexed, which means that the data rate of each component signal is 10.125 MHz.

Pin 20 – PLL Tuning Clock Input
(Interface to DMA, see Fig. 3–3):
This pin gets the clock for the PLL tuning data signal from the DMA. This pin has to be connected with the pin 26 of the DMA circuit.

Pin 21 – PLL Tuning Data Input (Interface to DMA, Fig. 3–3):
This pin gets the data signal for the clock generation PLL from the DMA. The signal is a 12-bit serial data word which will be loaded into a shift register. The data contains the information for the frequency adjustment of the clock generator. The data format is compatible with the MCU 2600 clock generator. The clock phase will be compared with the phase of the MAC signal clock in the DMA circuit. This pin has to be connected with pin 25 of the DMA circuit.

Pin 26 – $\overline{\text{Reset}}$ Input (Fig. 3–4):
A low signal at this pin generates a reset. The low-high transition of this signal should come when the supply voltage is stable (power-on reset). The input has Schmitt trigger characteristics.

Pin 27 and 28 – XTAL 1/2 (Fig. 3–8):
The 20.25 MHz crystal is connected with these two pins. Pin 27 is the input and pin 28 is the output of the oscillator circuit. Both pins need an external capacitor to ground.

Pin 29 – Composite Sync Input (Interface to DMA, Fig. 3–2):
This pin gets the composite sync signal from the DMA. This signal is used as synchronization signal in the PAL coder of the DMI and has to be connected to pin 53 of the DMA circuit.

Pins 30 and 31 – MAC Data and Sync Input (Interface to DMA, Fig. 3–3):
Via this pin the VBI Teletext signal will be supplied from the DMA. The burst data signal contains the binary teletext data in lines 2 to 22 and lines 314 to 334 of the D2MAC signal. The burst sync signal synchronizes the teletext data. Pin 30 has to be connected to pin 59 and pin 31 has to be connected to pin 58 of the DMA circuit.

Pins 32, 33, 38 to 41 – Test Pins:
These pins are for test purposes only. In normal operation the pins 32, 33, 40, and 41 have to be connected to ground.

Pins 34 to 37 – On-screen Display Inputs (Fig. 3–3):
Via these pins the DMI will be supplied with the on-screen signals. Three inputs are for the one-bit RGB signals, the fourth input is for the fast blanking signal. A high level at the fast blanking input enables the OSD signal. This can be inserted (switchable) into all analog output signals of the DMI. The input signals are sampled with twice the clock frequency (40.5 MHz).

Pin 43 – Ground Connection:
This pin has some internal shielding function. It has to be connected to ground.

Pin 44, 46, 48, 50, 52, 54 – Analog Outputs (Fig. 3–5):
These are the outputs of the six D/A converters. The D/A converters are current source types and deliver output currents from VSUPA to ground. The nominal output voltages require 75 Ω load resistances. At higher load resistances the output voltages will increase, but will become nonlinear above approx. 2 V. The outputs are short-circuit protected.

Pin 45 and 53 – Reference Resistors D/A Converters (Fig. 3–6):
The reference currents for the D/A converters can be adjusted with a resistor from each of these pins to ground. With these resistors the output currents can be adjusted in the range of 25% to 100% of the maximal output currents. One resistor is responsible for the RGB D/A converters, the other one for the Y,C,CVBS D/A converters.

The nominal reference resistance value for a given load resistance can be seen in the table “recommended operating conditions”.

Pin 47 and 55 – Analog Ground:
These are the ground pins for the A/D and the D/A converters and have to be connected to the ground of the power supply. Note: the layout of the printing circuit board should take into consideration the need for a relatively noise-free supply.

Pin 49 and 56 – Analog Supply Voltage:
These are the supply voltage pins for the A/D and the D/A converters and have to be connected to the positive supply voltage. Note: The layout of the printing circuit board should take into consideration the need for a relatively noise-free supply.

Pin 51 – Reference Capacitor D/A Converters (Fig. 3–6):
This pin is the internal reference for the D/A converters. It has to be connected to ground over a capacitor with a value of approx. 100 nF. The capacitor should be a type with a low inductance and a high insulation resistance.

Pin 57 – Top Reference Voltage A/D Converter (Fig. 3–7):
This pin is connected to the top end of the reference resistor chain of the A/D converter. The reference voltage is generated inside the DMI, therefore only a capacitor has to be connected to this pin. The cold end of the capacitor should be connected to the signal ground.

Pin 58 and 60 – MAC Inputs (Fig. 3–3):
These are the inputs of the A/D converter (respectively clamping circuit) and have to be supplied with the analog MAC signals. One of these inputs can be selected via I^2C-bus. The signal amplitude is nominal 1 V_{pp} and can vary by ± 6 dB. The input signals must be AC-coupled over a capacitor. The clamping time constant is proportional to the capacity.

Pin 59 – Signal Ground A/D Converter (Fig. 3–7):
This pin has to be connected to the ground of the analog input signal. The layout of the printing circuit board should take into consideration the need for a relatively noise-free signal ground potential.

Pin 61 – Substrate Voltage:
This is the connection to the substrate (platform) of the IC. It has to be connected to ground.

Pin 62 and 63 – I^2C-Bus Serial Clock and Data (Fig. 3–3):
These are the connections of the DMI with the I^2C-Bus. All adjustments are done via this bus and the information will be provided by a Central Control Unit (CCU).

3.4. Pin Configuration

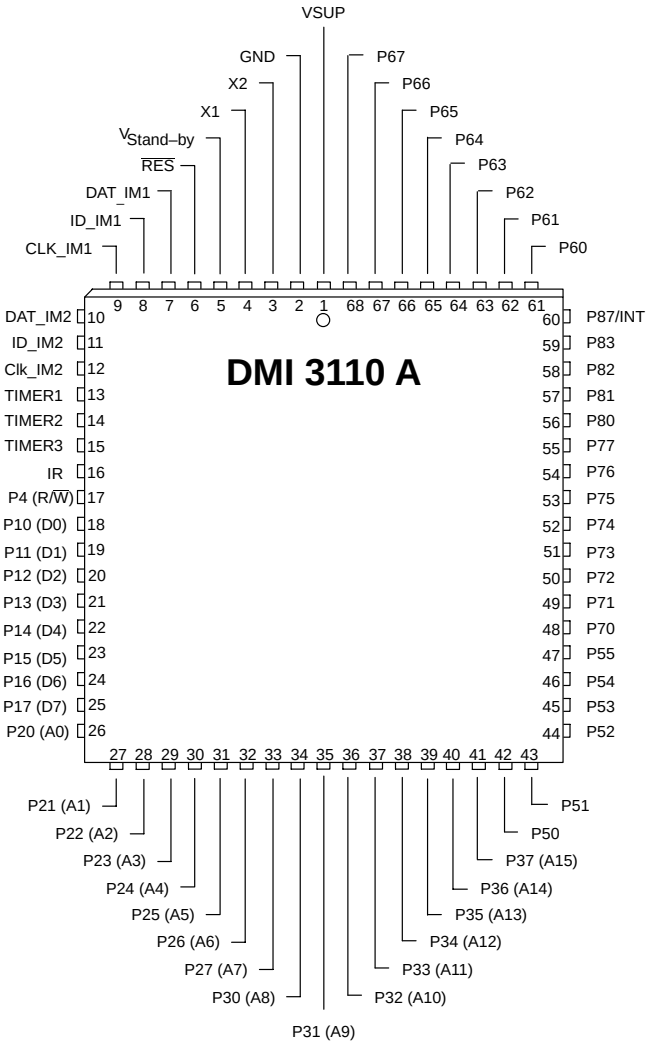


Fig. 3–2: Pinning of the DMI 3110 A in PLCC68 Package

3.5. Pin Circuits

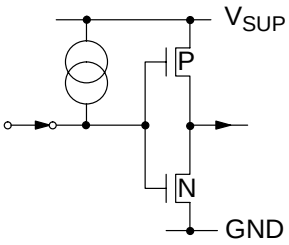


Fig. 3–3: Input pins 8 to 19, 22 to 25, 29

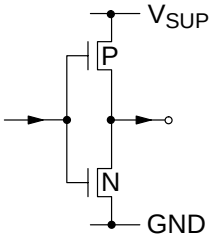


Fig. 3–4: Input pins 6, 20, 21, 30, 31, 34 to 37, 53, 60, 62, 63

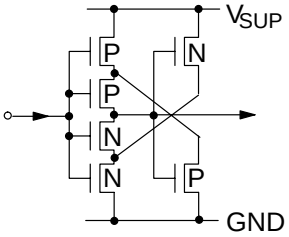


Fig. 3–5: Input pin 26

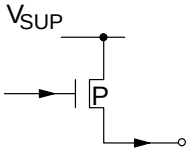


Fig. 3–6: Output pins 44, 46, 48, 50, 52, 54

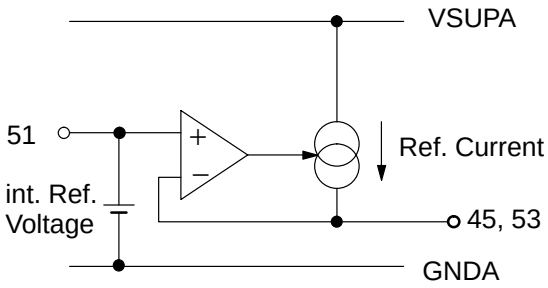


Fig. 3–7: Pins 45, 51, 53

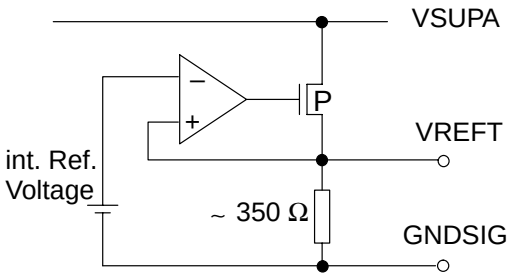


Fig. 3–8: Pins 57, 59

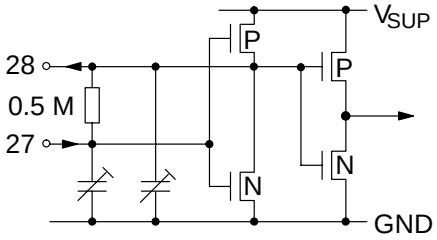


Fig. 3–9: Input pin 27, output pin 28

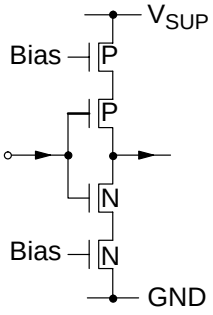


Fig. 3–10: Output pins 1 to 3, 64 to 68

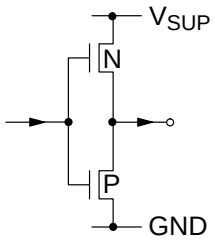


Fig. 3–11: Output Pin 7

3.6. Electrical Characteristics (pin numbers for 68-pin PLCC package)

3.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	65	°C
T_S	Storage Temperature	–	−40	125	°C
V_{SUP}	Supply Voltage	4, 49, 56	–	6	V
V_I	Input Voltage, all pins	–	−0.3	V_{SUP}	V
I_I	Input Current, all pins		−20	+20	mA
P_{TOT}	Chip Power Dissipation	–	–	1.325	W

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

3.6.2. Recommended Operating Conditions at V_{SUP}= 5 V, T_A= 0 °C to 65 °C

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{SUPD}	Digital Supply Voltage	4	4.75	5.0	5.25	V
V_{SUPA}	Analog Supply Voltage	49, 56	4.75	5.0	5.25	V
V_{MAC}	Analog MAC Input Voltage	58, 60	0.5	1.0	2.0	V_{SS}
C_{MACI}	Coupling Capacitance MAC Inputs		–	470	–	nF
C_{REFT}	Decoupling Capacitance Top Reference A/D Converter	57	–	10||10	–	nF|| µF
C_{REFD}	Decoupling Capacitance A/D Converter	51	–	100	–	nF
R_{REFR}	Reference Resistor RGB D/A Converter	45	1100	–	4400	Ω
R_{REFY}	Reference Resistor, Y, C, CVBS D/A Converter	53	680	–	2720	Ω
R_{LOAD}	Load Resistance D/A Converter	44, 46, 48, 50, 52, 54	0	75	300	Ω
V_{AMAX}	Maximum Output Voltage Range (all D/A converters)		–	–	1.4	V
V_{LCIL}	Digital Luma/Chroma Input Low Voltage	8 to 19, 22 to 25	–	–	0.4	V
V_{LCIH}	Digital Luma/Chroma Input High Voltage		2.4	–	–	V
t_{LCIST}	Digital Luma/Chroma Input Setup Time		10	–	–	ns
t_{LCIHT}	Digital Luma/Chroma Input Hold Time		0	–	–	ns

Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{OSDL}	OSD Input Low Voltage	34 to 37	–	–	0.2	V
V_{OSDH}	OSD Input High Voltage		0.6	–	–	V
t_{OSDSL}	OSD Input Setup Time at Falling Clock Edge		10	–	–	ns
t_{OSDHL}	OSD Input Hold Time at Falling Clock Edge		0	–	–	ns
t_{OSDSH}	OSD Input Setup Time at Rising Clock Edge		10	–	–	ns
t_{OSDHH}	OSD Input Hold Time at Rising Clock Edge		0	–	–	ns
V_{REIL}	$\overline{\text{Reset}}$ Input Low Voltage	26	–	–	0.8	V
V_{REIH}	$\overline{\text{Reset}}$ Input High Voltage		2.8	–	–	V
t_{REIL}	$\overline{\text{Reset}}$ Input Low Time		1	–	–	µs
V_{IIC}	I^2C-bus Input Low Voltage	62, 63	–	–	1.5	V
V_{IIC}	I^2C-bus Input High Voltage	62, 63	3.0	–	–	V

3.6.3. Crystal Oscillator (DCO) Characteristics (for TC09)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Recommended Crystal Characteristics					
T_A	Operating Ambient Temperature	0	–	65	°C
f_P	Parallel Resonance Frequency with Load Capacitance **C_L = 13 pF**	–	20.250	–	MHz
$\Delta f_P/f_P$	Accuracy of Adjustment	–20	–	+20	ppm
$\Delta f_P/f_P$	Frequency Temperature Drift	–30	–	+30	ppm
R_R	Series Resistance	–	–	25	Ω
C_0	Shunt (Parallel) Capacitance	3	–	7	pF
C_1	Motional (Dynamic) Capacitance	20	–	–	fF
Load Capacitance Recommendation					
C_L	External Load Capacitance **1)** from Pins 27 and 28 to Ground (pin names: XTAL_IN, XTAL_OUT)	–	2.2	–	pF
DCO Characteristics					
C_{ILmin}	Minimum Effective Load Capacity **2)**	–	9.5	–	pF
C_{ILrng}	Effective Load Capacity Range **2)**	–	7.5	–	pF

1) Remark on defining the External Load Capacitance:
External capacitors at each crystal pin to ground are required. They are necessary to tune the open-loop frequency of the internal PLL and to stabilize the frequency in closed-loop operation. The higher the capacitors, the lower the clock frequency results. The nominal free running frequency should match 20.250 MHz as closely as possible. Due to different layouts of customer PCBs the matching capacitor size should be defined in the application. The suggested value is a figure based on experience with various PCB layouts.
Tuning condition: VCOA = –25 (bits 7...0 of IM-bus register 14 of DMA 2281/DMA 2381)
2) DCO Range 128...384

3.6.4. Characteristics at V_{SUP}= 5 V, $T_{A=}$ 0 to 65 °C

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
I_{SUPD}	Current Consumption Digital	4	–	130	160	mA	V_{SUPD} = 5.0 V
I_{SUPAF}	Current Consumption Analog Front-End	56	–	50	70	mA	V_{SUPAF} = 5.0 V
I_{SUPAB}	Current Consumption Analog Back-End	49	–	30	35	mA	V_{SUPAB} = 5.0 V R_{REFY} = 2720 Ω R_{REFR} = 4400 Ω R_{LOAD} = 6 × 300 Ω
			–	110 [1]	130 [1]	mA	V_{SUPAB} = 5.0 V R_{REFY} = 680 Ω R_{REFR} = 1100 Ω R_{LOAD} = 6 × 75 Ω
P_{TOT}	Total Power Dissipation	–	–	1050	1325	mW	V_{SUPAB} = 5.0 V R_{REFY} = 2720 Ω R_{REFR} = 4400 Ω R_{LOAD} = 6 × 300 Ω
			–	1450 [1]	1800 [1]	mW	V_{SUPAB} = 5.0 V R_{REFY} = 680 Ω R_{REFR} = 1100 Ω R_{LOAD} = 6 × 75 Ω
FRONT-END							
V_{REFT}	A/D Converter Top Reference Voltage	57	2.55	2.7	2.85	V	
R_{MAC}	Analog Input Impedance	58, 60	1	–	–	MΩ	
C_{MAC}	Analog Input Capacitance		–	5	–	pF	
I_{CLMP}	Analog Input Clamping Current range		+14 –12	+17 –15	+20 –18	µA µA	full range, divided into 17 steps of 2 µA offset +1 µA
V_{MAC}	MAC Input Voltage Full Range		0.9	1.0	1.1	V_{PP}	AGC= 0dB (code 32)
G_{MAC}	AGC Range	In: 58, 60 Out: 1...3, 64...68	±6	±7	±8	dB	full range divided into 64 steps
DN_{AGC}	AGC Differential Nonlinearity		–	0.8	–	LSB	
B_{MAC}	Frontend –3 dB Bandwidth at 100 % Signal		7.5	8	–	MHz	f_{MCLK} = 20.25 MHz AGC= –6 dB (code 0)
SND_{MAC}	Frontend Signal to Noise and Distortion Ratio at 100 % Signal		42	44	–	dB	1 MHz sine input AGC= –6 dB (code 0) Bandwidth = fs/2
THD_{MAC}	Total Harmonic Distortion at 100 % Signal		–42	–48	–	dB	1 MHz sine input AGC= –6 dB (code 0) Bandwidth = 6 MHz
$PSRR_{MAC}$	Power Supply Rejection Ratio at MAC Input		–	46	–	dB	$\Delta V_{SUPAD}/\Delta V_{MAC}$ at DC AGC= 0 dB (code 32)
IN_{MAC}	MAC Input Integral Non-linearity		–	±2	–	LSB	
DN_{MAC}	MAC Input Differential Non-linearity		–	±0.8	–	LSB	
CT_{MAC}	Analog Input Adjacent Cross-talk MAC1/MAC2		–	–55	–50	dB	Input1 = 1 MHz 80 % signal Input2 = 1.1 MHz 80 % signal

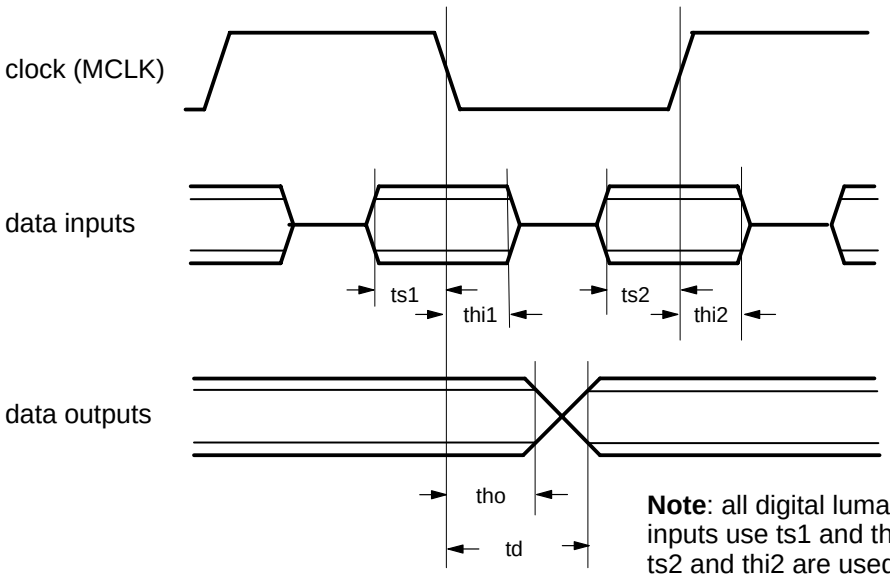
[1] Cooling required.

Characteristics, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
BACK-END							
V_{REF}	Reference Voltage for all D/A converters	51	1.9	2.1	2.3	V	V_{SUPA} = 4.75 to 5.25 V to be measured with $R_j \geq 1$ G Ω
$-I_{OUTY}$	Maximum Analog Output Current CVBS, Y, C	50, 52, 54	15.6	16.5	17.3	mA	R_{REFY} = 680 Ω R_L = 0
			–	4.1	–	mA	R_{REFY} = 2720 Ω R_L = 0
$-I_{OUTR}$	Maximum Analog Output Current R, G, B	44, 46, 48	9.5	10	11	mA	R_{REFR} = 1100 Ω R_L = 0
			–	2.5	–	mA	R_{REFR} = 4400 Ω R_L = 0
ID_{OUTR}	Output Deviation between R, G and B peak–to–peak current		–	3	6	%	$100(I_{MAX} - I_{MIN})/I_{MEAN}$ R_{REFR} = 1100 Ω R_L = 0
DN_{DAC}	Differential Nonlinearity (all D/A converters)	44, 46, 48, 50, 52, 54	–	±0.3	–	LSB	
IN_{DAC}	Integral Nonlinearity (all D/A converters)		–	±0.5	–	LSB	
THD_{DAC}	Total Harmonic Distortion (all D/A converters)		–	50	–	dB	Signal 1MHz Bandwidth 6 MHz
MISCELLANEOUS							
V_{MCLKD}	Clock Output DC Voltage	7	–	2.5	–	V	C_L = 50 pF
V_{MCLCA}	Clock Output Voltage Swing		1.0	1.2	1.4	V_{PP}	C_L = 50 pF
t_{MCLKR}	Clock Rise Time		–	9	–	ns	C_L = 50 pF
t_{MCLKF}	Clock Fall Time		–	11	–	ns	C_L = 50 pF
R_{MCLK}	Clock Output Impedance		–	30	–	Ω	AC Coupling
V_{LCIT}	Digital Luma/Chroma Input Threshold Voltage	8 to 19, 22 to 25	–	1.1	–	V	
$-I_{LCIL}$	Digital Luma/Chroma Input Low Current		1.4	2.0	3.0	mA	V_{IL} = 0.4 V
C_{LCI}	Digital Luma/Chroma Input Capacitance		–	5	–	pF	
V_{OSDT}	OSD Input Threshold Voltage	34 to 37	–	0.4	–	V	
I_{OSDL}	OSD Input Leakage Current		–	–	±1	µA	
C_{OSD}	OSD Input Capacitance		–	5	–	pF	
V_{RESQT}	$\overline{\text{Reset}}$ Input Threshold Voltage	26	–	2.2	–	V	Rising Edge
$-I_{RESQL}$	$\overline{\text{Reset}}$ Input Low Current		–	1.2	–	V	Falling Edge
I_{RESQH}	$\overline{\text{Reset}}$ Input High Current		–	0	–	µA	
C_{RESQ}	$\overline{\text{Reset}}$ Input Capacitance		–	5	–	pF	

Characteristics, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{BOL}	Digital Baseband Output Low Voltage	1 to 3, 64 to 68	–	–	2.2	V	
V_{BOH}	Digital Baseband Output High Voltage		2.8	–	–	V	
t_{BOD}	Digital Baseband Output Delay Time		–	–	16.5	ns	$C_L = 50$ pF
$-I_{IICIL}$	I²C-Bus Input Leakage Current	62, 63	–	–	±1	µA	
C_{IICI}	I²C-Bus Input Capacitance		–	5	–	pF	
V_{IICOL}	I²C-Bus Output Low Voltage	62	–	–	0.4	V	$I_{LOW} = 3.0$ mA



Note: all digital luma and chroma inputs use ts1 and thi1;
ts2 and thi2 are used for PLL clock/ data, Csync and Msync/Mdata both edges are used for the double Clock OSD Input

Fig. 3–12: Data input & outputs timing chart and symbols

4. Programming

4.1. I²C-Bus Interface

The I²C-bus interface is used to program all parameters to the DMI 3110 A. Data can only be written to the DMI 3110 A. The I²C-bus interface uses a chip address, a register (sub-) address and an 8-bit data word that is written to the addressed register. The bus protocol is shown in the figure below. The main address is $0E.

The register assignment for the I²C-bus registers is given in the following table. The DMI 3110 A evaluation software allows the access of all subregisters via the indicated mnemonics.

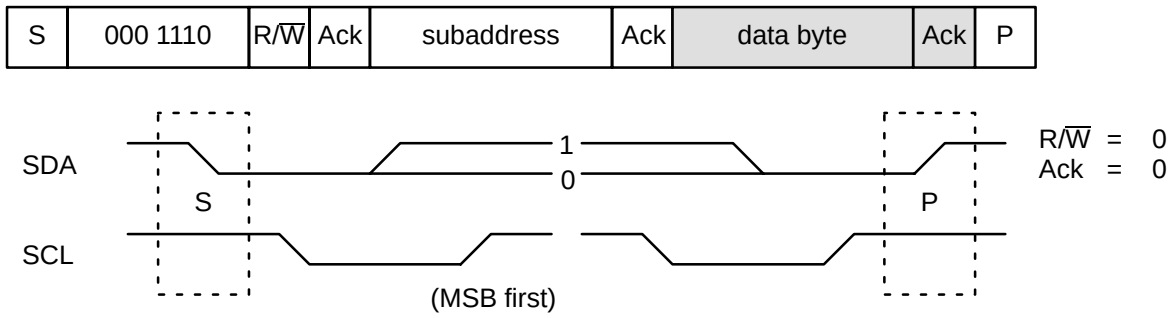


Fig. 4–1: I²C-bus protocol

Table 4–1: I²C-Bus Registers

I²C subad-dress	I²C data[7:0]		Name	Default
0		not used	–	0
1	d[7:0]	Timing Generator disable time	TGDIS	250
2	d[7] d[6] d[5:0]	reserved Low Pass Filter On Luma Gain Adjustment	– YLPF YGAIN	0 0 24
3	d[4:0]	Chroma Gain Adjustment	CGAIN	22
4	d[7:0]	PAL Color Burst Amplitude	BURST	–40
5	d[7] d[6] d[5:2] d[1] d[0]	reserved Chroma Demultiplexer Phase (PAL) Chroma Peaking Filter Chroma Lowpass Filter (F2) Chroma Lowpass Filter (F1)	– PALMUX CLPPK CLPF2 CLPF1	0 0 8 1 1
6	d[7] d[6:0]	reserved B-Y Gain	– UGAIN	0 63
7	d[7] d[6:0]	reserved R-Y Gain	– VGAIN	0 90
8	d[7:0]	Luminance Blanking Start	YBLANKS	2
9	d[7:0]	Luminance Blanking End	YBLANKE	100
10	d[7:0]	Key Pulse Start	KEYS	73
11	d[7:0]	Key Pulse End	KEYE	97
12	d[7:4] d[3:0]	Vertical blanking length reserved	VBLEN –	10 0
13	d[7:6] d[5:0]	reserved Luminance Delay	– YDEL	0 42
14	d[7:4] d[3:0]	reserved Composite Sync Delay	– CSDEL	0 4
15	d[7] d[6:4] d[3] d[2] d[1:0]	reserved Testbits special sync mode OSD-Insertion Into PAL Enable Testbits	 PALOSD 	0 0 0 0 0
16	 d[7:6] d[5] d[4:2] d[1] d[0]	TESTREGISTER Testbits TTX-Insertion Disable Testbits Sync Pulse Output Disable reserved		 0 0 0 0 0
17	d[7:0]	Chroma Blanking Start	CBLANKS	13
18	d[7:0]	Vertical Sync Trigger Point	VSTRIG	50
19	d[7:0]	Chroma Blanking End	CBLANKE	111

I²C-Bus Registers, continued

I²C subaddress	I²C data[7:0]		Name	Default
20	d[7:0]	Horizontal Sync Start	HSYNCS	0
21	d[7:0]	Horizontal Sync End	HSYNCE	1
22		TESTREGISTER	–	
	d[7:6]	Testbits		0
	d[5]	B-Y Disable		0
	d[4]	R-Y Disable		0
	d[3:0]	Testbits		0
23	d[7:0]	TTX–Insertion Start	TTXS	116
24–25		reserved	–	
26	d[7]	reserved		0
	d[6]	Chroma demultiplexer phase (RGB)	RGBMUX	0
	d[5]	OSD-Insertion Into RGB(YUV) Enable	RGBOSD	0
	d[4]	Luma Offset Subtracter Control	YOFFSET	0
	d[3]	Interpolation Filter Bypass	RGBFBP	0
	d[2]	RGB-Matrix Bypass	RGBMBP	0
	d[1:0]	Testbits		0
27	d[7:4]	reserved		0
	d[3:0]	RG–B (YUV)-Delay	RGBDEL	12
28		not used	–	
29		TESTREGISTER	–	
	d[7:0]	Testbits		0
30	d[6:0]	TTX-Window 2 End (line = 256 + x)	TTXW2E	79
31	d[7]	Testbit		0
	d[6:0]	TTX-Window 2 Start (line = 256 + x)	TTXW2S	62
32	d[6:0]	TTX-Window 1 End	TTXW1E	23
33	d[7]	Start Sample TTX Read 230/231 (1/0)	TTXSS	0
	d[6:0]	TTX-Window 1 Start	TTXW1S	6
34	d[7:6]	reserved		0
	d[5]	Gray Code off	GRAYOFF	0
	d[4]	Input Select	MACIN	1
	d[3:2]	Testbits		0
	d[1]	Clamping Enable	CLAMPEN	1
	d[0]	reserved		0
35		TESTREGISTER	–	
	d[7]	ADC-Standby Control		0
	d[6]	Gray Code Test Control		0
	d[5:0]	Testbits		0
36	d[5:0]	Automatic Gain Control	AGC	25
37 to 47		not used	–	
48 to 63	d[7:0]	OSD Color Look-Up Table	OSDX	

Table 4–2: Related DMA 2281 IM-Bus Registers

IM-Bus address	IM-Bus data[15:0]		Name	Default
23	d[15:10]	saturation U	SAU	32
23	d[7:2]	saturation V	SAV	32
200	d[15:10]	luma contrast	CT	63
200	d[8]	luma contrast switch	CTS	1
202	d[15:9]	composite sync delay	SD	70

4.2. General Remarks

For an easy adjustment of the DMI 3110 A, the MUBI software can be used. The parameter names mentioned below refer to the MUBI software and are in the same order. The register subaddress is always given in parenthesis.

4.2.1. Initialization

Command name: INIT or [F10]
This is a command in the MUBI program. It initializes the DMI 3110 A with the parameters set to the most recent values. Before this command, a hardware reset (power-on reset) should be done.

4.3. Analog Input

4.3.1. Input Select (34)

Command name: MACIN
This command switches between the analog MAC inputs 1 and 2. MACIN = 1 means the MAC input 1 is selected.

MACIN	0: Input 2 (pin 60) 1: Input 1 (pin 58)

4.3.2. Clamping Enable (34)

Command name: CLAMPEN
This command enables the clamping at the analog MAC inputs. CLAMPEN = 1 means that the clamping is enabled.

CLAMPEN	0: Clamping disabled 1: Clamping enabled

4.3.3. Automatic Gain Control (36)

Command name: AGC
The AGC value controls the gain of the input amplifier. In normal operation the CCU reads the amplitude value out of the DMA and adjusts the AGC value in the DMI for a proper signal amplitude at the A/D converter. The range of ±6 dB is divided into 64 steps.

AGC	Value = Gain[dB] / 0.19 dB range 0 to 63

4.3.4. Baseband Output Code (34)

Command name: GRAY
The digital baseband output code of the DMI 3110 A can be switched over between straight binary code and gray code.

GRAYOFF	1: binary code 0: gray code

4.4. Chrominance Channel

4.4.1. Chroma Demultiplexer Phase (5, 26)

PALMUX RGBMUX	0: normal 1: inverted

4.4.2. Chroma Lowpass (5)

Command names: CLPF1, CLPF2, CLPPK
This filter consists of 1 fixed part and 3 adjustable parts in series. Parts 1 to 3 are lowpass filters, part 4 is an adjustable peaking filter.

The transfer functions are:

Table 4–3: Transfer Functions

Part 1	Fixed	$H(z) = 0.5 \cdot (1 + Z^{-4}) \cdot (1 + Z^{-2})^2$
Part 2	$F1 = 0$	$H(z) = 0.5 \cdot (1 + Z^{-4})$
CLPF1	$F1 = 1$	$H(z) = Z^{-4}$
Part 3	$F2 = 0$	$H(z) = 0.5 \cdot (1 + Z^{-6})$
CLPF2	$F2 = 1$	$H(z) = Z^{-6}$
Part 4	$PK = 1$	$H(z) = Z^{-6} - 4/16 \cdot (1 + z^{-12})$
CLPPK	$PK = 2$	$H(z) = Z^{-6} - 3/16 \cdot (1 + z^{-12})$
	$PK = 4$	$H(z) = Z^{-6} - 2/16 \cdot (1 + z^{-12})$
	$PK = 8$	$H(z) = Z^{-6} - 1/16 \cdot (1 + z^{-12})$

4.4.3. Color Component Gain (6,7)

Command names: UGAIN, VGAIN
This is the gain adjustment for the color component signals in front of the 4:4:4 interpolation filter (after the lowpass filter). The B–Y signal is multiplied with the UGAIN value to result in the U component signal. The R–Y signal is multiplied with the VGAIN value to result in the V component signal. The gain should be adjusted as high as possible (short before signal limitation) for a low quantization noise.

UGAIN	Value = $128 \cdot gain$	range 0 to 127
VGAIN	Value = $128 \cdot gain$	range 0 to 127

4.4.4. Color Burst (4)

Command name: BURST
This is the value of the burst amplitude. The adjustment is relative to a maximum chroma amplitude of 1. This value's sign has to be negative. The positive sign can be used for test purposes. The formula for the calculation is:

Value =	$-91 \cdot$ Burst amplitude
range	-128 to $+127$

4.4.5. Color Carrier Gain (3)

Command name: CGAIN

The gain for the color subcarrier can be adjusted in front of the D/A converter (after the PAL modulator). This adjustment influences the color carrier inclusive the burst. The formulae for the calculation of these values are:

CGAIN	Value = $32 \cdot gain$	range 0 to 31

4.5. Luminance Channel

4.5.1. Luminance Offset (26)

Command name: YOFFSET
A luminance offset can be added at the luminance input. The offset will be added in the RGB as well as the PAL coder path.

YOFFSET	$0 \rightarrow$ Offset $= -16$
	$1 \rightarrow$ Offset $= 0$

4.5.2. Luminance Lowpass Filter (2)

Command name: YLPF
In the luma path of the encoder a switchable low-pass filter with a transfer function $1+z^{-1}$ can be selected.

YLPF	0: bypass 1: lowpass $0.5 \cdot (1 + z^{-1})$

4.5.3. Luminance Gain (2)

Command name: YGAIN
The luminance gain for the luminance signal at the composite video output can be adjusted after the chroma trap. The formula for the calculation of this value is:

YGAIN	Value = $64 \cdot gain$	range 0 to 63

4.6. Timing

4.6.1. Horizontal Pulses (1, 8 to 11, 17, 19)

Command names: TGDIS, KEYS, –E, YBLANKS, –E, CBLANKS, –E
All these pulses are started with the low transition of the hsync in the composite sync signal. The end of the timing generator (TGDIS) stops the pulse generation. It must therefore have the highest value of all. While the timing generator is running, the trigger input is disabled. This is necessary to prevent the timing generator from triggering at the H/2 pulses (equalization pulses) in the vertical sync signal. All pulses, except timing generator are adjustable within a step width of two clock periods, and have a range of 2 to 510 clock periods. The timing generator has a range of 4 to 1020 clock periods.

TGDIS	Value = $t_{delay} \cdot f_{clock} / 4$	range 1 to 255
KEY	Value = $t_{delay} \cdot f_{clock} / 2$	range 1 to 255
YBLANK	Value = $t_{delay} \cdot f_{clock} / 2$	range 1 to 255
CBLANK	Value = $t_{delay} \cdot f_{clock} / 2$	range 1 to 255

4.6.2. Short Vertical Sync (15, 20, 21)

Command names: SSYNC, HSYNCS, –E
It is possible to replace the vertical sync signal with a special short vertical sync signal with a duration of one horizontal line. The position of this sync pulse is one line before the original vertical sync pulse would appear. This mode can be selected with the SSYNC command. In this mode the composite sync signal is switched off and the short vertical sync pulse is used. The horizontal sync pulses are generated from the timing generator. Therefore the start and end values for the hsync have to be adjusted.

SSYNC	0: composite sync 1: short vertical sync	
HSYNC	Value = $t_{delay} \cdot f_{clock} / 2$	range 1 to 255

4.6.3. Vertical Pulses (12, 18)

Command names: VSTRIG, VBLEN
The detection level for the vertical sync separator can be adjusted to start the generated vertical blanking at the start of the equalization pulses or at the start of vertical sync pulses. A counter which runs with fc/8 starts at each rising edge of the composite sync signal. At the falling edge the counted number is compared with the detection level VSTRIG. If the counted number is smaller than the detection level a vertical blanking pulse will be generated.

The duration of the vertical blanking pulse (VBLEN) can be adjusted between 0 and 15.

VSTRIG	Value = $f_c \cdot t_{high} / 8$	range 0 to 255
VBLEN	Value = n_H	range 0 to 15

Example for VSTRIG:
fc = 20.25 MHz
High time at normal line = 59.3 µs · 20.25 MHz / 8 = 150
High time at equal. pulses = 29.7 µs · 20.25 MHz / 8 = 75
High time at vsync pulses = 4.7 µs · 20.25 MHz / 8 = 12
For a start of the vertical blanking at the equalization pulses the detection level has to be between 75 and 150.

For a start of the vertical blanking at the vsync pulses the detection level has to be between 12 and 75.

4.6.4. Delay for CSYNC, Luminance and RGB (13, 14, 27)

Command names: CSDEL, YDEL, RGBDEL
The delays for the composite sync, the luminance signal and the RGB signals can be adjusted separately. The luminance delay has to be adjusted for matching with the chroma signal. The RGB delay has to be adjusted for matching with the composite video signal.

CSDEL	Value = (see *)	range 0 to 15*
YDEL	Value = $t_{delay} \cdot f_{clock}$	range 0 to 63
RGBDEL	Value = $t_{delay} \cdot f_{clock}$	range 0 to 15

* the delay is added to the luma delay and the weighting of the bits is not binary weighting: bit 0 = 1, bit 1 = 1, bit 2 = 1, bit 3 = 2 (maximum delay = 5 clock periods).

4.7. Teletext Transcoder (23, 30 to 33)

Command names: TTXS, TTXSS, TTXW1S, _E, TTXW2S, _E
The teletext transcoder allows to select lines from the D2MAC/DMAC signal for the transcoding function. Two blocks of lines can be selected, for each block the first and the last line number must be programmed. If the last line number is smaller than the first line number the transcoding is inactive. The exact time for the insertion of the teletext signal into the luminance and composite signals can be programmed with the value of TTXS.tf.
For DMAC TTX transcoding, one of the two bit streams can be selected by selecting the start sample point for the TTX transcoder.

TTXS	Value = $t_{delay} \cdot f_{clock}$	range 0 to 255
TTXSS	sample at 230 / 231	range 0/1
TTXW1	Value = n_H	range 0 to 63
TTXW2	Value = 256 + n_H	range 0 to 63

4.8. On-Screen Display (48 to 63)

Command names: PALOSD, RGBOSD, OSDY0...7, OSDU0...7, OSDV0...7
The OSD insertion function can be activated separately for the composite video and SVHS signal (encoder) and the RGB path.
The on-screen display colors are programmed by a color look up table. For each color (0 to 7) of a binary RGB signal a 16-bit entry in the color look up table allows to program luminance with 6-bit resolution and chrominance (U/V) with 5-bit resolution respectively.

PALOSD	0: OSD disabled into PAL 1: OSD enabled into PAL	
RGBOSD	0: OSD disabled into RGB 1: OSD enabled into RGB	
CLUT[7:0]	address: data:	RGB color number 2 byte
	d0[7:2] d0[1:0], d1[7:5] d1[4:0]	luma chroma (U) chroma (V)

4.9. RGB Processing

The component processing path makes it possible to bypass the 4:2:2 to 4:4:4 interpolation filter and also to bypass the YUV to RGB matrix. When the matrix is bypassed, the BLUE/RED outputs which carry the U/V data are switched to signed binary format. The U/V multiplex is resynchronized on every line with the MAC sync signal; the multiplex order is adjustable. The on-screen display can be enabled to the RGB path. The RBG processing path has an adjustable delay to match the timing of composite/component signals.

RGBFBP	1 : bypass
RGBMBP	1 : bypass
RGBMUX	1: U/V multiplex inverted

5. Data Sheet History

1. Data sheet: “DMI 3110 A Digital MAC Interface”, July 1, 1996, 6251-381-1DS. First release of the data sheet.

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