RC288ACi/VFC, RC240ACi/VFC and RC192ACi/VFC Integrated V.Fast Class™ (V.FC™) Data and Fax Modem Device Set Family

INTRODUCTION

The Rockwell V.Fast Class™ (V.FC™) integrated modem device set family supports ultra high speed data and high speed fax operation. Models are provided that meet different requirements for data throughput and options (Table 1). Each model consists of modem data pump and controller devices and supporting firmware.

As a data modem, the modem operates at line speeds to 28800 bps (RC288ACi/VFC), 24000 bps (RC240ACi/VFC), or 19200 bps (RC192ACi/VFC). Error correction (V.42/MNP 2–4) and data compression (V.42 bis/MNP 5) maximize data transfer integrity and boost data throughput up to 115.2 kbps, 96 kbps, or 76.8 kbps. The modem also operates in non-error-correcting mode.

As a fax modem, the modem supports Group 3 send and receive rates up to 14400 bps and supports T.30 protocol.

Extended "AT" commands provide data, fax class 1 and class 2, MNP 10, and world-class functions while using minimal external ROM, RAM, and optional NVRAM. Models supporting US/Canada and multiple countries with different memory requirements are available (Table 1).

The modem operates over a dial-up telephone line, can auto-dial and auto-answer, and can operate in both synchronous and asynchronous modes. Configuration information can be stored in non-volatile memory.

Two system architectures are supported: a low cost configuration using a single microcontroller and a high performance configuration employing an added co-processor.

A PC-based "ConfigurACE™" utility program can be used to customize the MCU firmware to specific application and country requirements.

With its small size, this modem device set is ideal for desktop applications.

Accelerator kits are available to minimize application design time and costs.

FEATURES

- Data modem throughput up to 115.2 kbps
  - —V.Fast Class (V.FC), V.32 bis, V.32, V.22 bis, V.22A/B, V.23, and V.21; Bell 212A and 103
  - —V.42 LAPM and MNP 2-4 error correction
  - —V.42 bis and MNP 5 data compression
- MNP 10 data throughput enhancement (to V.32 bis)
- Fax modem send and receive rates up to 14400 bps
  - —V.17, V.29, V.27 ter, and V.21 channel 2
- World-class operation (option)
  - —V.25 bis commands (asynchronous only)
  - —Call progress and blacklisting parameters
  - —Multiple country support
- Hayes AutoSync (option)
- ConfigurACE utility program
- Communication software compatible command sets
  - —AT, fax class 1, and fax class 2 commands
  - —S registers
- Built-in DTE interfaces
  - —DTE speed up to 115.2 kbps
  - —Parallel 16550A UART-compatible interface
  - —Serial CCITT V.24 (EIA/TIA-232-E)
- Line quality monitoring and auto retrain
- NVRAM directory and stored profiles
- Flow control and speed buffering
- Automatic format/speed sensing
- Serial synchronous and asynchronous data
- Parallel asynchronous data
- Auto dial and auto answer
- Tone, pulse, and adaptive dialing
- Calling Number Delivery (Caller ID) detect
- Diagnostics
- Extended operating temperature models available
- +5V operation
- Typical power consumption:

Mode	Low Cost (Without CEP)	High Performance (With CEP)
Operating	1.07 W	1.22 W
Sleep	21 mW	32 mW
Stop	11 mW	12 mW

- CMOS VLSI devices
  - —MCU: 84-pin PLCC
  - —CEP: 84-pin PLCC
  - —MDP: 68-pin PLCC

Data Sheet
(Preliminary)

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Table 1. Modem Models, Functions, and Memory Requirements

Model[1]	Supported Functions[2]					Memory (Bytes)		
	Fax	MNP10	W-Class	AutoSync	Country	ROM	RAM[3]	NVRAM
RC288ACi-D/VFC	–	–	–	–	US/Can	64k	32k/40k	256
RC288ACi/VFC	S	–	–	–	US/Can	64k	32k/40k	256
RC288ACi(/A)/VFC	S	S	–	A	US/Can	128k	32k/40k	256
RC288ACiW-D/VFC	–	S	S	S	Multiple	128k	32k/40k	256
RC288ACiW(E)/VFC	S	S	S	S	Multiple	128k	32k/40k	256
RC240ACi-D/VFC	–	–	–	–	US/Can	64k	32k/40k	256
RC240ACi/VFC	S	–	–	–	US/Can	64k	32k/40k	256
RC240ACi(/A)/VFC	S	S	–	A	US/Can	128k	32k/40k	256
RC240ACiW-D/VFC	–	S	S	S	Multiple	128k	32k/40k	256
RC240ACiW(E)/VFC	S	S	S	S	Multiple	128k	32k/40k	256
RC192ACi-D/VFC	–	–	–	–	US/Can	64k	32k/40k	256
RC192ACi/VFC	S	–	–	–	US/Can	64k	32k/40k	256
RC192ACi(/A)/VFC	S	S	–	A	US/Can	128k	32k/40k	256
RC192ACiW-D/VFC	–	S	S	S	Multiple	128k	32k/40k	256
RC192ACiW/VFC	S	S	S	S	Multiple	128k	32k/40k	256

Notes:

1. Option notations:
   - -D Data only (no fax).
   - W World class support.
   - (/A) Optional AutoSync support.
   - (E) Optional industrial temperature range.
2. Supported functions (A = Optionally supported; S = Supported; – = Not supported):
   - Fax Fax class 1 and class 2 command functions.
   - MNP 10 Data throughput enhancement functions.
   - W-Class World class functions supporting multiple country requirements.
   - AutoSync Hayes AutoSync available with 128k-byte ROM installed.
3. Configuration dependent:
   32k bytes in low cost configuration;
   40k bytes in high performance configuration (8k bytes on the MCU external bus, 32k bytes on the CEP external bus).

TECHNICAL OVERVIEW

GENERAL DESCRIPTION

The modem device set provides the processing core of the modem. The OEM adds external memory, crystal, discrete components, and a digital access arrangement (DAA) circuit to complete the modem system.

System Configurations

High Performance. The modem device set consists of a L39 Microcontroller (MCU), a Modem Data Pump (MDP), and a Compression Expansion Processor (CEP). This configuration provides maximum bidirectional data throughput.

In this configuration, the OEM provides external memory for the MCU (64k/128k bytes ROM and 8k bytes RAM) and for the CEP (8k bytes ROM [initial code release only] and 32k bytes RAM).

Low Cost. The modem device set consists of a L39 MCU and a MDP.

In this configuration, the OEM provides external memory only for the MCU (64k/128k bytes ROM and 32k bytes RAM).

Modem Data Pump (MDP)

The MDP is a Rockwell RC288DPi/VFC, RC240DPi/VFC, or RC192DPi/VFC 2-wire data/fax modem data pump packaged in a 68-pin PLCC.

As a data modem, the MDP can operate in full-duplex, synchronous/asynchronous modes at line rates up to 28800 bps. Using a proprietary scheme to optimize modem configuration for line conditions, the MDP can connect at the highest data rate that the channel can support from 28800 bps (RC288DPi/VFC), 24000 bps (RC240DPi/VFC), or 19200 bps (RC192ACi/VFC) to 14400 bps with automatic fallback. Automode operation in V.32 bis is provided in accordance with EIA/TIA-PN2330.

As a fax modem, the MDP fully supports Group 3 facsimile send and receive speeds of 14400, 12000, 9600, 7200, 4800, and 2400 bps.

Microcontroller (MCU)

The MCU is a Rockwell L39 microcomputer packaged in a 84-pin PLCC. The MCU performs the command processing and host interface functions.

The MCU connects to the host via a V.24 (EIA/TIA-232-E) serial interface or a parallel microcomputer bus. The MCU connects to the MDP via dedicated lines and the external bus. The MCU external bus also connects to OEM-supplied ROM and RAM and, high performance configuration, to the CEP. The MCU external bus also connects to OEM-supplied ROM (64k bytes for US/Canada models or to a 128k bytes for models supporting MNP 10, W-class, or AutoSync functions) and to RAM (32k bytes for the low cost configuration or 8k bytes for the high performance configuration).

For W-class models, buffered switch inputs and latched indicator/control outputs can optionally be connected to the MCU external bus.

For all models, 256 bytes NVRAM can optionally be connected to the MCU over a dedicated serial interface.

Low Cost Configuration. The MCU connects to the MDP and to external memory over the MCU external bus. The MCU crystal frequency is 14.7456 MHz. The MCU external memory is 64k or 128k bytes ROM (45 ns) and 32k bytes RAM (45 ns).

High Performance Configuration. The MCU connects to the MDP, external memory, and to the CEP over the MCU external bus. The use of CEP in this configuration allows the MCU to operate slower which also permits the use of slower memory connected to the MCU bus. The MCU crystal frequency is 12.9024 MHz. The MCU external memory is 64k or 128k bytes ROM (55 ns) and 8k bytes RAM (55 ns).

Compression Expansion Processor (CEP)

The CEP performs the dedicated data compression and expansion functions in V.42 bis/MNP 5 modes to provide maximum bidirectional throughput for high performance operation. The CEP is packaged in a 84-pin PLCC.

The CEP host interface connects to the MCU external bus and the CEP external memory bus connects to 32k bytes RAM (55 ns) and 8k bytes ROM (55 ns). The external ROM for the CEP is required only for initial CEP code release. The CEP crystal frequency is 12.9024 MHz.

MCU Firmware

MCU firmware performs processing of general modem control, command sets, error correction, MNP 10, fax class 1 and class 2, and DTE interface functions. The MCU firmware is provided by Rockwell in object code form for the OEM to program into external ROM. The MCU firmware may also be provided in source code form under a source code addendum license agreement.

CEP Firmware

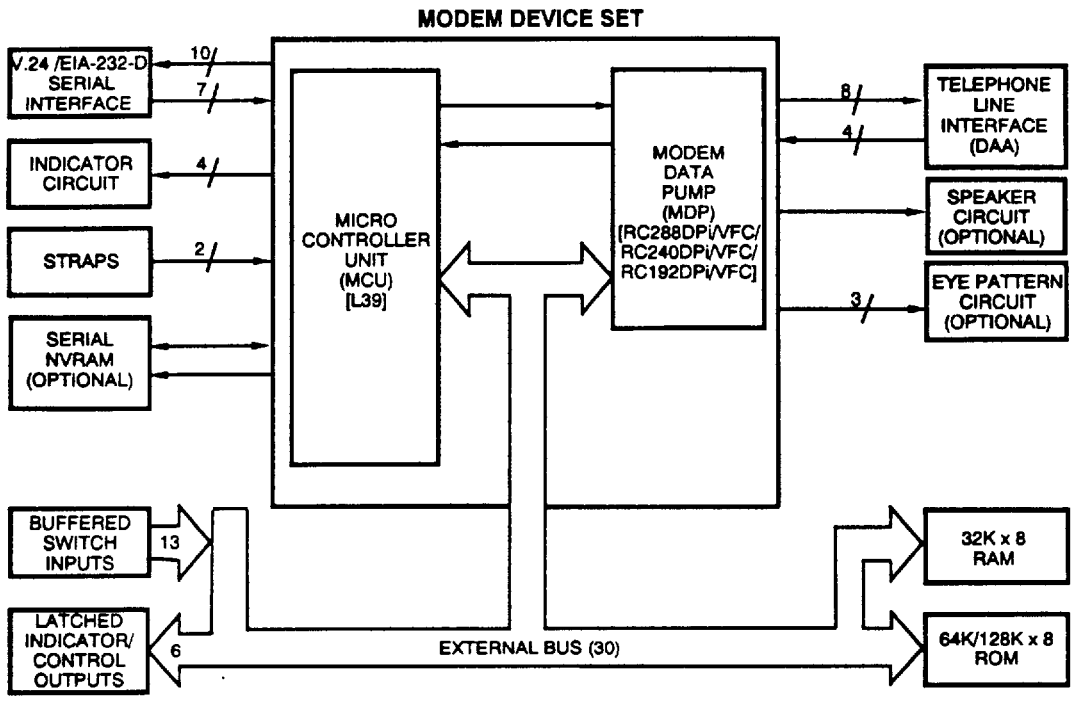
CEP firmware is provided by Rockwell in object code form for the OEM to program into an external 8k-byte ROM for initial CEP product. Later CEP products may incorporate the firmware internally thus eliminating the requirement for the external 8k-byte ROM.

SUPPORTED INTERFACES

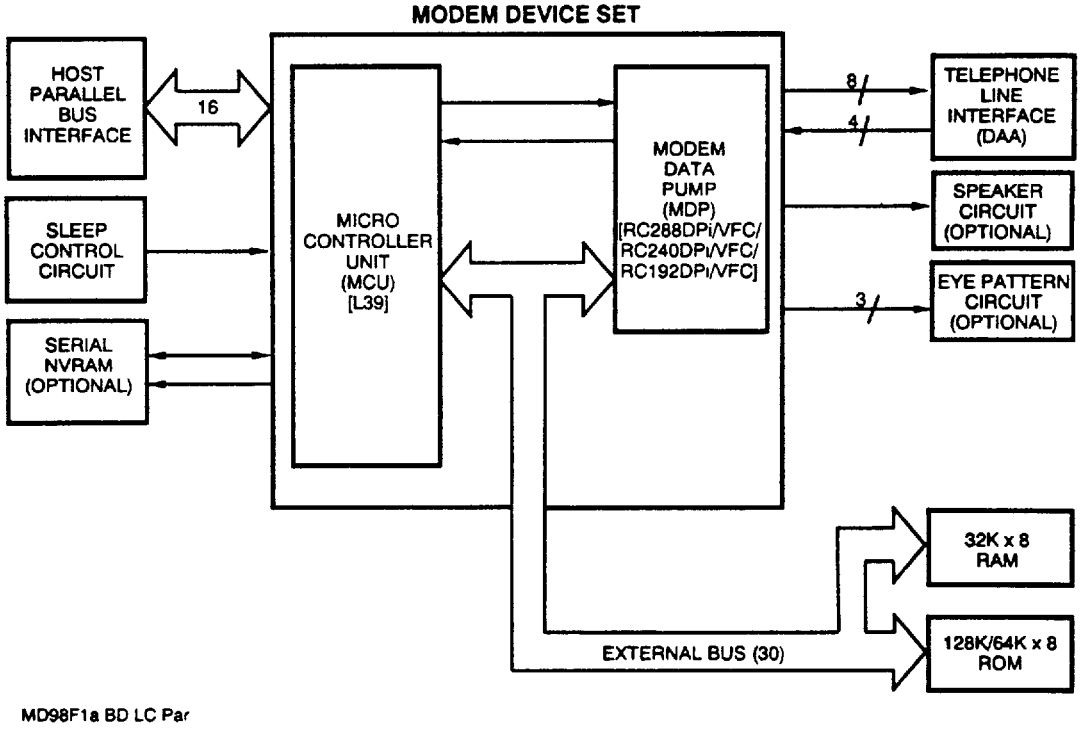
The major hardware signal interfaces of the modem device set are illustrated in Figure 1.

Parallel Host Bus Interface

A 16550A UART-compatible parallel interface is provided. Eight data lines, three address lines, and nine control lines are supported.

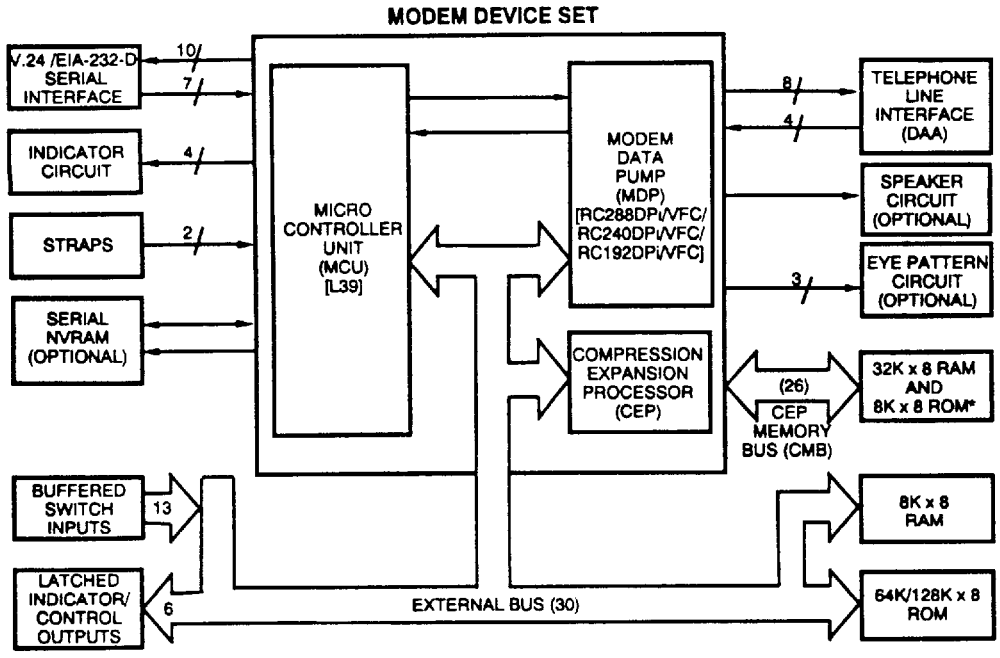


a. Serial Interface Selected

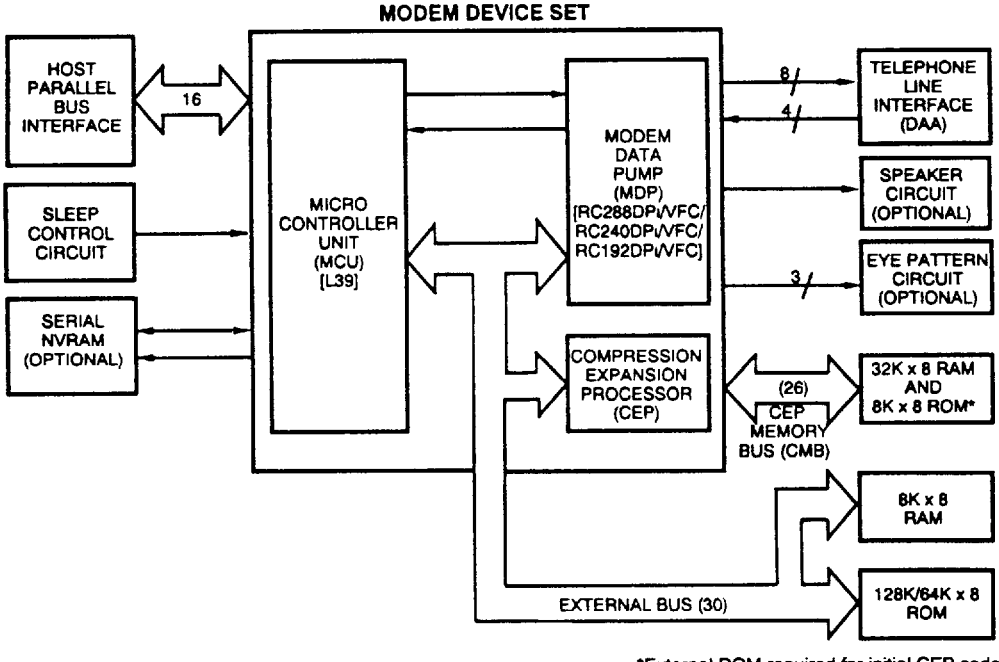


a. Parallel Interface Selected

Figure 1a. Modem General Interface-Low Cost



a. Serial Interface Selected



a. Parallel Interface Selected

Figure 1b. Modem General Interface-High Performance

Serial/Switch/Indicator Interface

A DTE serial interface, direct connect and bit mapped switch inputs, and indicator/control outputs are supported.

Serial Interface. A 16-line V.24 and EIA/TIA-232-E logic-compatible serial interface to the DTE is supported. A clock stop output signal is provided which can be used to turn off transmitter and receiver clocks to the DTE in asynchronous modes.

Switch Interface. A direct connect strap input can be sampled. Thirteen switch inputs, bit-mapped through an external three-state buffer, can be sampled in the world-class (W-class) configuration.

Indicator Interface. Four direct connect indicator outputs are supported. Six indicator outputs, bit-mapped through an external latch, are supported in W-class configurations.

Stop Mode Control

The $\overline{\text{STPMODE}}$ input is supported which controls modem entry into Stop Mode.

NVRAM Interface

A serial interface to the optional OEM-supplied 256-byte non-volatile RAM (NVRAM) is provided. Data stored in NVRAM can take precedence over the factory default settings. The 256-byte NVRAM can store up to two user-selectable configurations and can store up to four 45-digit dial strings.

Speaker Interface

A speaker output, controlled by AT or V.25 bis commands, is provided for an optional OEM-supplied speaker circuit.

MCU External Bus Interface

The MCU external bus connects to the MDP, ROM, RAM, and, for W-class configuration, a switch input buffer and indicator output latches. In the high performance configuration, MCU also connects to the CEP. The non-multiplexed bus supports eight bidirectional data lines and 17 address lines. Dedicated MDP, ROM, RAM, and CEP chip select and control outputs, as well as indicator/control device chip select outputs, are also provided.

Line Interface

MDP. The MDP connects to the line interface circuitry via a receive analog input, two transmit analog outputs, a relay driver output, and a ring signal input. The relay output may be used to drive the Caller ID relay.

MCU. The MCU provides four relay control outputs to the line interface. These outputs may be used to control relays such as off-hook, pulse, mute, A/A1, earth, and talk/data. The MCU accepts ring signal and line current sense from the line interface.

Eye Pattern Generator Interface

Eye pattern data, clock, and sync interface signals are provided to allow an external eye pattern generator circuit to be easily added in order to observe modem performance relative to line impairments.

COMMANDS

The modem supports data modem, fax class 1 and 2, MNP 10, and W-class commands and S Registers (see Tables 2 and 3, respectively) depending on the modem model.

Data Modem Operation. Data modem functions operate in response to the basic AT commands when +FCLASS=0. Default parameters support US/Canada operation.

MNP 10 Operation (Option). MNP 10 functions operate in response to MNP 10 commands.

AutoSync Operation (Option). AutoSync operates in response to the &Q4 command.

World Class (W-Class) Operation. W-class functions operate in response to W-class AT and V.25 bis commands.

Fax Modem Operation (Option). Facsimile functions operate in response to fax class 1 commands when +FCLASS=1 or to fax class 2 commands when +FCLASS=2.

DATA MODEM OPERATION

Automatic Speed/Format Sensing (Serial Interface)

The modem can automatically determine the speed and format of the data sent from the DTE (serial interface only). The modem can sense speeds of 300, 600, 1200, 2400, 4800, 7200, 9600, 12000, 14400, 16800, 19200, 21600, 24000, 26400, 28800, 38400, 57600, and 115200 bps and the following data formats:

Parity	Data Length (No. of Bits)	No. of Stop Bits	Character Length (No. of Bits)
None	7	2	10
Odd	7	1	10
Even	7	1	10
None	8	1	10
Odd	8	1	11 *
Even	8	1	11 *

* 11-bit characters are sensed, but the parity bits are stripped off during data transmission in Normal and Error Correction modes. Direct mode does not strip off the parity bits.

The modem can speed sense data with mark or space parity and configures itself as follows:

DTE Configuration	Modem Configuration
7 mark	7 none
7 space	8 none
8 mark	8 none
8 space	8 even

ESTABLISHING DATA MODEM CONNECTIONS

Note: Default parameter values support modem operation in the U.S. For modem use in a different country, parameter values can be changed using ConfigureACE.

Telephone Number Directory

The modem supports four telephone number entries in a directory that can be saved in a serial NVRAM. Each telephone number can be up to 45 characters in length. A telephone number can be saved using the &Zn=x com-

Table 2. AT Commands

Command	Function
	Basic AT Commands
A/	Re-execute command
A	Answer a call
Bn	Set CCITT or Bell Mode
Cn	Carrier control
Dn	Dial (originate a call)
E	Command echo
Fn	Select line modulation
Hn	Disconnect (hang-up)
In	Identification
Ln	Speaker volume
Mn	Speaker control
Nn	Automode enable
On	Return to on-line data mode
P	Set pulse dial default
Qn	Quiet results codes control
Sn=x	Write to S Register
Sn?	Read S Register
T	Set tone dial default
Vn	Result code form
Wn	Error correction message control
Xn	Extended result codes
Yn	Long space disconnect
Zn	Soft reset and restore profile
&Cn	RLSD (DCD) option
&Dn	DTR option
&F	Restore factory configuration (profile)
&Gn	Select guard tone
&Jn	Telephone jack control
&Kn	Flow control
&Mn	Asynchronous/synchronous mode selection
&Pn	Select pulse dial make/break ratio
&Qn	Asynchronous/synchronous mode selection
&Rn	RTS/CTS option
&Sn	DSR override
&Tn	Test and diagnostic
&V	Display current configuration and stored profiles
&Wn	Store current configuration
&Xn	Select synchronous clock source
&Yn	Designate a default reset profile
&Zn=x	Store phone number
%En	Enable/disable line quality monitor and auto-retrain or fallback/fall forward
%L	Report line signal level
%Q	Report line signal quality
%TTn	PTT testing utilities
\Gn	Modem-to-modem flow control (XON/XOFF)
\Kn	Break control
\Nn	Operating mode
#CID	Caller ID detection and reporting
**	Download to flash memory

Table 2. AT Commands (Cont'd)

Command	Function
	ECC AT Commands
%C	Select data compression
\An	Maximum MNP block size
\Bn	Transmit BREAK to remote
\Ln	MNP block transfer control
	MNP 10 AT Commands
)Mn	Enable cellular power level adjustment
* Hn	Set link negotiation speed
-Kn	MNP extended services
-Qn	Enable fallback to V.22 bis/V.22
@Mn	Select initial transmit level
:E	Compromise equalizer enable
	Fax Class 1 AT+F Commands
+FCLASS=n	Service class
+FTS=n	Stop transmission and wait
+FRS=n	Receive silence
+FTM=n	Transmit data
+FRM=n	Receive data
+FTH=n	Transmit data with HDLC framing
+FRH=n	Receive data with HDLC framing
	Fax Class 2 AT+F Commands
+FCLASS=n	Service class
	Class 2 Action Commands
+FCIG	Set the polled station identification
+FDT	Data transmission
+FET=N	Transmit page punctuation
+FDR	Begin or continue Phase C receive data
+FK	Terminate session
+FLPL	Document for polling
+FSPL	Enable polling
	Class 2 DCE Responses
+FCIG:	Report the polled station identification
+FCON	Facsimile connection response
+FDCS:	Report current session
+FDIS:	Report remote capabilities
+FDTC:	Report the polled station capabilities
+FCFR	Indicate confirmation to receive
+FTSI:	Report the transmit station ID
+FCSI:	Report the called station ID
+FPTS:	Page transfer status
+FET:	Post page message response
+FHNG:	Call termination with status
+FPOLL	Indicates polling request
	Class 2 Session Parameters
+FMFR?	Identify manufacturer
+FMDL?	Identify model
+FREV?	Identify revision
+FDCC	DCE capabilities parameters
+FDIS	Current sessions parameters
+FDCS	Current session results
+FLID	Local ID string
+FPTS	Page transfer status
+FCR	Capability to receive
+FAA	Adaptive answer
+FBUF?	Buffer size (read only)
+FPHCTO	Phase C time out
+FAXERR?	Fax error value
+FBOR	Phase C data bit order

Table 2. AT Commands (Cont'd)

Command	Function
	W-Class AT Commands
%Fn	Split-speed direction select
\S	Display active configuration
\W	Split-speed operation
*B	Display blacklisted numbers
*D	Display delayed numbers
*NCnn	Country select
	W-Class V.25 bis Commands
CIC	Connect incoming call
CNL	Execute AT command (if permitted)
CRN	Call request with number
CRS	Call request with memory address
DIC	Disregard incoming call
PRN	Program normal
RLD	Request list of delayed call numbers
RLF	Request list of forbidden call numbers
RLN	Request stored number list (dial strings)

Table 3. S Registers

Register	Function
S0	Rings to auto-answer
S1	Ring counter
S2	Escape character
S3	Carriage return character
S4	Line feed character
S5	Backspace character
S6	Maximum time to wait for dial tone
S7	Wait for carrier
S8	Pause time for dial delay modifier
S9	Carrier detect response time
S10	Carrier loss disconnect time
S11	DTMF Tone Duration
S12	Escape code guard time
S13	Reserved
S14	General bit mapped options
S15	Reserved
S16	Test mode bit mapped options (&T)
S17	Reserved
S18	Test timer
S19-S20	Reserved
S21	V24/general bit mapped options
S22	Speaker/results bit mapped options
S23	General bit mapped options
S24	Sleep inactivity timer
S25	Delay to DTR (CT108) off
S26	RTS-to-CTS (CT105-to-CT106) delay
S27	General bit mapped options
S28	General bit-mapped options
S29	Flash modifier time
S30	Inactivity timer
S31	General bit-mapped options
S32	XON character
S33	XOFF character
S34-S35	Reserved
S37	Line connection speed
S38	Delay before forced hangup
S39	Flow control
S40	General bit-mapped options
S41	General bit-mapped options
S42-S45	Reserved
S91	PSTN transmit attenuation level
S92	Fax transmit attenuation level
S95	Result code messages control
	ECC S Registers
S36	LAPM failure control
S46	Data compression control
S48	V.42 negotiation control
S82	Break handling control
S86	Call failure reason code
	W-Class S Registers
S80	Soft-switch functions
	Cellular Registers
S201	Cellular transmit level

mand and a saved telephone number can be dialed using the DS=n command.

Dialing

DTMF Dialing. DTMF dialing using DTMF tone pairs is supported in accordance with CCITT Q.23. The transmit tone level complies with Bell Publication 47001.

Pulse Dialing. Pulse dialing is supported in accordance with EIA/TIA-496-A.

Adaptive Dialing. If DTMF dialing is selected (T command) and the telephone network will not recognize DTMF tones, the modem will switch to pulse dialing. If pulse dialing is selected (P command), pulse dialing will be used.

Blind Dialing. The modem can blind dial in the absence of a dial tone if enabled by the X0, X1, or X3 command.

Modem Handshaking Protocol

If a tone is not detected within the time specified in the S7 register after the last digit is dialed, the modem aborts the call attempt.

Call Progress Tone Detection

Ringback, equipment busy, and progress tones can be detected in accordance with the applicable standard.

Answer Tone Detection

Answer tone detection can be detected over the frequency range of 2100 ± 40 Hz in CCITT modes and 2225 ± 40 Hz in Bell modes.

Ring Detection

A ring signal can be detected from a TTL-compatible 15.3 Hz to 68 Hz square wave input.

Billing Protection

When the modem goes off-hook to answer an incoming call, both transmission and reception of data are prevented for 2 seconds (data modem) or 4 seconds (fax adaptive answer) to allow transmission of the billing signal.

Connection Speeds

The modem functions as a data modem when the +FCLASS=0 command is active. The possible data connection modes/speeds are listed in Table 4. Two methods of establishing a connection are supported: use of the F command and use of N command, speed sense, and S37 register combination.

Automode

Automode detection can be enabled by the N1 or F0 commands to allow the modem to connect to a remote modem in V.FC mode or in accordance with EIA/TIA-PN2330.

DATA MODE

Data mode exists when a telephone line connection has been established between modems and all handshaking has been completed.

Speed Buffering (Normal Mode)

Speed buffering allows a DTE to send to, and receive data from, a modem at a speed different than the line speed. The modem supports speed buffering at all line speeds.

Flow Control

DTE-to-Modem Flow Control. If the modem-to-line speed is less than the DTE-to-modem speed, the modem supports XOFF/XON or RTS/CTS flow control with the DTE to ensure data integrity.

Mo ,em-to-Modem Flow Control. When enabled by the \G1 command, the modem supports XON/XOFF flow control with the remote modem to ensure data integrity. Modem-to-modem flow control is not used in error correction mode. In this case, flow control is accomplished within the error-correction protocol.

Escape Sequence Detection

The "+++" escape sequence with guard time can be used to return control to the command mode from the data mode. Escape sequence detection is disabled by a S2 Register value greater than 127. Escape sequence detection is disabled in synchronous mode.

BREAK Detection

The modem can detect a BREAK signal from either the DTE or the remote modem. The \Kn command determines the modem response to a received BREAK signal.

Telephone Line Monitoring

GSTN Cleardown (V.FC, V.32 bis, V.32). Upon receiving GSTN Cleardown from the remote modem in a non-error correcting mode, the modem cleanly terminates the call.

Loss of Carrier. If carrier is lost for a time greater than specified by the S10 register, the modem will disconnect.

Receive Space Disconnect. If selected by the Y1 command in non-error-correction mode, the modem will disconnect after receiving 1.6 ± 10% seconds of continuous SPACE.

Table 4. Connection Speed Options

Configuration	Rate
V.FC	28800[1], 26400[1], 24000[2], 21600[2], 19200, 16800, or 14400 bps
V.32 bis	14400, 12000, 9600, 7200, or 4800 bps
V.32	9600 or 4800 bps
V.22 bis	2400 or 1200 bps
V.22	1200 bps
V.23	1200Tx/75Rx or 75Tx/1200Rx
V.21	0-300 bps
Bell 212A	1200 bps
Bell 103	0-300 bps

Notes:
1. RC288ACi/VFC.
2. RC288ACi/VFC and RC240ACi/VFC.

Send SPACE on Disconnect

If selected by the Y1 command in non-error-correction mode, the modem will send 4 ± 10% seconds of continuous SPACE when a locally commanded hang-up is issued by the &Dn or H command.

Fall Forward/Fallback (V.FC, V.32 bis/V.32)

During initial handshake, the modem will fallback to the optimal line connection within V.FC mode if the remote modem is a V.FC modem, or within V.32 bis/V.32 mode if the remote modem is a V.32 bis/V.32 modem, depending upon signal quality if automode is enabled by the N1 command.

When connected in V.FC or V.32 bis/V.32 mode, the modem will fall forward or fallback to the optimal line speed within the connected mode depending upon signal quality if fall forward/fallback is enabled by the %E2 command.

Retrain

The modem may lose synchronization with the received line signal under poor line conditions. If this occurs, retraining may be initiated to attempt recovery depending on the type of connection.

The modem initiates a retrain if line quality becomes unacceptable if enabled by the %E command. The modem continues to retrain until an acceptable connection is achieved or until 30 seconds elapse which will result in telephone line disconnect.

Synchronous Data Mode (Serial Interface Only)

The modem can establish a synchronous connection in accordance with the &Mn or &Qn commands. Upon completing the physical handshake, the modem enters synchronous data mode. The inactivity timer is not used during synchronous data mode.

Direct Mode (Serial Interface Only)

The Direct mode allows data to be transmitted and received directly from the DTE and remote modem. The Direct mode is selected with the &Q0 or \N1 command. In Direct mode, no flow control characters are recognized or transmitted, the modem cannot execute error correction, and the inactivity timer is not used. Speed buffering is disabled in Direct mode.

Programmable Inactivity Timer

The modem will disconnect from the line if data is not sent or received for a specified length of time. In normal or error-correction mode, this inactivity timer is reset when data is received from either the DTE or from the line. This timer can be set to a value between 0 and 2550 seconds by register S30. A value of 0 disables the inactivity timer.

DTE Signal Monitoring

$\overline{\text{DTR}}$. When $\overline{\text{DTR}}$ is asserted, the modem responds in accordance with the &Dn and &Qn commands.

$\overline{\text{RTS}}$. $\overline{\text{RTS}}$ is used for flow control if enabled by the &K command in normal or error-correction mode, or to affect the $\overline{\text{CTS}}$ output if enabled by the &R command in synchronous mode.

$\overline{\text{RDL}}$. When $\overline{\text{RDL}}$ is asserted, the modem requests a remote digital loop if connected in non-error-correction mode (serial interface only).

$\overline{\text{AL}}$. When $\overline{\text{AL}}$ is asserted, the modem disconnects and enters analog loop (serial interface only).

ERROR CORRECTION AND DATA COMPRESSION

V.42 Error Correction

V.42 supports two methods of error correction: LAPM and, as a alternative, MNP 4. The modem provides a detection and negotiation technique for determining and establishing the preferred method of error correction between two modems.

MNP 2-4 Error Correction

MNP 2-4 is a data link protocol that uses error correction algorithms to ensure data integrity. MNP block or stream mode operation may be selected by the \Ln command.

In stream mode, the modem sends data frames in varying lengths depending on the amount of time between characters coming from the DTE.

In block mode, the modem sends data frames of 256 characters in length. Special communication software must be used when using block mode.

V.42 bis Data Compression

V.42 bis data compression mode, enabled by the %Cn or S46 command, operates when a LAPM or MNP 10 connection is established.

The V.42 bis data compression employs a "string learning" algorithm in which a string of characters from the DTE is encoded as a fixed length codeword. Two 2k-byte dictionaries are used to store the strings. These dictionaries are dynamically updated during normal operation.

MNP 5 Data Compression

MNP 5 data compression mode, enabled by the %Cn command, operates during an MNP connection.

In MNP 5, the modem increases its throughput by compressing data into tokens before transmitting it to the remote modem, and by decompressing encoded received data before sending it to the DTE.

MNP 10 DATA THROUGHPUT ENHANCEMENT (TO V.32 BIS)

MNP10 protocol, cellular functionality, and MNP Extended Services enhance performance under adverse channel conditions such as those found in rural, long distance, or cellular environments. An MNP 10 connection is established when either an MNP 2-4 connection is negotiated with a remote modem supporting MNP 10 or MNP 10 extended services is enabled as described below. MNP 10 functions include:

Robust Auto-Reliability. Higher connection success rate is achieved by attempting to overcome channel interference during the modem negotiation phase while maintaining backward compatibility with non-MNP 10 modems.

Negotiated Speed Upshift. Initial connection and MNP handshake is performed at the most dependable speed, then the connection upshifts to the highest supported modem/channel speed. This function is particularly useful in channel conditions with high connection failure rates.

Aggressive Adaptive Packet Assembly. Frame size is dynamically changed to quickly adapt to varying levels of interference.

Dynamic Speed Shifting. Connection speed is shifted upward or downward to optimize data throughput for the channel conditions by continuously monitoring the line quality and link performance.

Dynamic Transmit Level Adjustment. Transmit level is dynamically adjusted to adapt to the varying cellular network environment and to prevent "clipping," which causes data corruption, due to the Preemphasis and Compander effect.

MNP Extended Services. The modem can quickly switch to MNP 10 operation when the remote modem supports MNP 10 and both modems are configured to operate in V.42.

V.42 bis/MNP 5 Support. MNP 10 can operate with V.42 bis or MNP 5 data compression.

FAX CLASS 1 AND CLASS 2 OPERATION

The modem operates as a facsimile (fax) DCE whenever the +FCLASS=1 or +FCLASS=2 command is active. In the fax mode, the on-line behavior of the modem is different from the data (non-fax) mode. After dialing, modem operation is controlled by the fax commands. Some AT commands are still valid but may operate differently from data modem mode.

Calling Tone

Calling tone is generated in accordance with T.30.

WORLD CLASS COUNTRY SUPPORT

The W-class models include functions which support modem operation in multiple countries. The following capabilities are provided in addition to the data modem functions previously described. Country dependent parameters are all programmable by ConfigurACE.

V.25 bis Commands

V.25 bis commands (Table 2) are available in asynchronous modes when enabled by the AT/V25B bit in the External Buffer 1 inputs.

Blacklist Parameters

The modem can operate in accordance with requirements of individual countries to prevent misuse of the network by limiting repeated calls to the same number when previous call attempts have failed. Call failure can be detected for reasons such as no dial tone, number busy, no answer, no ringback detected, voice (rather than modem) detected, and key abort (dial attempt aborted by user). Actions resulting from such failures can include specification of minimum inter-call delay, extended delay between calls, and maximum numbers of retries before the number is permanently forbidden ("blacklisted"). Up to 40 such numbers may be tabulated. The blacklist parameters are established by ConfigurACE.

Dialing

Dial Tone Detection. Dial tone detection levels and frequency ranges are programmable by ConfigurACE.

DTMF Dialing. Transmit output level, DTMF signal duration, and DTMF interdigit interval parameters are programmable by ConfigurACE.

Pulse Dialing. Parameters such as make/break times, set/clear times, and dial codes are programmable by ConfigurACE.

Ring Detection. The frequency range is programmable by ConfigurACE.

Adaptive Dialing. Adaptive dialing can be disabled by ConfigurACE.

Blind Dialing. Blind dialing, permitted only in some countries, can be enabled or disabled by setting or resetting a flag bit in the corresponding country file using ConfigurACE. If enabled, blind dialing can be invoked using the ATX command; if disabled, blind dialing is not available.

Carrier Transmit Level

The carrier transmit level is programmable by ConfigurACE to match specific country and DAA characteristics.

Calling Tone

Calling tone is generated in accordance with V.25. Calling tone may be toggled (enabled/disabled) by inclusion of a "A" character in a dial string. It may also be enabled or disabled by programming a country specific parameter using ConfigurACE.

Call Progress Tone Detection

Frequency and cadence of tones for busy, ringback, congested, dial tone 1, and dial tone 2 are programmable by ConfigurACE.

Answer Tone Detection

The answer tone detection period is programmable by ConfigurACE.

Relay Control

On-hook/off-hook, make/break, and set/clear relay control parameters are programmable by ConfigurACE.

Automatic Country Code Recognition

Automatic country code recognition is supported in conjunction with country identification code circuitry provided

in the DAA. Automatic country code recognition is enabled using the AT*NCnn command with nn = 0. Automatic country code recognition is disabled using the AT*NCnn command with nn = any valid country code other than 0. (See the IDID and IDCLK parameters in Table 9.)

Once enabled, the MCU interrogates the DAA circuit upon reset (POR or the ATZ command) or attempt to go off-hook. An 8-bit country code is shifted in from the DAA and is used to look up the corresponding country code parameters loaded in ROM. If country code parameters are present for the shifted-in country code and the country is different from the active country, the country code parameters are loaded. If the shifted-in country code does match a country with stored parameters in ROM, the modem issues an ERROR message.

Note that when automatic country code recognition is enabled, the country code can be changed at any time before going off-hook (e.g., by changing the DAA or selecting a different country code on the DAA). Upon going off-hook, the MCU will then load the country code parameters corresponding to the new DAA country code.

ConfigurACE UTILITY PROGRAM

The ConfigurACE utility program allows the OEM to customize the MCU firmware to suit specific application and country requirements. ConfigurACE allows programming of functions such as:

- —Loading of multiple sets of country parameters
- —Call progress and blacklisting parameters
- —Entry of S register maximum/minimum values
- —Use of "soft switches" instead of panel switches
- —Modification/limitation of transmit levels
- —Modification of result codes
- —Modification of factory default values
- —Customization of the ATI4 response
- —Customization of fax OEM messages

This program, which runs on a PC-compatible computer, modifies the hex object code which can be programmed directly into the system ROM. Lists of the generated parameters can be displayed or printed.

Rockwell-provided country parameter files allow a complete set of country-specific call progress and blacklisting parameters to be selected.

DIAGNOSTICS

Commanded Tests

Diagnostics are performed in response to &T commands, serial interface control signals, or switch inputs per V.54.

Analog Loopback. Data from the local DTE is sent to the modem, which loops the data back to the local DTE.

Analog Loop Self Test. An internally generated test pattern of alternating 1s and 0s (reversals) is sent to the modem. An error detector within the modem checks for errors in the string of reversals.

Remote Digital Loopback (RDL). Data from the local DTE is sent to the remote modem which loops the data back to the local DTE.

Remote Digital Loopback with Self Test. An internally generated pattern is sent from the local modem to the remote modem which loops the data back to the local modem.

Local Digital Loopback. When local digital loop is requested from the local DTE, two data paths are set up in the local modem. Data from the local DTE is looped back to the local DTE (path 1) and data received from the remote modem is looped back to the remote modem (path 2).

Power On Reset Tests

Upon power on, or receipt of the Z command, the modem performs tests of the MDP, RAM, ROM, and NVRAM.

LOW POWER MODES

Sleep Mode

Entry. The modem will enter the low power sleep mode when no line connection exists and no host activity occurs for the period of time specified in the S24 register. All MCU circuits are turned off except the internal MCU clock circuitry in order to consume lower power but be able to immediately wake up and resume normal operation.

Wake-Up. Wakeup occurs when a ring is detected on the telephone line, the host writes to the modem (parallel interface version) or the DTE sends a character to the modem (serial interface version).

Stop Mode

Entry. The modem will enter the low power stop mode when the $\overline{\text{STPMODE}}$ input is asserted. All MCU circuits are turned off including the internal MCU clock circuitry in order to consume lower power than sleep mode. The modem will enter stop mode immediately, terminating a line connection, terminating any test in process, and allowing any data in the Receive Buffer Register to clear.

$\overline{\text{STPMODE}}$ must be returned high before the modem can wake-up.

Wake-Up. Wakeup occurs when a ring is detected on the telephone line, the host writes to the modem (parallel interface version) or the DTE sends a character to the modem (serial interface version). Since the modem requires more time to attain normal operation when waking up from Stop mode rather than from Sleep mode, the host must send a character to the modem before issuing the first AT command.

CALLER ID

Caller ID can be enabled/disabled using the #CID command. When enabled, caller ID information (date, time, caller code, and name) can be passed to the DTE in formatted or unformatted form. Inquiry support allows the current caller ID mode and mode capabilities of the modem to be retrieved from the modem.

ADDITIONAL INFORMATION

Additional information is described in the RC288ACi/VFC, RC240ACi/VFC, and RC192ACi/VFC Modem Designer's Guide (Order No. 899) and the AT Command Reference Manual (Order No. 1034).

HARDWARE INTERFACE

HARDWARE INTERFACE SIGNALS

The modem hardware interface signals for serial and parallel interface configurations are shown in Figures 2 and 3, respectively.

The MCU pin assignments for serial interface firmware are shown in Figure 4 and are listed in Table 5.

The MCU pin assignments for parallel interface firmware are shown in Figure 5 and are listed in Table 6.

The CEP pin assignments are shown in Figure 6 and are listed in Table 7.

The MDP pin assignments are shown in Figure 7 and are listed in Table 8.

The MCU hardware interface signals are defined in Table 9.

The MDP hardware interface signals are defined in Table 10.

The CEP hardware interface signals are defined in Table 11.

The digital electrical characteristics for the hardware interface signals are listed in Table 12.

The analog electrical characteristics for the hardware interface signals are listed in Table 13.

The current and power requirements are listed in Table 14.

The absolute maximum ratings are listed in Table 15.

Table 16 shows the parallel interface registers and the corresponding bit assignments.

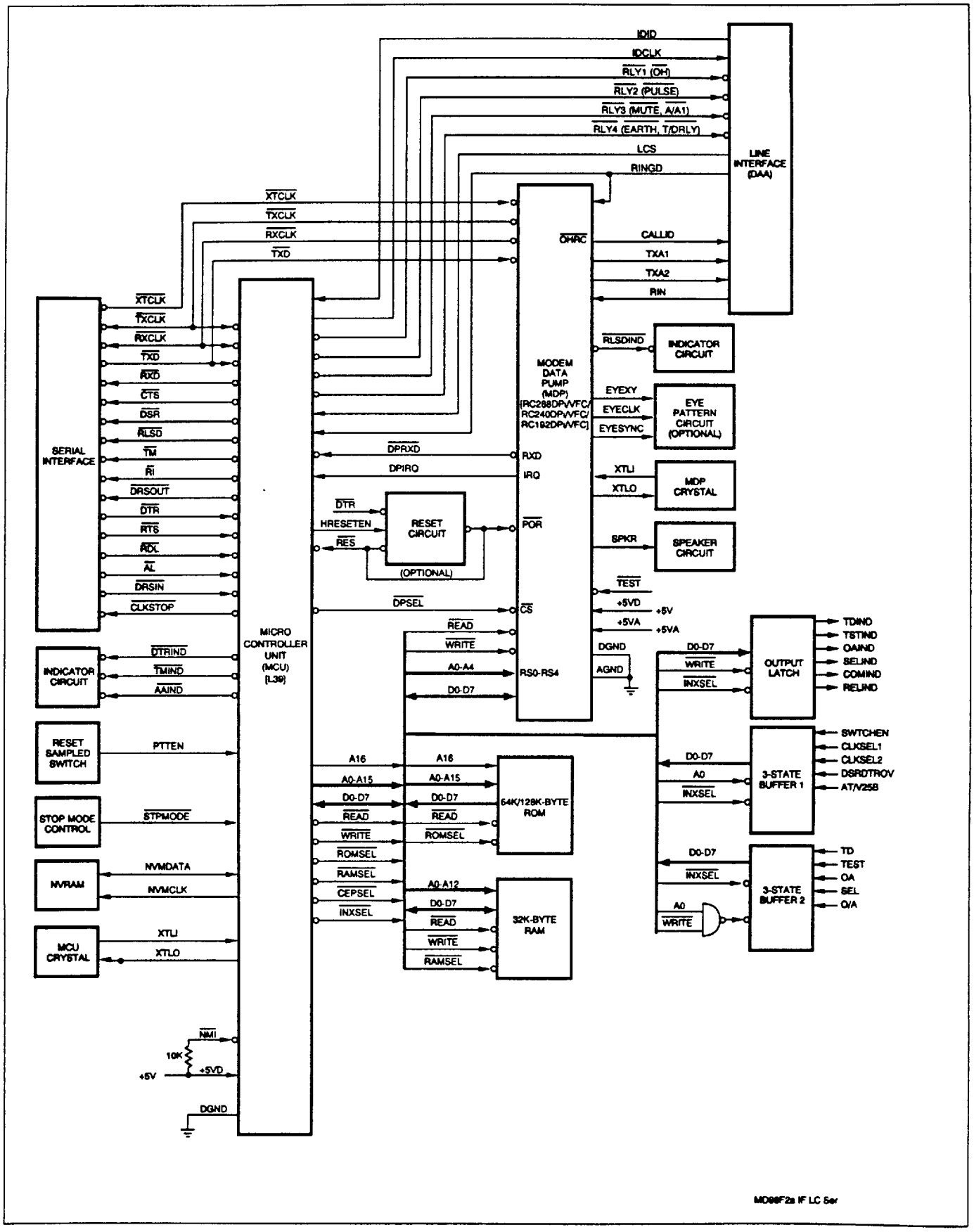


Figure 2a. Hardware Signals-Serial I/F-Low Cost

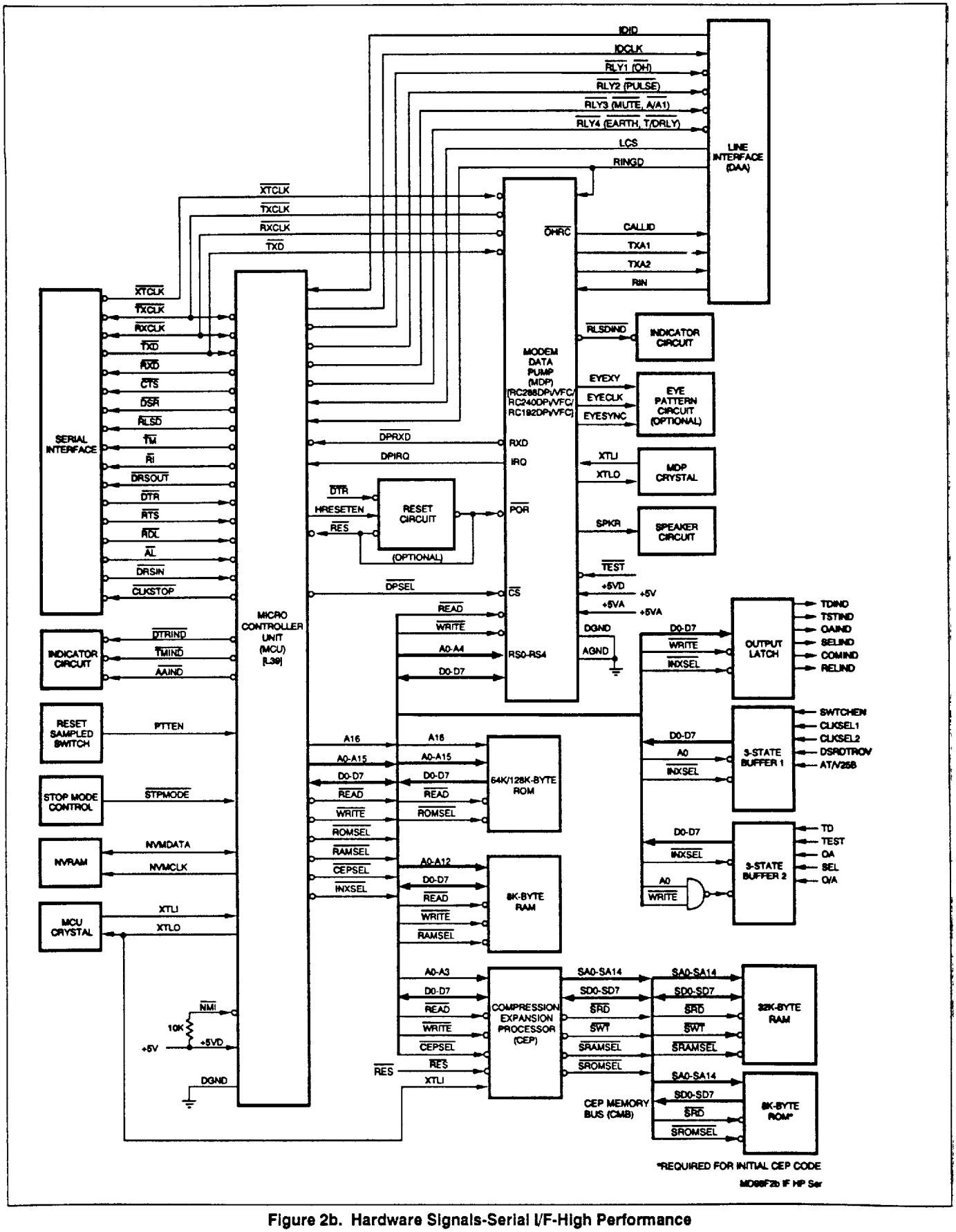


Figure 2b. Hardware Signals-Serial I/F-High Performance

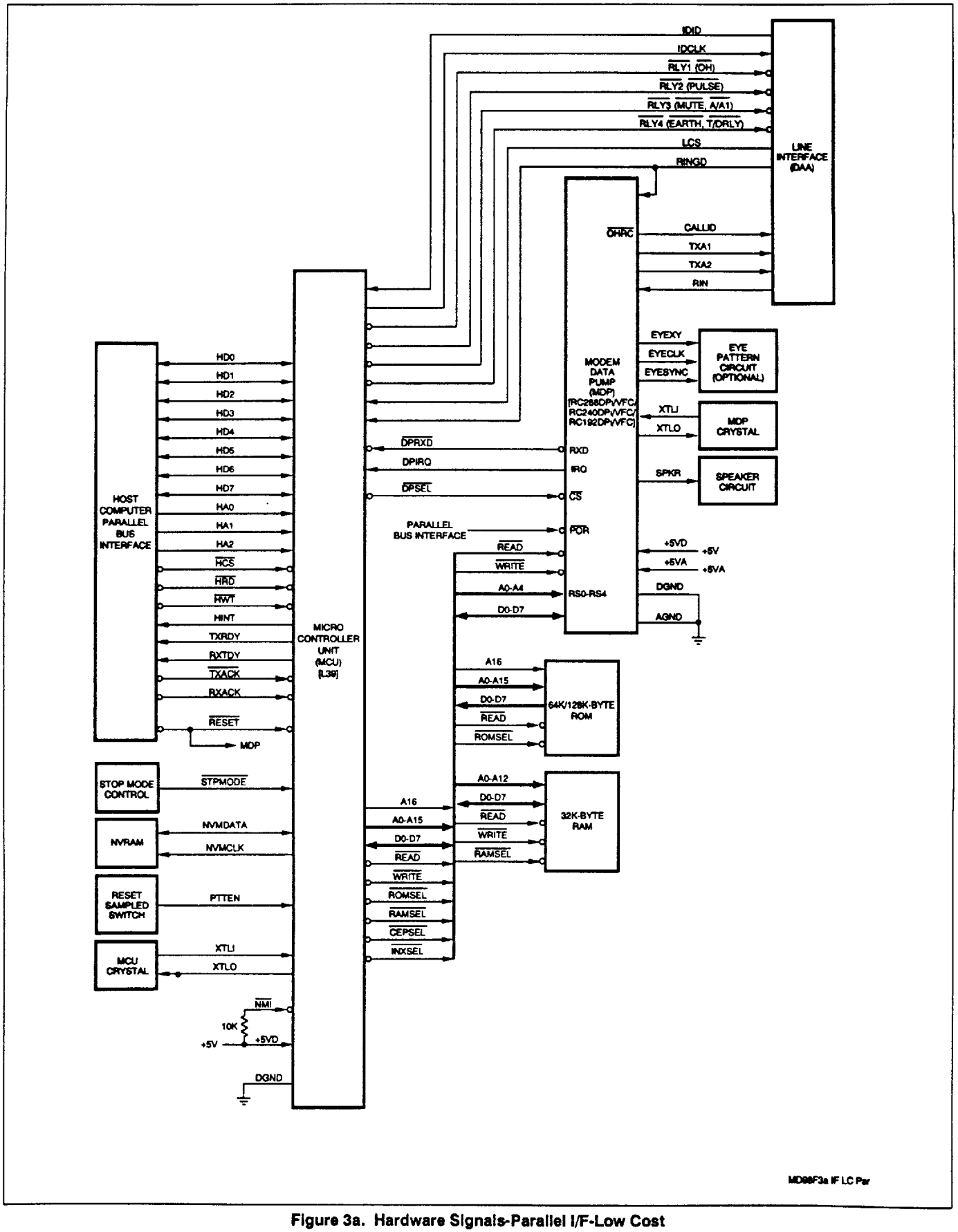


Figure 3a. Hardware Signals-Parallel I/F-Low Cost

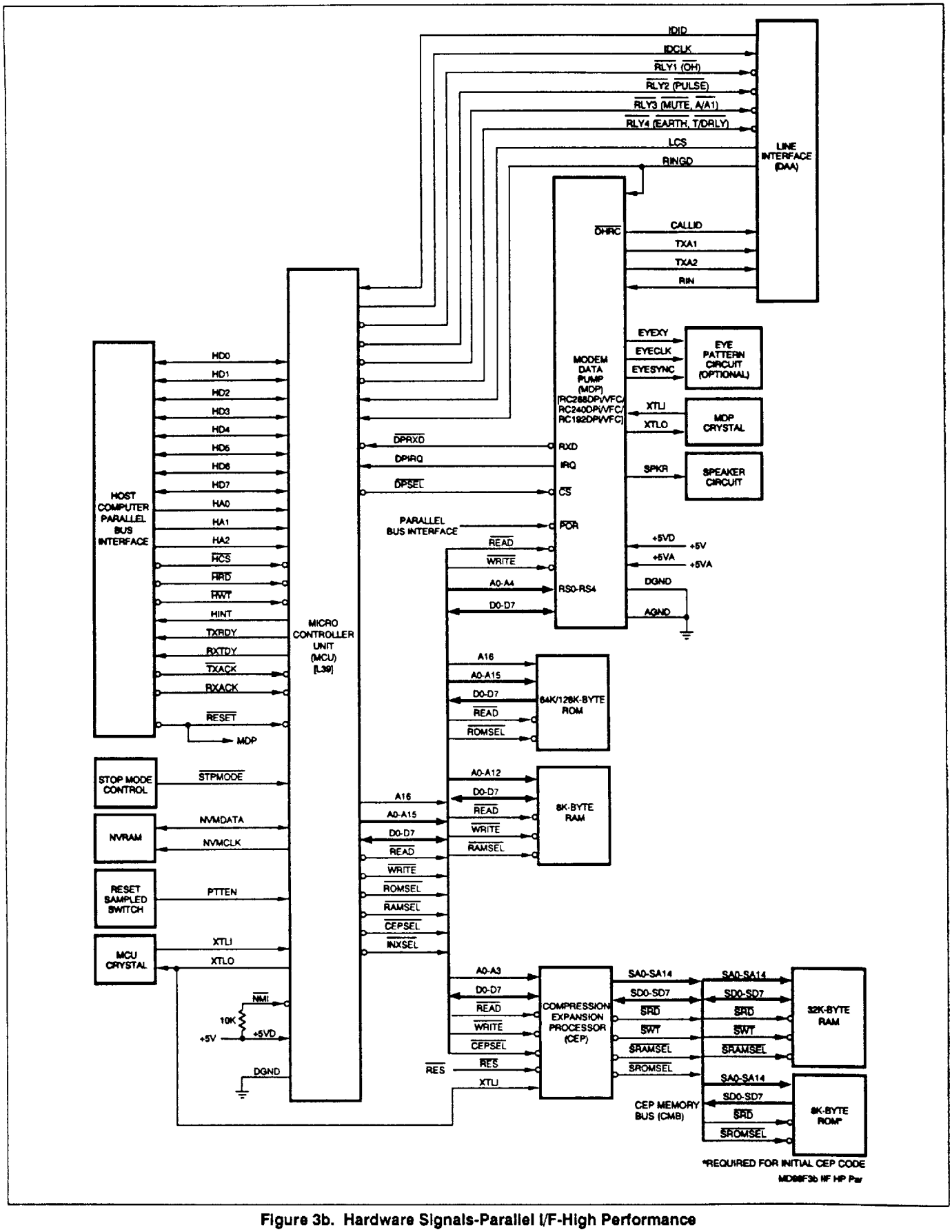


Figure 3b. Hardware Signals-Parallel I/F-High Performance

Table 5. MCU Pin Signals - Serial I/F - 84-Pin PLCC

Pin	MCU Signal	I/O Type	Modem Signal
1	PE0	OA	RLY1 (OH)
2	PE1	OA	RLY2 (PULSE)
3	GND1	GND	GND
4	PB0	OA	A16
5	PB1	OA	DPSEL
6	PB2	OA	ROMSEL
7	PB3	OA	RAMSEL
8	PB4	OA	INXSEL
9	PB5	OA	CEPSEL
10	PB6	OA	AAIND
11	PB7	OA	TMIND
12	RES	IC	RES
13	NMI	MI	NMI (Note 4)
14	WT	OA	WRITE
15	RD	OA	READ
16	PE2	OA	RLY3 (MUTE, A/A1)
17	PE3	OA	RLY4 (EARTH, T/DRLY)
18	NC		NC
19	VCC1	PWR	+5VDC
20	XTLI	IE	XTLI
21	XTLO	OE	XTLO
22	GND2	GND	GND
23	GND3	GND	GND
24	MK6	MI	Connect to GND
25	PC0	OA	DSR
26	PC1	OA	CTS
27	PC2	OA	RLSD
28	PC3	OA	DRSOUT
29	PC4	IA	DRSIN
30	PC5	OA	RI
31	PC6	OA	TM
32	PC7	IA	RDL
33	SYNC		NC
34	PD0	OA	DTRIND
35	PD1	IA	HRESETEN
36	PD2		NC
37	PD3	IA	STPMODE
38	PD4	IA	DTR
39	PD5	IA	AL
40	PD6	IA	RTS
41	PD7	IA	DPIRQ
42	GND6	GND	GND
43	PE4	IA	LCS
44	PE5	OA [IA]	CLKSTOP [PTTEN]
45	PA0	IA	RINGD
46	PA1	IA/OA	NVMDATA (Note 4)
47	PA2	IA	TXD
48	PA3	IA	TXCLK
49	PA4	IA	RXCLK
50	PA5	MI	DPRXD
51	PA6	OA	RXD
52	PA7	OA	NVMCLK
53	TST	MI	Connect to GND
54	D0	IA/OA	D0
55	D1	IA/OA	D1
56	D2	IA/OA	D2
57	D3	IA/OA	D3
58	D4	IA/OA	D4
59	D5	IA/OA	D5
60	D6	IA/OA	D6

Table 5. MCU Pin Signals-Ser I/F-84-Pin PLCC (Cont'd)

Pin	MCU Signal	I/O Type	Modem Signal
61	D7	IA/OA	D7
62	PE6	OA	IDCLK
63	PE7	IA	IDID
64	VCC2	PWR	+5VDC
65	GND4	GND	GND
66	MK7		Connect to GND
67	GND8	GND	GND
68	A0	OA	A0
69	A1	OA	A1
70	A2	OA	A2
71	A3	OA	A3
72	A4	OA	A4
73	A5	OA	A5
74	A6	OA	A6
75	SC2		NC
76	A7	OA	A7
77	A8	OA	A8
78	A9	OA	A9
79	A10	OA	A10
80	A11	OA	A11
81	A12	OA	A12
82	A13	OA	A13
83	A14	OA	A14
84	A15	OA	A15

Notes:
1. MI = Modem interconnect.
2. NC = No external connection.
3. NU = Not used; connect as noted.
4. Connect to +5 VDC through 10 KΩ.

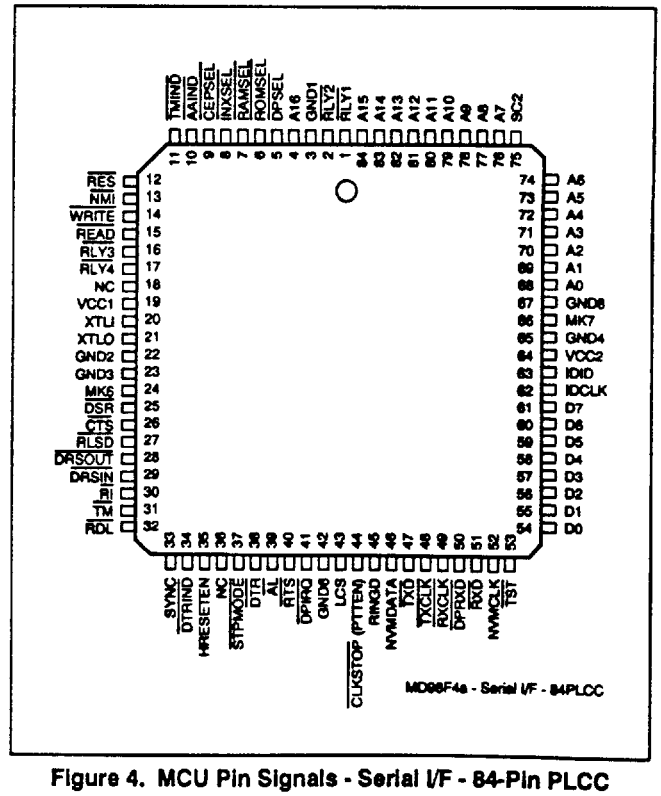


Figure 4. MCU Pin Signals - Serial I/F - 84-Pin PLCC

Table 6. MCU Pin Signals - Parallel I/F - 84-Pin PLCC

Pin	MCU Signal	I/O Type	Modem Signal
1	PE0	OA	RLY1 (OH)
2	PE1	OA	RLY2 (PULSE)
3	GND1	GND	GND
4	PB0	OA	A16
5	PB1	OA	DPSEL
6	PB2	OA	ROMSEL
7	PB3	OA	RAMSEL
8	PB4		NC
9	PB5	OA	CEPSEL
10	PB6		NC
11	PB7	OA	HINT
12	RES	IC	RES
13	NMI	MI	NMI (Note 4)
14	WT	OA	WRITE
15	RD	OA	READ
16	PE2	OA	RLY3 (MUTE, A/A1)
17	PE3	OA	RLY4 (EARTH, T/DRLY)
18	NC		NC
19	VCC1	PWR	+5VDC
20	XTLI	IE	XTLI
21	XTLO	OE	XTLO
22	GND2	GND	GND
23	GND3	GND	GND
24	MK6	MI	Connect to GND
25	PC0	IA/OA	HD0
26	PC1	IA/OA	HD1
27	PC2	IA/OA	HD2
28	PC3	IA/OA	HD3
29	PC4	IA/OA	HD4
30	PC5	IA/OA	HD5
31	PC6	IA/OA	HD6
32	PC7	IA/OA	HD7
33	SYNC		NC
34	PD0	IA	HA0
35	PD1	IA	HA1
36	PD2	IA	HA2
37	PD3	IA	STPMODE
38	PD4	IA	HCS
39	PD5	IA	HWT
40	PD6	IA	HRD
41	PD7	IA	DPIRQ
42	GND6	GND	GND
43	PE4	IA	LCS
44	PE5	IA	PTTEN
45	PA0	IA	RINGD
46	PA1	IA/OA	NVMDATA (Note 4)
47	PA2		NC
48	PA3	IA	TXACK
49	PA4	IA	RXACK
50	PA5	OA	TXRDY
51	PA6	OA	RXRDY
52	PA7	OA	NVMCLK
53	TST	MI	Connect to GND
54	D0	IA/OA	D0
55	D1	IA/OA	D1
56	D2	IA/OA	D2
57	D3	IA/OA	D3
58	D4	IA/OA	D4
59	D5	IA/OA	D5
60	D6	IA/OA	D6

Table 6. MCU Pin Signals-Par I/F-84-Pin PLCC (Cont'd)

Pin	MCU Signal	I/O Type	Modem Signal
61	D7	IA/OA	D7
62	PE6	OA	IDCLK
63	PE7	IA	IDID
64	VCC2	PWR	+5VDC
65	GND4	GND	GND
66	MK7		Connect to GND
67	GND8	GND	GND
68	A0	OA	A0
69	A1	OA	A1
70	A2	OA	A2
71	A3	OA	A3
72	A4	OA	A4
73	A5	OA	A5
74	A6	OA	A6
75	SC2		NC
76	A7	OA	A7
77	A8	OA	A8
78	A9	OA	A9
79	A10	OA	A10
80	A11	OA	A11
81	A12	OA	A12
82	A13	OA	A13
83	A14	OA	A14
84	A15	OA	A15

Notes:
1. MI = Modem interconnect.
2. NC = No external connection.
3. NU = Not used; connect as noted.
4. Connect to +5 VDC through 10 KΩ.

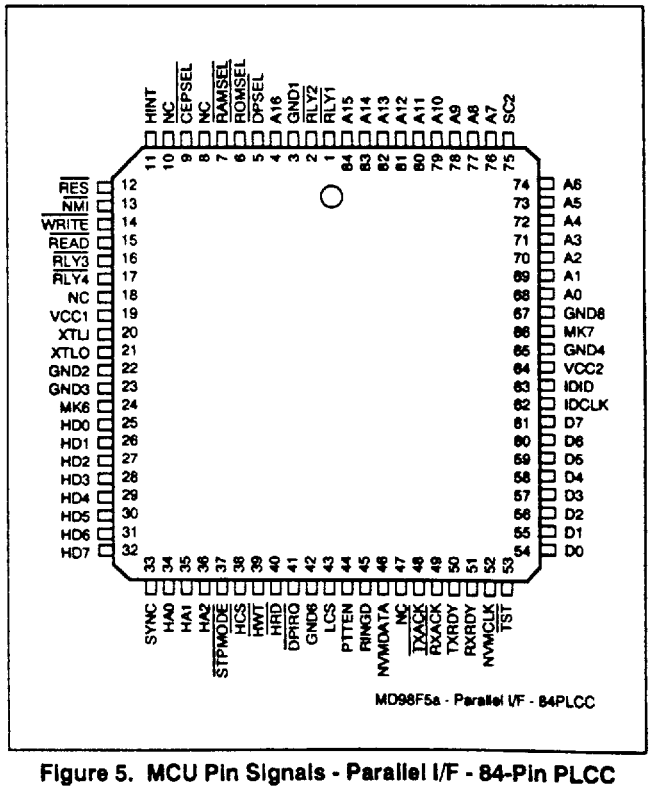


Figure 5. MCU Pin Signals - Parallel I/F - 84-Pin PLCC

Table 7. CEP Pin Signals - 84-Pin PLCC

Pin	MCU Signal	I/O Type	Modem Signal
1	PE0		NC
2	PE1		NC
3	GND1	GND	GND
4	PB0		NC
5	PB1		NC
6	PB2	OA	$\overline{\text{SROMSEL}}$
7	PB3	OA	$\overline{\text{SRAMSEL}}$
8	PB4		NC
9	PB5		NC
10	PB6		NC
11	PB7		NC
12	$\overline{\text{RES}}$	IC	$\overline{\text{RES}}$
13	$\overline{\text{NMI}}$	MI	$\overline{\text{NMI}}$ (Note 4)
14	$\overline{\text{WT}}$	OA	$\overline{\text{SWT}}$
15	$\overline{\text{RD}}$	OA	$\overline{\text{SRD}}$
16	PE2		NC
17	PE3		NC
18	NC		NC
19	VCC1	PWR	+5VDC
20	XTLI	IE	XTLI
21	XTLO	OE	XTLO
22	GND2	GND	GND
23	GND3	GND	GND
24	MK6	MI	Connect to GND
25	PC0	IA/OA	MCU: D0
26	PC1	IA/OA	MCU: D1
27	PC2	IA/OA	MCU: D2
28	PC3	IA/OA	MCU: D3
29	PC4	IA/OA	MCU: D4
30	PC5	IA/OA	MCU: D5
31	PC6	IA/OA	MCU: D6
32	PC7	IA/OA	MCU: D7
33	SYNC		NC
34	PD0	IA	MCU: A0
35	PD1	IA	MCU: A1
36	PD2	IA	MCU: A2
37	PD3	IA	MCU: A3
38	PD4	IA	MCU: $\overline{\text{CEPSEL}}$
39	PD5	IA	MCU: $\overline{\text{WT}}$
40	PD6	IA	MCU: $\overline{\text{RD}}$
41	PD7		NC
42	GND6	GND	GND
43	PE4		NC
44	PE5		NC
45	PA0		NC
46	PA1		NC
47	PA2		NC
48	PA3	IA	$\overline{\text{TXACK}}$ (Note 4)
49	PA4	IA	$\overline{\text{RXACK}}$ (Note 4)
50	PA5		NC
51	PA6		NC
52	PA7		NC
53	$\overline{\text{TST}}$	MI	Connect to GND (Note 5)
54	D0	IA/OA	SD0
55	D1	IA/OA	SD1
56	D2	IA/OA	SD2
57	D3	IA/OA	SD3
58	D4	IA/OA	SD4
59	D5	IA/OA	SD5
60	D6	IA/OA	SD6

Table 7. CEP Pin Signals -84-Pin PLCC (Cont'd)

Pin	MCU Signal	I/O Type	Modem Signal
61	D7	IA/OA	SD7
62	PE6		NC
63	PE7		NC
64	VCC2	PWR	+5VDC
65	GND4	GND	GND
66	MK7		Connect to GND
67	GND8	GND	GND
68	A0	OA	SA0
69	A1	OA	SA1
70	A2	OA	SA2
71	A3	OA	SA3
72	A4	OA	SA4
73	A5	OA	SA5
74	A6	OA	SA6
75	SC2		NC
76	A7	OA	SA7
77	A8	OA	SA8
78	A9	OA	SA9
79	A10	OA	SA10
80	A11	OA	SA11
81	A12	OA	SA12
82	A13	OA	SA13
83	A14	OA	SA14
84	A15	OA	NC

Notes:
1. MI = Modem interconnect.
2. NC = No external connection.
3. NU = Not used; connect as noted.
4. Connect to +5 VDC through 10 KΩ.
5. Connect to GND if optional external ROM is installed; otherwise NC .

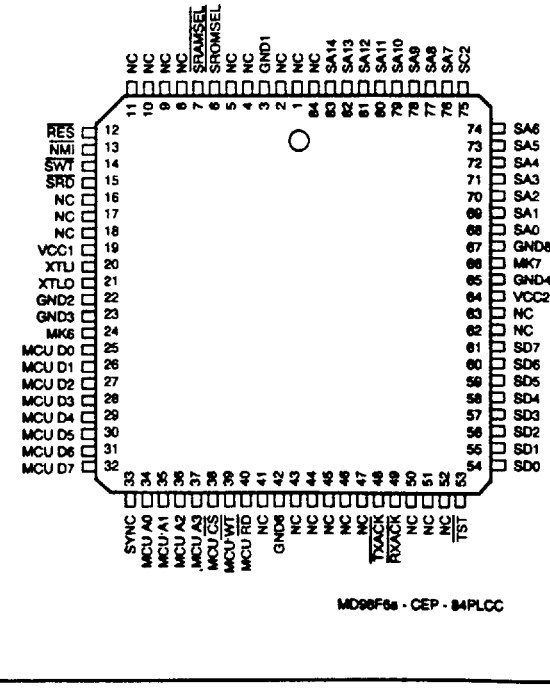


Figure 6. CEP Pin Signals- 84-Pin PLCC

Table 8. MDP Pin Signals - 68-Pin PLCC

Pin	Signal Label	I/O Type	Interface
1	VREG	MI	To GND through 0.1 μF[3]
2	DSP_RESET	MI	MDP: $\overline{RES}$
3	IA_CLKIN	MI	MDP: CLKIN
4	DSP_IRQ	MI	MDP: $\overline{IRQ}$
5	$\overline{RI}$/TXRQ	OA	NC
6	RINGD	IA	Line Interface
7	$\overline{RTS}$	IA	To +5VD through 10KΩ
8	IRQ	OA	MCU: $\overline{DPIRQ}$
9	D1	IA/OA	MCU: D1
10	GND1	GND	GND
11	+5VD1	PWR	+5VDC
12	XTLI	I	Crystal/Clock Circuit
13	XTLO	O	Crystal/Clock Circuit
14	D0	IA/OA	MCU: D0
15	D2	IA/OA	MCU: D2
16	D3	IA/OA	MCU: D3
17	D5	IA/OA	MCU: D5
18	D7	IA/OA	MCU: D7
19	DGND2	GND	GND
20	RS0	IA	MCU: A0
21	+5VA	PWR	+5VA
22	AGND1	GND	GND
23	RIN	I(DA)	Line Interface
24	VC		To GND through capacitors
25	VREF		To VC through capacitors
26	TXA2	O(DD)	Line Interface
27	TXA1	O(DD)	Line Interface
28	$\overline{TALK}$	OD	NC
29	SPKR	O(DF)	Speaker Circuit
30	AGND2	GND	GND
31	$\overline{OHRC}$	OD	CALLID to Line Interface
32	$\overline{POR}$	MI	MDP: $\overline{RESET}$
33	CLKIN	MI	MDP: IA_CLKOUT
34	$\overline{DTR}$	IA	To +5VD through 10KΩ
35	RXD	OA	MCU: $\overline{DPRXD}$
36	+5VD2	PWR	+5VD
37	$\overline{CTS}$	OA	NC
38	$\overline{IRQ}$	MI	MDP: DSP_IRQ
39	$\overline{RES}$	MI	MDP: DSP_RESET
40	DGND3	GND	GND
41	+5VD3	PWR	+5VD
42	RXOUT		NC
43	DGND4	GND	GND
44	RMODE	MI	MDP: TMODE
45	TMODE	MI	MDP: RMODE
46	EYESYNC	OA	Eye Pattern Circuit
47	EYECLK	OA	Eye Pattern Circuit
48	EYEXY	OA	Eye Pattern Circuit
49	TXDAT		NC
50	TDCLK	OA	DTE/MCU: $\overline{TXCLK}$
51	$\overline{RLSD}$	OA	$\overline{RLSDIND}$
52	$\overline{RDCLK}$	OA	DTE/MCU: $\overline{RXCLK}$
53	GP0	MI	Connect to EYESYNC
54	XTCLK	IA	DTE : $\overline{XTCLK}$
55	DGND5	GND	GND
56	+5VD4	PWR	+5VD
57	TXD	IA	DTE/MCU: $\overline{TXD}$
58	$\overline{DSR}$/RXRQ	OA	NC
59	$\overline{RESET}$	OA	MCU: $\overline{RES}$
61	A7	OA	RAM: A7

Table 8. MDP Pin Assignments - 68-Pin PLCC (Cont'd)

Pin	Signal Label	I/O Type	Interface
61	$\overline{WRITE}$	IA	MCU: $\overline{WRITE}$
62	$\overline{CS}$	IA	MCU: $\overline{DPSEL}$
63	RS4	IA	MCU: A4
64	RS3	IA	MCU: A3
65	RS2	IA	MCU: A2
66	RS1	IA	MCU: A1
67	D6	IA/OA	MCU: D6
68	D4	IA/OA	MCU: D4

Notes:

1. I/O types:
   - MI = Modem interconnect.
   - IA, IB = Digital input.
   - OA, OB, OD = Digital output.
   - I(DA)] = Analog input.
   - O(DD), O(DF) = Analog output.
2. NC = No external connection.
3. VREG pin can be NC; capacitor connection required for compatibility with future products.

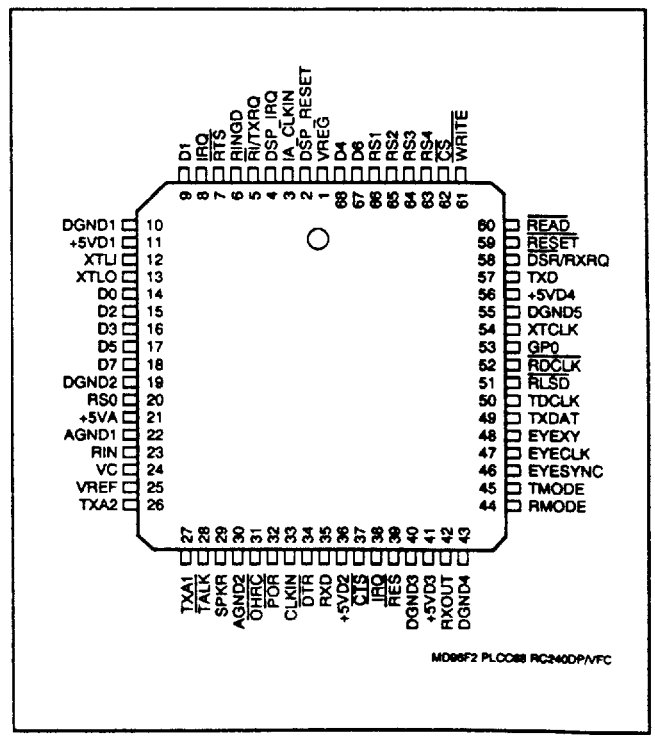


Figure 7. MDP Pin Assignments- 68-Pin PLCC

Table 9. MCU Signal Definitions

Label	I/O Type	Signal Name/Description
		MCU SYSTEM
XTLI, XTLO	IE, OE	**MCU Crystal/Clock In and Crystal Out.** Connect to an external crystal circuit consisting of a 12.9024 MHz crystal (high performance configuration, i.e., with CEP) or 14.7456 MHz crystal (low cost configuration, i.e., without CEP), and a capacitance network.
$\overline{\text{RES}}$	IC	**MCU Reset.** The active low $\overline{\text{RES}}$ input resets the MCU logic, and restores the saved configuration from NVRAM, or returns the modem to the factory default values if NVRAM is not present. For serial interface, the $\overline{\text{RES}}$ input is typically connected to MDP $\overline{\text{POR}}$ pin and a reset circuit. For parallel interface, the $\overline{\text{RES}}$ input is connected to the MDP $\overline{\text{POR}}$ pin and the host bus RESET line through an inverter.
$\overline{\text{DPIRQ}}$	IA	**MDP Interrupt Request.** Connect to the MDP IRQ output.
$\overline{\text{DPRXD}}$	IA	**MDP Received Data.** Connect to the MDP MRXD output.
VCC1, VCC2	PWR	**+ 5V Digital Supply.** +5V ± 5%.
GND1-GND8	GND	**Digital Ground.** Connect to ground.
		LINE INTERFACE
$\overline{\text{RLY1}}$	OA	**Relay 1 Control** ($\overline{\text{OH}}$). The active low $\overline{\text{RLY1}}$ output can be used to control the normally open off-hook relay.
$\overline{\text{RLY2}}$	OA	**Relay 2 Control** ($\overline{\text{PULSE}}$). The active low $\overline{\text{RLY2}}$ output can be used to control the normally open pulse dial relay.
$\overline{\text{RLY3}}$	OA	**Relay 3 Control** ($\overline{\text{MUTE}}$, $\overline{\text{A/A1}}$). The active low $\overline{\text{RLY3}}$ output can be used to control the normally open mute relay or the normally open key telephone hold indicator (A/A1) relay.
$\overline{\text{RLY4}}$	OA	**Relay 4 Control** ($\overline{\text{EARTH}}$, $\overline{\text{T/DRLY}}$). The active low $\overline{\text{RLY4}}$ output can be used to control the normally open earthing relay or the normally closed talk/data relay.
LCS	IA	**Line Current Sense.** LCS is an active high input that indicates an handset off-hook status.
RINGD	IA	**Ring Frequency.** A high-going edge on the RINGD input initiates an internal ring frequency measurement. The RINGD input from an external ring detect circuit is monitored to determine when to wake up from sleep or stop mode. The RINGD input is typically connected to the output of an optoisolator or equivalent. The idle state (no ringing) output of the ring detect circuit should be low.
IDCLK	OA	**Country Identifier Clock.** IDCLK is an output clock to the country identifier shift register.
IDID	IA	**Country Identifier Code.** IDID is an input serial stream from the country identifier shift register.
		NVRAM INTERFACE
NVMCLK	OA	**NVRAM Clock.** NVMCLK output high enables the NVRAM.
NVMDATA	IA/OA	**NVRAM Data.** The NVMDATA pin supplies a serial data interface to the NVRAM.
		EXTERNAL MEMORY BUS INTERFACE
A0-A15	OA	**Address Lines 0-15.** A0-A15 are the external memory bus address lines.
A16	OA	**Address Line 16.** A16 is a bank select line.
D0-D7	IA/OA	**Data Line 0-7.** D0-D7 are the external memory bus data lines.
$\overline{\text{READ}}$	OA	**Read Enable.** $\overline{\text{READ}}$ output low enables data transfer from the selected device to the D0-D7 lines.
$\overline{\text{WRITE}}$	OA	**Write Enable.** $\overline{\text{WRITE}}$ output low enables data transfer from the D0-D7 lines to the selected device.
$\overline{\text{DPSEL}}$	OA	**Modem Data Pump Select.** $\overline{\text{DPSEL}}$ output low selects the MDP.
$\overline{\text{RAMSEL}}$	OA	**RAM Select.** $\overline{\text{RAMSEL}}$ output low selects the external RAM.
$\overline{\text{ROMSEL}}$	OA	**ROM Select.** $\overline{\text{ROMSEL}}$ output low selects the external 64k/128k-byte ROM.
$\overline{\text{CEPSEL}}$	OA	**CEP Select.** $\overline{\text{CEPSEL}}$ output low selects the CEP.
$\overline{\text{INXSEL}}$	OA	**Input Buffer Select.** $\overline{\text{INXSEL}}$ output low and A0 high select external input buffer 1. $\overline{\text{INXSEL}}$ output low and A0 NANDed with $\overline{\text{WRITE}}$ select external input buffer 2. $\overline{\text{INXSEL}}$ output low clocked by $\overline{\text{WRITE}}$ select the external latch. (Serial interface only.)

Table 9. MCU Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		V.24 (EIA-232-D) SERIAL INTERFACE (SERIAL INTERFACE ONLY)
		The serial interface signals correspond functionally to V.24/EIA-232-D signals. The signals levels are TTL compatible and are inverted from V.24/EIA-232-D levels.
$\overline{TXD}$	IA	**Transmitted Data (EIA BA/CCITT CT103).** The DTE uses the $\overline{TXD}$ line to send data to the modem for transmission over the telephone line or to transmit commands to the modem.
$\overline{RXD}$	OA	**Received Data (EIA BB/CCITT CT 104).** The modem uses the $\overline{RXD}$ line to send data received from the telephone line to the DTE and to send modem responses to the DTE. During command mode, $\overline{RXD}$ data represents the modem responses to the DTE.
$\overline{CTS}$	OA	**Clear To Send (EIA CB/CCITT CT106).** $\overline{CTS}$ output ON (low) indicates that the DTE is ready to accept data from the DTE. In asynchronous operation, in error correction or normal mode, $\overline{CTS}$ is always ON (low) unless RTS/CTS flow control is selected by the &Kn command. In synchronous operation, the modem also holds $\overline{CTS}$ ON during asynchronous command state. The modem turns $\overline{CTS}$ OFF immediately upon going off-hook and holds $\overline{CTS}$ OFF until both $\overline{DSR}$ and $\overline{RLSD}$ are ON and the modem is ready to transmit and receive synchronous data. The modem can also be commanded by the &Rn command to turn $\overline{CTS}$ ON in response to an $\overline{RTS}$ OFF-to-ON transition.
$\overline{DSR}$	OA	**Data Set Ready (EIA CC/CCITT CT107).** $\overline{DSR}$ indicates modem status to the DTE. $\overline{DSR}$ OFF (high) indicates that the DTE is to disregard all signals appearing on the interchange circuits except Ring Indicator (RI). $\overline{DSR}$ output is controlled by the AT&Sn command.
$\overline{RLSD}$	OA	**Received Line Signal Detector (EIA CF/CCITT CT109).** When AT&C0 command is not in effect, $\overline{RLSD}$ output is ON when a carrier is detected on the telephone line or OFF when carrier is not detected.
$\overline{TM}$	OA	**Test Mode Indicate (EIA TM/CCITT CT142).** The $\overline{TM}$ output indicates the modem is in test mode (low) or in any other mode (high).
$\overline{RI}$	OA	**Ring Indicator (EIA CE/CCITT CT125).** $\overline{RI}$ output ON (low) indicates the presence of an ON segment of a ring signal on the telephone line.
$\overline{DRSOUT}$	OA	**Data Signalling Rate Indicator (EIA CI/CCITT CT112).** $\overline{DRSOUT}$ is ON (low) when the modem desires or is engaged in the high speed (2400 bps or higher) mode. $\overline{DRSOUT}$ is OFF (high) otherwise.
$\overline{DTR}$	IA	**Data Terminal Ready (EIA CD/CCITT CT108).** The $\overline{DTR}$ input is turned ON (low) by the DTE when the DTE is ready to transmit or receive data. $\overline{DTR}$ ON prepares the modem to be connected to the telephone line, and maintains the connection established by the DTE (manual answering) or internally (automatic answering). $\overline{DTR}$ OFF places the modem in the disconnect state under control of the &Dn and &Qn commands.
$\overline{RTS}$	IA	**Request To Send (EIA CA/CCITT CT105).** $\overline{RTS}$ input ON (low) indicates that the the DTE is ready to accept data from the modem. In the command state, the modem ignors $\overline{RTS}$. In asynchronous operation, the modem ignors $\overline{RTS}$ unless RTS/CTS flow control is selected by the &Kn command. In synchronous on-line operation, the modem can be commanded by the &Rn command to ignor $\overline{RTS}$ or to respond to $\overline{RTS}$ by turning on $\overline{CTS}$ after the delay specified by Register S26.
$\overline{RDL}$	IA	**Remote Digital Loop Select (EIA RL/CCITT CT140).** $\overline{RDL}$ input low activates remote digital loop request. The loop is executed at the speed for which the modem is currently configured.
$\overline{AL}$	IA	**Analog Loop (EIA LL/CCITT CT141).** The $\overline{AL}$ input low causes the modem to assume the analog loop test mode.
$\overline{DRSIN}$	IA	**Data Signalling Rate Select (EIA CI/CCITT CT111).** This signal, relevant only in Central Europe, applies only to V.22 bis and V.22 modes. $\overline{DRSIN}$ ON (low) will result in a 2400 bps connection. $\overline{DRSIN}$ OFF (high) will force a 1200 bps connection, or will result in a fallback from 2400 bps to 1200 bps if already on-line.

Table 9. MCU Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		LED INDICATOR CIRCUIT INTERFACE (SERIAL INTERFACE ONLY)
$\overline{\text{AAIND}}$	OA	**Auto Answer Indicator.** $\overline{\text{AAIND}}$ output ON (low) corresponds to the indicator on. $\overline{\text{AAIND}}$ output is active when modem will answer the ring automatically (ATS0 command ≠ 0).
$\overline{\text{TMIND}}$	OA	**Test Mode Indicator.** $\overline{\text{TMIND}}$ output ON (low) corresponds to the indicator on. $\overline{\text{TMIND}}$ output pulses (LED flashes) when modem is in test mode and if an error is detected.
$\overline{\text{DTRIND}}$	OA	**DTR Indicator.** $\overline{\text{DTRIND}}$ output ON (low) corresponds to the indicator on. The $\overline{\text{DTRIND}}$ state reflects the $\overline{\text{DTR}}$ output state except when the &D0 command is active, in which case $\overline{\text{DTRIND}}$ is low.
		AUXILIARY CIRCUITS (SERIAL INTERFACE ONLY)
$\overline{\text{CLKSTOP}}$	OA	**Clock Stop.** Active low output that can be used to force the $\overline{\text{RXCLK}}$ and $\overline{\text{TXCLK}}$ outputs high to the DTE.
		RESET SAMPLED DIRECT SWITCH INPUT TO MCU
		This switch input can be read upon power up or after a warm reset.
PTTEN	IA	**PTT Test Enable.** The PTTEN input enables (high) or disables (low) the use of the PTT test commands. PTTEN is checked only for countries which do not permit the use of the %TT command at the approval site (e.g., Germany).
		EXTERNAL BUFFER 1 INPUTS TO MCU (SERIAL INTERFACE ONLY)
		Switch inputs are available via external buffer 1 as enabled by ConfigurACE. These inputs are sampled onto the data bus, typically via a 74HCT541 three-state buffer (see $\overline{\text{INXSEL}}$). The data bus bit number for each signal is defined below.
SWTCHEN	Bus	**Switch Enable.** The SWTCHEN input (bit 0) enables (high) or disables (low) use of external switch inputs to invoke AT commands and S Register functions rather than default values from ROM.
CLKSEL1/2	Bus	**Clock Select 1 and 2.** The CLKSEL1 and CLKSEL2 inputs (bits 1 and 2, respectively) select async/sync operation and the clock source for synchronous operation. The selectable options are:

Mode/Clock Source	CLKSEL1	CLKSEL2
Asynchronous	L	L
Synchronous with Internal clock	L	H
Synchronous with External clock	H	L
Synchronous with Slave clock	H	H

DSRDTROV	Bus	**DSR/DTR Override.** The DSRDTROV input (bit 3) enables (high) or disables (low) override of DSR and DTR from the EIA (V.24) interface.
AT/V25B	Bus	**AT/V.25 bis Commands Select.** The AT/V25B input (bit 5) selects V.25 bis (high) or AT command (low) operation.

Table 9. MCU Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		EXTERNAL BUFFER 2 INPUTS TO MCU (SERIAL INTERFACE ONLY)
		Four momentary switch (TD, TEST, OA, and SEL) and one discrete switch (O/A) inputs are available via external buffer 2 as enabled by ConfigurACE. These inputs are sampled onto the data bus, typically via a 74HCT541 three-state buffer (see INXSEL). The momentary switch inputs are asserted upon the ON-to-OFF transition. The data bus bit number for each signal is defined below.
TD	Bus	**Data/Talk.** TD input (bit 0) operation depends upon the SELIND, TDIND, and TSTIND outputs. a. If SELIND is ON, the TD input ON-to-OFF transition steps the selected directory to the next entry (see SELIND output). b. If SELIND is OFF and TDIND is ON, the TD input ON-to-OFF transition will cause the modem to disconnect from the line. c. If SELIND is OFF and TDIND is OFF, the telephone set may be used for voice communication. If a directory entry has been selected, TD ON-to-OFF transition will cause the modem to dial the telephone number from the selected directory entry. If no directory entry has been selected, the modem will go off-hook and attempt a handshake depending upon the OAIND output state.
TEST	Bus	**Test.** TEST input (bit 1) operation depends upon the SELIND, TDIND, and TSTIND outputs. a. If SELIND is ON, the TEST input is not operative. b. If SELIND is OFF and TSTIND is ON, the modem is in a test mode. The TEST ON-to-OFF transition will cause the modem to exit the test mode and to turn TSTIND OFF. c. If SELIND is OFF, TSTIND is OFF, and TDIND is OFF, the TEST ON-to-OFF transition will cause the modem to enter local analog loopback (V.54 loop 3) and to turn the TSTIND ON. d. If SELIND is OFF, TSTIND is OFF, and TDIND is ON, the TEST ON-to-OFF transition will cause the modem to establish remote digital loopback (V.54 loop 2) in the remote modem and turn TSTIND ON. If the remote end does not accept the RDL then TSTIND will not be turned ON and the modem will remain in data mode.
OA	Bus	**Answer/Originate.** If SELIND is OFF, the OA input (bit 2) ON-to-OFF transition will toggle the OAIND output to answer (ON) or originate (OFF). If SELIND is ON, the OA input is not operative.
SEL	Bus	**Select.** The SEL ON-to-OFF transition will toggle the SELIND output to ON or OFF.
O/A	Bus	**Originate/Answer.** The O/A input selects answer (ON) or originate (OFF) mode.
		EXTERNAL LATCHED OUTPUTS FROM MCU (SERIAL INTERFACE ONLY)
		Outputs are available via an external output latch as enabled by ConfigurACE. These outputs are extracted from the data bus, typically by a 74HCT377 data latch (see INXSEL). The data bus bit number for each signal is defined below.
SELIND	Bus	**Select Indicate.** SELIND output (bit 3) toggles in response to the SEL input ON-to-OFF transition to reflect the directory entry (SELIND ON) or normal (SELIND OFF) operation. If SELIND is ON, the TD input ON-to-OFF transition steps the selected directory to the next entry. The selected entry is indicated by the TDIND, OAIND, and TSTIND outputs as follows: **TDIND / OAIND / TSTIND / Selection** 0 / 0 / 0 / No selection 0 / 0 / 1 / Entry 1 0 / 1 / 0 / Entry 2 . . . 1 / 1 / 1 / Entry 7
TDIND	Bus	**Talk/Data Indicate.** When SELIND is OFF, the TDIND output (bit 0) reflects the state of the off-hook relay. When SELIND is ON, the TDIND output reflects the state of bit 2 of the directory entry selection (see SELIND output).

Table 9. MCU Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
TSTIND	Bus	**Test Indicate.** When SELIND is OFF, the TSTIND output (bit 1) is ON during modem test (see TEST input). When SELIND is ON, the TSTIND output reflects the state of bit 0 of the directory entry selection (see SELIND output).
OAIND	Bus	**Originate/Answer Indicate.** When SELIND is OFF, OAIND output (bit 2) reflect the originate (OFF) or answer (ON) state when connected or toggles to originate (OFF) or answer (ON) in response to the OA input ON-to-OFF transition. When SELIND is ON, the OAIND output reflects the state of bit 1 of the directory entry selection (see SELIND output).
COMIND	Bus	**Compressed Indicate.** COMIND output (bit 4) indicates data compression (MNP 5, V.42 bis) is in effect (high) or is not in effect (low).
RELIND	Bus	**Reliable Connection Indicate.** RELIND output (bit 5) indicates that a reliable connection (MNP, LAPM) is in effect (high) or a non-error-connected connection exists or the modem is off-line (low).
		PARALLEL HOST INTERFACE (PARALLEL INTERFACE ONLY)
		The parallel interface emulates a 16450/16550A UART interface. The parallel interface is compatible with communications software designed to operate with a 16450/16550A interface.
HA0-HA2	IA	**Host Bus Address Lines 0-2.** During a host read or write operation, HA0-HA2 select an internal MCU 16450/16550A-compatible register.
HD0-HD7	IA/OA	**Host Bus Data Lines 0-7.** HD0-HD7 are comprised of eight three-state input/output lines providing bidirectional communication between the host and the MCU. Data, control words, and status information are transferred through HD0-HD7.
$\overline{HCS}$	IA	**Host Bus Chip Select.** $\overline{HCS}$ input low selects the host bus.
$\overline{HRD}$	IA	**Host Bus Read.** $\overline{HRD}$ is an active low, read control input. When $\overline{HCS}$ is low, $\overline{HRD}$ low allows the host to read status information or data from a selected MCU register.
$\overline{HWT}$	IA	**Host Bus Write.** $\overline{HWT}$ is an active low, write control input. When $\overline{HCS}$ is low, $\overline{HWT}$ low allows the host to write data or control words into a selected MCU register.
HINT	OA	**Host Bus Interrupt.** HINT output is set high when the receiver error flag, received data available, transmitter holding register empty, or modem status interrupt has an active high condition. HINT is reset low upon the appropriate interrupt service or master reset operation.
$\overline{TXACK}$	IA	**Host Transmit Acknowledge.** $\overline{TXACK}$ is an active low transmit acknowledge input acknowledging that the DMA controller received the Transmit Ready (TXRDY) data transfer request output.
$\overline{RXACK}$	IA	**Host Receive Acknowledge.** $\overline{RXACK}$ is an active low receive acknowledge input acknowledging that the DMA controller received the Receiver Ready (RXRDY) data transfer request output.
TXRDY	OA	**Transmitter Ready.** TXRDY is an active high transmit ready output in the FIFO mode (FCR0 = 1). When asserted, TXRDY indicates that the TX FIFO is not full, i.e., the TX FIFO can accept data to be transmitted.
RXRDY	OA	**Receiver Ready.** RXRDY is an active high receiver ready output in the FIFO mode (FCR0 = 1). When asserted, RXRDY indicates that the RX FIFO is not empty, i.e., the RX FIFO has received data ready for transfer.
		STOP MODE CONTROL
$\overline{STPMODE}$	IA	**Stop Mode.** $\overline{STPMODE}$ low causes the modem to enter the stop mode immediately after terminating a line connection if connected, terminating any test in process, and allowing any data in the receive buffer to clear. $\overline{STPMODE}$ must be high before the modem can attain normal operation after power turn-on, reset, or wake-up from sleep or stop mode.

Table 10. MDP Signal Definitions

Label	I/O Type	Signal/Definition
		OVERHEAD SIGNALS
XTLI, XTLO	I, O	**Crystal In and Crystal Out.** Connect to an external crystal circuit consisting of a 40.32 MHz crystal, three capacitors, and an inductor, or to a square wave generator/sine wave oscillator.
$\overline{\text{POR}}$	IA	**Power On Reset.** Connect to MCU $\overline{\text{RES}}$.
$\overline{\text{RESET}}$	IA	**Reset.** Connect to MDP $\overline{\text{POR}}$.
+5VD	PWR	**+ 5V Digital Supply.** +5V ± 5%.
+5VA	PWR	**+ 5V Analog Supply.** +5V ± 5%.
DGND	GND	**Digital Ground.** Connect to ground.
AGND	GND	**Analog Ground.** Connect to ground.
VC	MI	**Low Voltage Reference.** Connect to analog ground through 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) in parallel.
VREF	MI	**High Voltage Reference.** Connect to VC through 10 µF (polarized, + terminal to VREF) and 0.1 µF (ceramic) in parallel.
VREG	MI	**Voltage Regulator.** No connect. For compatibility with future modem data pumps, provide a printed circuit board connection to digital ground through 0.1 µF. This capacitor may be installed for this modem but is not required.
		SERIAL INTERFACE (SERIAL INTERFACE ONLY)
$\overline{\text{TXD}}$	IA	**Transmitted Data.** The MDP obtains serial data to be transmitted from the DTE on the TXD input.
$\overline{\text{RXD}}$	OA	**Received Data.** The MDP presents received serial data to the DTE on the RXD output.
$\overline{\text{TDCLK}}$	OA	**Transmit Data Clock.** The modem outputs a synchronous Transmit Data Clock (TDCLK) for USRT timing. The TDCLK frequency is the data rate (±0.01%) with a duty cycle of 50 ±1%.
$\overline{\text{XTCLK}}$	IA	**External Transmit Clock.** In synchronous communication, an external transmit data clock can be connected to the MDP $\overline{\text{XTCLK}}$ input. The clock supplied at $\overline{\text{XTCLK}}$ must exhibit the same characteristics as TDCLK.
$\overline{\text{RDCLK}}$	OA	**Receive Data Clock.** The modem outputs a synchronous Receive Data Clock ($\overline{\text{RDCLK}}$) for USRT timing.
$\overline{\text{RTS}}$	IA	**Request to Send.** Not used; pull up to VCC through 10k Ω.
$\overline{\text{DTR}}$	IA	**Data Terminal Ready.** Not used; pull up to VCC through 10k Ω.
$\overline{\text{CTS}}$	OA	**Clear to Send.** Not used; leave open.
$\overline{\text{DSR}}$	OA	**Data Set Ready.** Not used; leave open.
		INDICATOR SIGNALS (SERIAL INTERFACE ONLY)
$\overline{\text{RLSDIND}}$	OA	**Received Line Signal Detector.** $\overline{\text{RLSDIND}}$ active indicates that energy above the receive level threshold is present on the receiver input, and that the energy is not a training sequence.
		SERIAL/INDICATOR INTERFACE (PARALLEL INTERFACE ONLY)
$\overline{\text{TXD}}$	IA	**Transmitted Data.** Not used; pull up to VCC through 10k Ω.
$\overline{\text{RXD}}$	OA	**Received Data.** Not used; leave open.
$\overline{\text{TDCLK}}$	OA	**Transmit Data Clock.** Not used; leave open.
$\overline{\text{XTCLK}}$	IA	**External Transmit Clock.** Not used; leave open.
$\overline{\text{RDCLK}}$	OA	**Receive Data Clock.** Not used; leave open.
$\overline{\text{RLSDIND}}$	OA	**Received Line Signal Detector.** Not used, leave open.
$\overline{\text{RTS}}$	IA	**Request to Send.** Not used; pull up to VCC through 10k Ω.
$\overline{\text{DTR}}$	IA	**Data Terminal Ready.** Not used; pull up to VCC through 10k Ω.
$\overline{\text{CTS}}$	OA	**Clear to Send.** Not used; leave open.
$\overline{\text{DSR}}$	OA	**Data Set Ready.** Not used; leave open.

Table 10. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
		MCU INTERFACE
D0–D7	IA/OB	**Data Lines.** Connect to the MCU D0-D7, respectively.
RS0–RS4	IA	**Register Select Lines.** Connect to the MCU A0–A4, respectively.
$\overline{CS}$	IA	**Chip Select.** Connect to MCU $\overline{DPSEL}$ output.
$\overline{READ}$	IA	**Read Enable.** Connect to MCU $\overline{READ}$.
$\overline{WRITE}$	IA	**Write Enable.** Connect to MCU $\overline{WRITE}$.
IRQ	OA	**Interrupt Request.** Connect to MCU $\overline{DPIRQ}$.
		LINE INTERFACE
TXA1, TXA2	O(DF)	**Transmit Analog 1 and 2.** The TXA1 and TXA2 outputs are differential outputs 180 degrees out of phase with each other.
RIN	I(DA)	**Receive Analog.** RIN is a single-ended receive data input from the external hybrid in the telephone line interface circuit.
RINGD	IA	**Ring Frequency Detect.** A high-going edge on the RINGD input initiates an internal ring frequency measurement. The RINGD input is typically connected to the output of an optoisolator or equivalent. The idle state (no ringing) output of the ring detect circuit should be low.
CALLID	OD	**Caller ID Relay Control (MDP $\overline{OHRC}$).** Typically, the MDP CALLID output is connected to the normally open Caller ID relay. When the modem detects a Calling Number Delivery (CND) message, the CALLID output is asserted to close the CALLID relay in order to AC couple the CND information to the modem RIN input (without closing the off-hook relay and allowing loop current flow which would indicate an off-hook condition). The MDP CALLID output can each directly drive a +5V reed relay coil with a minimum resistance of 360 ohms and having a must-operate voltage of no greater than 4.0 Vdc. A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor, such as an MPSA20, can be used to drive heavier loads (e.g., electro-mechanical relays).
		SPEAKER INTERFACE
SPKR	O(DF)	**Speaker Analog Output.** The SPKR output reflects the received analog input signal. The SPKR is controlled by the ATMn command. The SPKR output can drive an impedance as low as 300 ohms. In a typical application, the SPKR output is an input to an external LM386 audio power amplifier.
		DIAGNOSTIC SIGNALS Three signals provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified.
EYEXY	OA	**Serial Eye Pattern X/Y Output.** EYEXY is a serial output containing two 15-bit diagnostic words (EYEX and EYEY) for display on the oscilloscope X axis (EYEX) and Y axis (EYEY). EYEX is the first word clocked out; EYEY follows. Each word has 8-bits of significance. Each 15-bit data word is shifted out most significant bit first with the seven most significant bits set to zero. EYEXY is clocked by the rising edge of $\overline{EYECLK}$. This serial digital data must be converted to parallel digital form by a serial-to-parallel converter and then to analog form by two digital-to-analog (D/A) converters.
$\overline{EYECLK}$	OA	**Serial Eye Pattern Clock.** $\overline{EYECLK}$ is a 288 kHz output clock for use by the serial-to-parallel converters. The low-to-high transitions of RDCLK coincide with the low-to-high transitions of $\overline{EYECLK}$. EYECLK, therefore, can be used as a receiver multiplexer clock.
EYESYNC	OA	**Serial Eye Pattern Strobe.** EYESYNC is a strobe for loading the D/A converters.

Table 11. CEP Signal Definitions

Label	I/O Type	Signal Name/Description
		CEP SYSTEM
XTLI, XTLO	IE, OE	**CEP Crystal/Clock In and Crystal Out.** Connects to an external crystal circuit consisting of a 12.9024 MHz crystal and a capacitance network. The CEP XTLI input can be connected to the MCU XTLO output.
$\overline{RES}$	IC	**CEP Reset.** The active low $\overline{RES}$ input resets the CEP logic For serial Interface, the $\overline{RES}$ input is typically connected to MDP $\overline{POR}$, a reset switch, and/or the DTR input as enabled by the HRESETEN output. For parallel Interface, the $\overline{RES}$ input is typically connected to the host bus RESET line through an inverter.
VCC1, VCC2	PWR	**+ 5V Digital Supply.** +5V ± 5%.
GND1-GND8	GND	**Digital Ground.** Connect to ground.
		CEP MEMORY BUS (CMB) BUS INTERFACE
SD0–SD7	IA/OB	**Data Lines.** Connect the RAM D0-D7 lines to the to the SD0-SD7 lines, respectively.
SA0–SA14	OA	**Address Lines.** Connect the RAM A0-A14 lines to the to the SA0-SA14 lines, respectively.
$\overline{SRAMSEL}$	OA	**RAM Chip Select.** Connect the RAM $\overline{CS}$ input to the $\overline{SRAMSEL}$ line.
$\overline{SROMSEL}$	OA	**ROM Chip Select.** Connect the ROM $\overline{CS}$ input to the $\overline{SROMSEL}$ line.
$\overline{SRD}$	OA	**Read Enable.** Connect the RAM $\overline{RD}$ input to the $\overline{SRD}$ line.
$\overline{SWT}$	OA	**Write Enable.** Connect the RAM $\overline{WT}$ input to the $\overline{SWT}$ line.
		MCU EXTERNAL BUS INTERFACE
MCU: D0–D7	IA/OB	**MCU Bus Data Lines.** Connect to the MCU D0-D7, respectively.
MCU: A0–A3	IA	**MCU Bus Address Lines.** Connect to the MCU A0–A3, respectively.
MCU: $\overline{CEPSEL}$	IA	**MCU Bus CEP Chip Select.** Connect to MCU $\overline{CEPSEL}$ output.
MCU: $\overline{RD}$	IA	**MCU Bus Read Enable.** Connect to MCU $\overline{READ}$.
MCU: $\overline{WT}$	IA	**MCU Bus Write Enable.** Connect to MCU $\overline{WRITE}$.

Table 12. Digital Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions[1]
Input High Voltage	V_{IH}				Vdc	
Type IA		2.0	–	V_{CC}		
Type IC		0.7 V_{CC}	–	V_{CC} + 0.3		
Type IE		–	4.0	–		Note 2.
Input Low Voltage	V_{IL}				Vdc	
Type IA and 1C		–0.3		0.8		
Type IE		–	1.0	–		Note 2.
Input Leakage Current	I_{IN}				µAdc	V_{IN} = 0 to V_{CC}
$\overline{RES}$ and PD0-PD7		–	–	±2.5		
XTLI		–	–	±10		
$\overline{NMI}$ and $\overline{TST}$		–	–	±100		
Output High Voltage	V_{OH}				Vdc	
Type OA and OB		2.4	–	–		I_{LOAD} = – 100 µA
Type OD		–	–	V_{CC}		I_{LOAD} = 0 mA
Type OE						Note 3.
Output Low Voltage	V_{OL}				Vdc	
Type OA		–	–	0.4		I_{LOAD} = 1.6 mA
Type OB		–	–	0.4		I_{LOAD} = 0.8 mA
Type OD		–	–	0.75		I_{LOAD} = 15 mA
Three-State (Off) Current	I_{TSI}			±10	µAdc	V_{IN} = 0 V to V_{CC}

Notes:

1. Test Conditions: V_{CC} = 5V ± 5%, T_A = 0°C to 70°C, (unless otherwise stated).
   Output loads: Data bus (D0-D7), address bus (A0-A15), chip selects, $\overline{READ}$, and $\overline{WRITE}$ loads = 70 pF + one TTL load.
   Other = 50 pF + one TTL load.
2. Type IE inputs are centered approximately 2.5 V and swing 1.5 V_{PEAK} in each direction.
3. Type OE outputs provide oscillator feedback when operating with an external crystal.

Table 13. Analog Characteristics

Name	Type	Characteristic	Value
RIN	I (DA)	Input Impedance	> 70K Ω
		Maximum AC Input Voltage	1.1 VP-P**
		Reference Voltage*	+2.5 VDC
TXA1, TXA2	O (DD)	Minimum Load	300 Ω
		Maximum Capacitive Load	0 µF
		Output Impedance	10 Ω
		Maximum AC Output Voltage	2.2 VP-P
		Reference Voltage*	+2.5 VDC
		DC Offset Voltage	± 200 mV
SPKR	O (DF)	Minimum Load	300 Ω
		Maximum Capacitive Load	0 µF
		Output Impedance	10 Ω
		Maximum AC Output Voltage	1.1 VP-P
		Reference Voltage*	+2.5 VDC
		DC Offset Voltage	± 20 mV

* Reference Voltage provided internal to the modem data pump.

** Corresponds to 2.2 VP-P at Tip and Ring.

Table 14. Current and Power Requirements

Mode	Current (I_D) Typical @ 25°C (mA)	Current (I_D) Maximum @ 0°C (mA)	Current (I_D) Maximum @ -40°C[1] (mA)	Power (P_D) Typical @ 25°C (mW)	Power (P_D) Maximum @ 0°C (mW)	Power (P_D) Maximum @ -40°C[1] (mW)	Notes
Configuration without CEP							
MCU - L39							f_{IN} = 14.7456 MHz
Normal mode	34	41	51	170	214	268	
Sleep mode	2.20	2.70	2.80	11.00	14.20	14.70	
Stop mode	0.15	0.20	0.20	0.80	1.10	1.10	
MDP							f_{IN} = 40.32 MHz
Normal mode	180	215	270	900	1135	1420	
Sleep mode	2.00	2.40	3.10	10.00	12.60	16.30	
Total							
Normal mode	214	256	321	1070	1349	1688	
Sleep/Stop mode	4.20	5.10	5.90	21.00	26.80	31.00	
Stop mode	2.15	2.60	3.30	10.80	13.70	17.40	
Configuration with CEP							
MCU - L39							f_{IN} = 12.9024 MHz
Normal mode	32	39	44	160	200	230	
Sleep mode	2.20	2.70	2.80	11.00	14.20	14.70	
Stop mode	0.15	0.20	0.20	0.80	1.10	1.10	
CEP							f_{IN} = 12.9024 MHz
Normal mode	32	39	44	160	200	230	
Sleep mode	2.20	2.70	2.80	11.00	14.20	14.70	
Stop mode	0.15	0.20	0.20	0.80	1.10	1.10	
MDP							f_{IN} = 40.32 MHz
Normal mode	180	215	270	900	1135	1420	
Sleep mode	2.0	2.4	3.1	10.0	12.6	16.3	
Total							
Normal mode	244	293	358	1220	1535	1880	
Sleep mode	6.40	7.80	8.70	32.00	41.00	45.70	
Stop mode	2.30	2.40	3.50	11.60	14.80	18.50	

Notes:
1. Maximum power @ -40°C specified only for extended temperature range parts.
2. Test conditions: VCC = 5.0 VDC for typical values; VCC = 5.25 VDC for maximum values.

Table 15. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to +5VD +0.5	V
Analog Inputs	V_{IN}	-0.3 to +5VA + 0.3	V
Voltage Applied to Outputs in High Z State	V_{HZ}	-0.5 to +5VD + 0.5	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (@ 25°C)	V_{ESD}	±2500	V
Latch-Up Current (@ 25°C)	I_{TRIG}	±200	mA
Operating Temperature Range	T_A		
Commercial		-0 to +70	°C
Extended		-40 to +85	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C

Table 16. Parallel Interface Registers

Register No.	Register Name	Bit No.							
		7	6	5	4	3	2	1	0
7	Scratch Register (SCR)	Scratch Register							
6	Modem Status Register (MSR)	Data Carrier Detect (DCD)	Ring Indicator (RI)	Data Set Ready (DSR)	Clear to Send (CTS)	Delta Data Carrier Detect (DDCD)	Trailing Edge of Ring Indicator (TERI)	Delta Data Set Ready (DDSR)	Delta Clear to Send (DCTS)
5	Line Status Register (LSR)	RX FIFO Error	Transmitter Empty (TEMT)	Transmitter Buffer Register Empty (THRE)	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	Receiver Data Ready (DR)
4	Modem Control Register (MCR)	0	0	0	Local Loopback	Out 2	Out 1	Request to Send (RTS)	Data Terminal Ready (DTR)
3	Line Control Register (LCR)	Divisor Latch Access Bit (DLAB)	Set Break	Stick Parity	Even Parity Select (EPS)	Parity Enable (PEN)	Number of Stop Bits (STB)	Word Length Select Bit 1 (WLS1)	Word Length Select Bit 0 (WLS0)
2	Interrupt Identify Register (IIR) (Read Only)	FIFOs Enabled	FIFOs Enabled	0	0	Pending Interrupt ID Bit 2	Pending Interrupt ID Bit 1	Pending Interrupt ID Bit 0	"0" if Interrupt Pending
2	FIFO Control Register (FCR) (Write Only)	Receiver Trigger MSB	Receiver Trigger LSB	Reserved	Reserved	DMA Mode Select	TX FIFO Reset	RX FIFO Reset	FIFO Enable
1 DLAB = 0	Interrupt Enable Register (IER)	0	0	0	0	Enable Modem Status Interrupt (EDSSI)	Enable Receiver Line Status Interrupt (ELSI)	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Enable Received Data Available Interrupt (ERBFI)
0 DLAB = 0	Transmitter Buffer Register (THR)	Transmitter FIFO Buffer Register (Write Only)							
0 DLAB = 0	Receiver Buffer Register (RBR)	Receiver FIFO Buffer Register (Read Only)							
1 DLAB = 1	Divisor Latch MSB Register (DLM)	Divisor Latch MSB							
0 DLAB = 1	Divisor Latch LSB Register (DLL)	Divisor Latch LSB							