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8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The W78C458 is a high performance single-chip CMOS 8-bit microcontroller and is a derivative of the W78C52 microcontroller family that is functionally compatible with the W78C32, except that it provides an internal 32K byte mask ROM, either 64 KB program/1 MB data memory address or memory-mapped chip select logic, five general I/O ports, and four external interrupts.

In the W78C32, two I/O ports, Port 1 and Port 3, are available for general purpose use (Port 3 also supports alternative functions), and Port 2 and Port 0 are used as the address bus and data bus, respectively. The W78C458 provides two dedicated address ports (AP5, AP6) as 64 KB address output and one address/data port (DP4) as ROM code input and external RAM data input/output to enable Port 0 and Port 2 to be used as general purpose I/O ports. Unlike the W78C32, this product does not require an external latch device for multiplexing low byte addresses. The W78C458 also provides four pins (AP7.0–P7.3) to support either 64 KB program/1 MB data memory space or memory-mapped chip select logic, one parallel I/O port (Port 8) without bit addressing mode, and two additional external interrupts ($\overline{INT2}$, $\overline{INT3}$).

The programming of the W78C458 is fully compatible with that of the W78C32, except that the external data RAM is accessed by the "MOVX @Ri" instruction. Address paging is performed by loading page addresses into the HB (high byte) register, which is not a standard register in the W78C32, before execution of the "MOVX @Ri" instruction.

FEATURES

- 8-bit CMOS microcontroller
- Fully static design
- DC to 40 MHz operation
- 32 KB on-chip mask ROM
- 256 byte on-chip scratchpad RAM
- Either 64 KB program/1 MB data memory address space or 4 memory-mapped chip select pins
- 8-bit data/address port
- Two 8-bit and one 4-bit (optional) address ports
- Five 8-bit bidirectional I/O ports:
  - Four 8-bit bit-addressable I/O ports and one 8-bit parallel I/O port
- Eight-source, two-level interrupt capability
- Three 16-bit timer/counters
- Four external interrupts
- One full duplex serial channel
- Built-in power management
  - Idle mode
  - Power-down mode
- Packages:
  - 84-pin PLCC: W78C458P-16/24/33/40
  - 100-pin PQFP: W78C458F-16/24/33/40

Publication Release Date: October 1996
Revision A4

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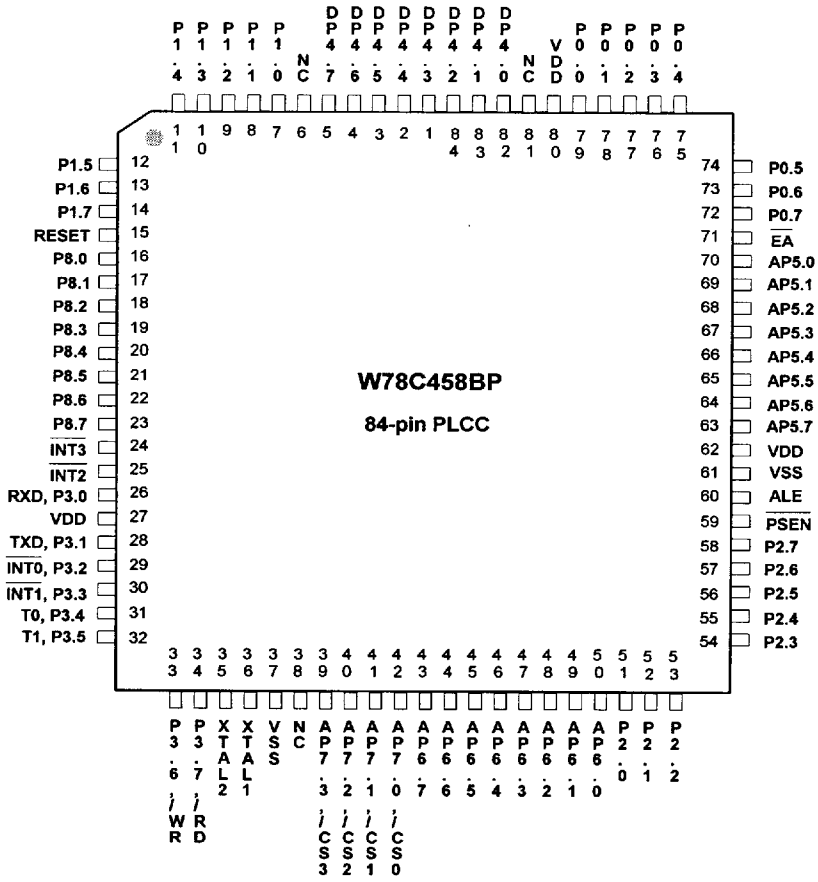
PIN CONFIGURATIONS



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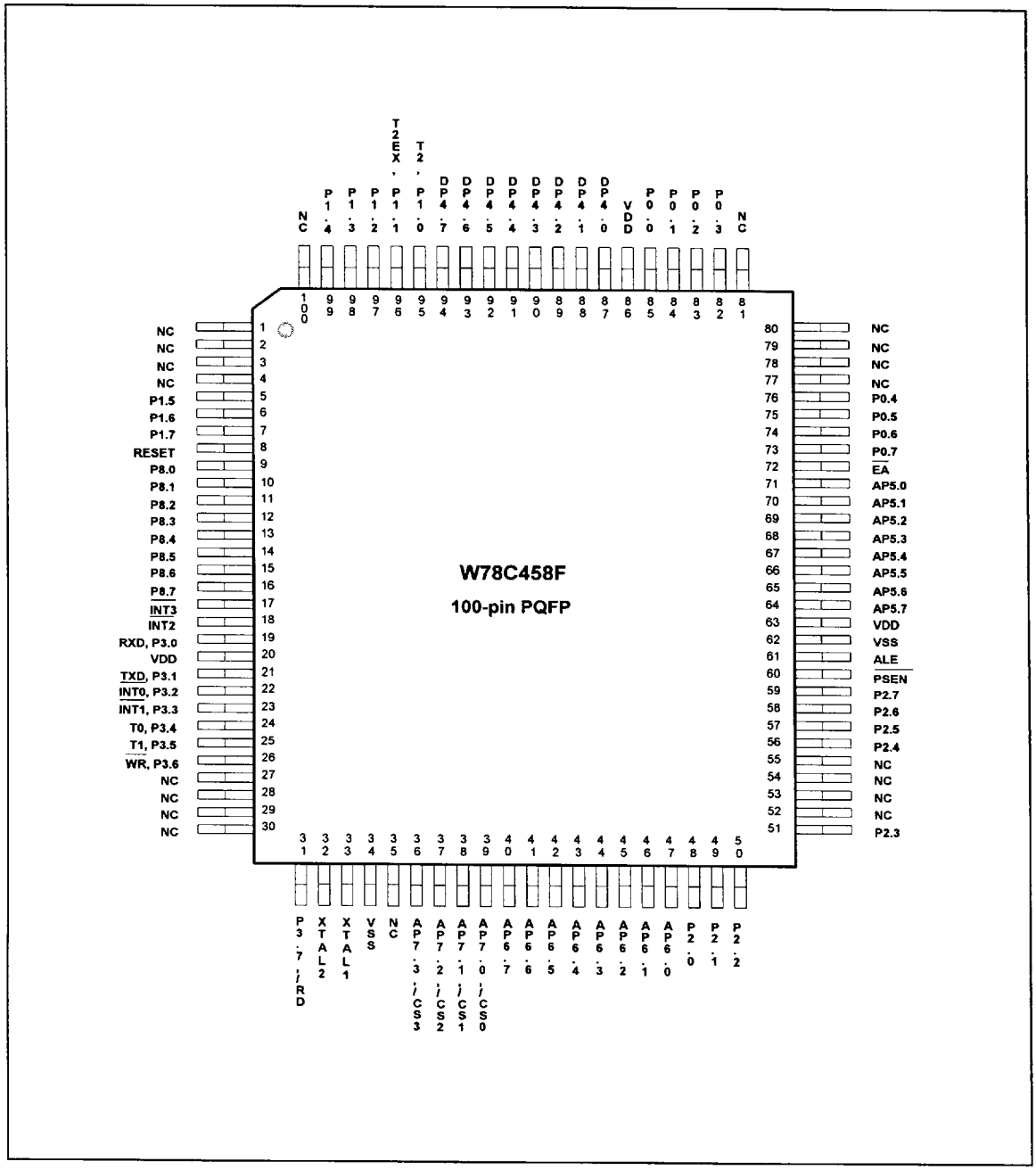
Pin Configurations, continued



PIN DESCRIPTION

P0.0–P0.7 I/O Port 0

These pins function the same as those in the W78C32, except that a multiplexed address/data bus is not provided during accesses to external memory.

P1.0–P1.7 I/O Port 1

Functions are the same as in the W78C32.

P2.0–P2.7 I/O Port 2

Functions are the same as in the W78C32, except that an upper address bus is not provided during accesses to external memory.

P3.0–P3.7 I/O Port 3

Functions are the same as in the W78C32.

DP4.0–DP4.7 Data/Address Bus

DP4 provides a multiplexed low-byte address/data during access to external memory.

AP5.0–AP5.7 Address Bus

AP5 outputs the <7:0> address of the external ROM multiplexed with the <7:0> address of the external data RAM.

AP6.0–AP6.7 Address Bus

AP6 outputs the <15:8> address of the external ROM multiplexed with the <15:8> address of the external data RAM. During the execution of "MOVX @Ri," the output of AP6 comes from the HB register, which is the page register for the high byte address, and its address is 0A1H.

AP7.0–AP7.3 Address Bus/Chip Select Pins

Setting bit 7 of EPMA (Extended Program Memory Address) register determines the functions of port 7. When this bit is "0" (default value), AP7 outputs the <19:16> address of the external memory from bits<3:0> of EPMA register during the execution of "MOVC A, @A+DPTR" to read the external ROM data or the execution of "MOVX dest, src" to access the external RAM data. At all other times, AP7<3:0> will output 0H.

When this bit is "1," AP7<3:0> (CS3-0) are the chip select pins to support memory-mapped peripheral device select, and only one of them is active low at any one time. These pins are decoded by AP6<7:6>. For details, see the table below.

AP6.7	AP6.6	DESCRIPTION
0	0	AP70: low; others: high
0	1	AP71: low; others: high
1	0	AP72: low; others: high
1	1	AP73: low; others: high

P8.0–P8.7 I/O Port

Functions are the same as those of Port 1 in the W78C31, except that they are mapped by the P8 register and not bit-addressable. The P8 register is not a standard register in the W78C32. Its address is at 0A6H.

INT2, INT3External Interrupt, Input

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Functions are similar to those of external $\overline{INT0}$, $\overline{INT1}$ in the W78C32, except that the functions/status of these interrupts are determined by the bits in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the W78C32. Its address is at 0C0H. For details, see the Functional Description.

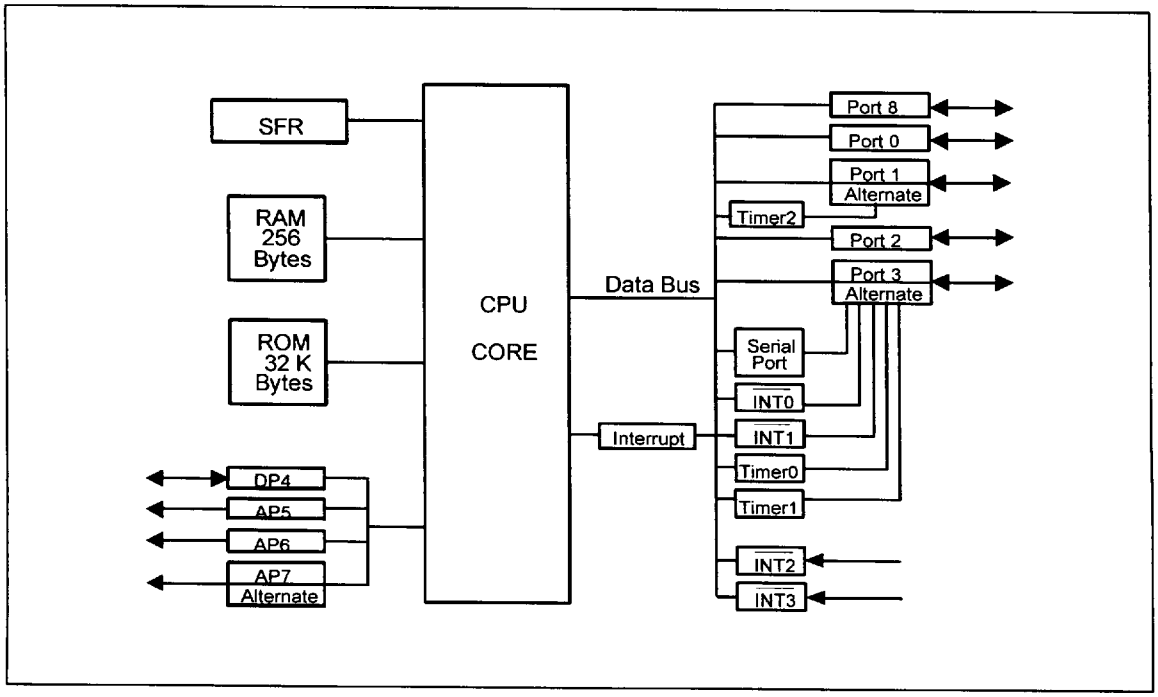
$\overline{EA}$ External Address, Input

Functions same as W78C32.

RST, XTAL1, XTAL2, $\overline{PSEN}$, ALE

Functions same as W78C32.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The W78C458 is a functional extension of the W78C52 microcontroller. It contains a 32K × 8 ROM, 256 × 8 RAM, 64 KB program/1 MB/data memory address or memory-mapped chip select logic, two 8-bit address ports, one 8-bit address/data port, five general I/O ports, four external interrupts, three timers/counters, and one serial port.

Dedicated Data and Address Port

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The W78C458 provides four general-purpose I/O ports for W78C32 applications; the address and data bus are separated from Port 0 and Port 2 so that these ports can be used as general-purpose I/O ports. In this product, DP4 is the data bus for external ROM and RAM, AP5<7:0> is the low byte address, AP6<7:0> is the high byte address, $\overline{PSEN}$ enables the external ROM to DP4, and P3.6 ($\overline{WR}$) and P3.7 ($\overline{RD}$) are the write/read control signals for the external RAM. An external latch for multiplexing the low byte address is no longer needed in this product. The W78C458 uses AP5 and AP6 to support 64 KB external program memory and 64 KB external data memory, just as a standard W78C32 does.

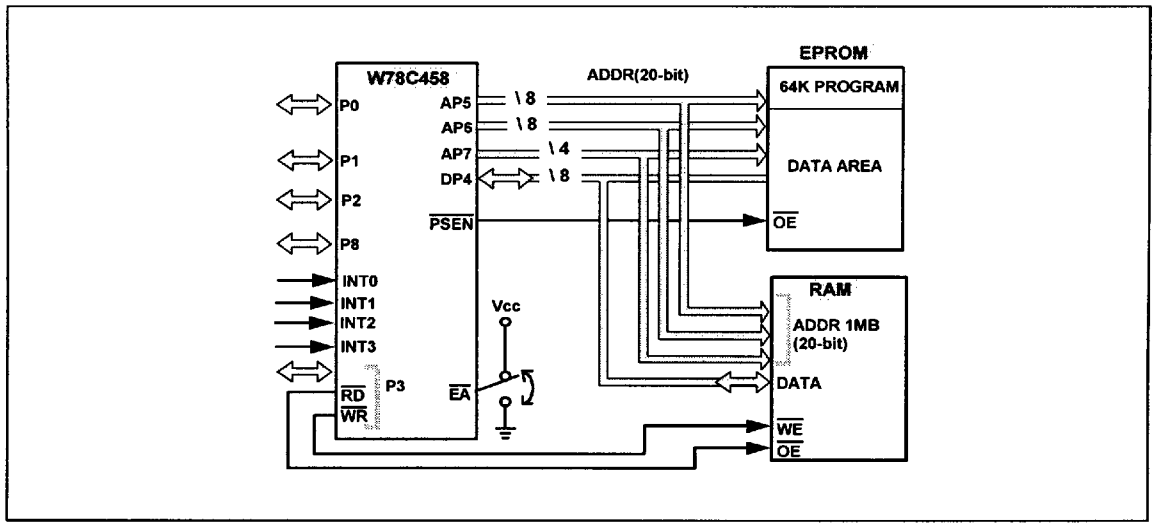
The W78C458 provides four pins, AP7.3–AP7.0 (CS3–CS0), to support either 64 KB program/1 MB data memory space or memory-mapped chip select logic. Bit 7 of the EPMA (Extended Program Memory Address) register, which is described in Table 1, determines the functions of these pins.

When this bit is "0" (default value), AP7<3:0> supports external program/data memory addresses up to 64 KB/1 MB for applications which need additional external program/data memory to store large amounts of data.

Although there is 1M bytes memory space, instructions stored here can not be run at full range of this area except the first 64 Kbytes. It is owing to the fact that during the instruction fetch cycle, AP7<3:0> always output 0s to address lines A19-A16. This limits the program code to store at address 0-0FFFFH (64K). The rest of the area (10000H–FFFFFH) can be treated as ROM data storage which can be read by "MOVC A, @A+DPTR" instruction.

During the execution of "MOVC A, @A+DPTR" to read the external ROM data or the execution of "MOVX dest, src" to access the external RAM data, AP7<3:0> outputs address <19:16> from bits <3:0> of the EPMA (Extended Program Memory Address) register. At other times, AP7<3:0> always outputs 0H to ensure the instruction fetch is within the 64K program memory address. Different banks can be selected by modifying the content of the EPMA register before the execution of "MOVC A, @A+DPTR." or "MOVX dest, src."

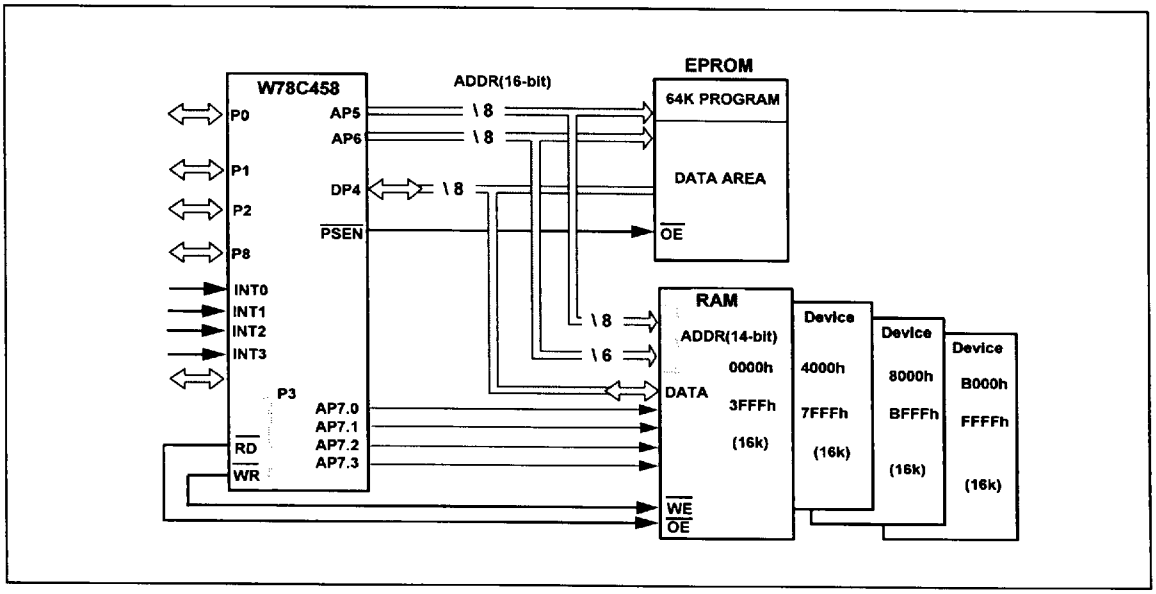
(A) EPMA.7 = 0



When the EPMA.7 is "1," AP7<3:0> are the output pins to support memory-mapped peripheral chip select logic, which eliminates the need for glue logic. These pins are decoded by AP6<7:6>. Only one of them is active low at any time. That is, they are active individually with 16K address resolution. For

example, CS0 is active low in the address range from 0000H to 3FFFH, CS1 is active low in the address range from 4000H to 7FFFH, and so forth.

(B) EPMA.7 = 1



The EPMA register is a nonstandard 8-bit SFR at address 0A2H in the standard W78C32. To read/write the EPMA register, one can use the "MOV direct" instruction or "read-modify-write" instructions. Bits <6:4> of the EPMA register are reserved bits, and their output values are 111B if they are read. The content of EPMA is 70H after RESET. The EPMA register does not support bit-addressable instructions.

BIT	NAME	FUNCTION
7	EPMA7	EPMA7 = 0: 64 KB program/1 MB data memory space mode EPMA7 = 1: memory-mapped chip select mode
6	EPMA6	Reserved
5	EPMA5	Reserved
4	EPMA4	Reserved
3	EPMA3	Value of AP7.3
2	EPMA2	Value of AP7.2
1	EPMA1	Value of AP7.1
0	EPMA0	Value of AP7.0

Table 1: The Functional Description of the EPMA

Additional I/O Port

The W78C458 provides one parallel I/O port, Port 8. Its function is the same as of Port 1 in the W78C31, except that it is mapped by the P8 register and is not bit-addressable. The P8 register is not a standard register in the standard W78C32. Its address is at 0A6H. To read/write the P8 register, one can use the "MOV direct" instruction or "read-modify-write" instructions.

Additional External Interrupt

The W78C458 provides two additional external interrupts, $\overline{INT2}$ and $\overline{INT3}$, whose functions are similar to those of external interrupt 0 and 1 in the W78C32. The functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. For details, see Table 2. The XICON register is bit-addressable but is not a standard register in the W78C32. Its address is at 0C0H. To set/clear a bit of the XICON register, one can use the "SETB(/CLR) bit" instruction. For example, "SETB 0C2H" sets the EX2 bit of XICON. The interrupt vector addresses and the priority polling sequence within the same level are shown in Table 3.

BIT	ADDR.	NAME	FUNCTION
7	0C7H	PX3	High/low priority level for $\overline{INT3}$ is specified when this bit is set/cleared by software.
6	0C6H	EX3	Enable/disable interrupt from $\overline{INT3}$ when this bit is set/cleared by software.
5	0C5H	IE3	If IT3 is "1," IE3 is set/cleared automatically by hardware when interrupt is detected/serviced.
4	0C4H	IT3	$\overline{INT3}$ is falling-edge/low-level triggered when this bit is set/cleared by software.
3	0C3H	PX2	High/low priority level for $\overline{INT2}$ is specified when this bit is set/cleared by software.
2	0C2H	EX2	Enable/disable interrupt from $\overline{INT2}$ when this bit is set/cleared by software.
1	0C1H	IE2	If IT2 is "1," IE2 is set/cleared automatically by hardware when interrupt is detected/serviced.
0	0C0H	IT2	$\overline{INT2}$ is falling-edge/low-level triggered when this bit is set/cleared by software.

Table 2: Functions of XICON Register

INTERRUPT SOURCE	VECTOR ADDRESS	PRIORITY SEQUENCE
External Interrupt 0	03H	0 (highest)
Timer/Counter 0	0BH	1
External Interrupt 1	13H	2
Timer/Counter 1	1BH	3
Serial Port	23H	4
Timer/Counter 2	2BH	5
External Interrupt 2	33H	6
External Interrupt 3	3BH	7 (lowest)

Table 3: Priority of Interrupts

Newly Defined Special Function Registers

The W78C458 uses four newly defined special function registers, which are described in Table 4. To read/write the registers, one can use the "MOV direct" or "read-modify-write" instructions.

NAME	ADDR	OBJECT	VALUE AFTER RESET
HB	A1	During the execution of "MOVX @Ri," the content of HB is output to AP6.	00H
EPMA	A2	EPMA.7 determines the functions of AP7. EPMA.3–EPMA.0 determine the values of P7<3:0> when EPMA.7 is "0."	70H
P8	A6	The content of P8 is output to port 8.	0FFH
XICON	C0	The bits of XICON determine/show the functions/status of $\overline{INT2}$–$\overline{INT3}$.	00H

Table 4: New Special Function Registers of the W78C458

Note: The instructions used to access these nonstandard registers may cause assembling errors with respect to the 2500 A. D. assembler, but these errors can be ignored by adding directive ".RAMCHK OFF" ahead these instructions.

Power Reduction Function

The W78C458 supports power reduction just as the W78C32, does. The following table shows the status of the external pins during the idle and power-down modes.

FUNCTION	ALE	$\overline{PSEN}$	P0–P3, P8	DP4	AP5 AP6	AP7
Idle	1	1	Port Data	Floating	Address	Note
Power Down	0	0	Port Data	Floating	Address	Note

Note: Either 0 or decoded value by AP6<7:6>, depending on the value of EPMA.7.

Programming Difference

The programming of the W78C458 is fully compatible with that of the W78C32, except that the external data RAM is accessed by a "MOVX @Ri" instruction. To support address paging, there is an additional 8-bit SFR "HB" (high byte), which is a nonstandard register, at address 0A1H. During the execution of "MOVX @Ri," the contents of HB are output to AP6. The page address is modified by loading the HB register with a new value before execution of the "MOVX @Ri" instruction. To read/write the HB register, one can use the "MOV direct" instruction or "read-modify-write" instructions. The HB register does not support bit-addressable instructions.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_{OPR}	0	70	°C
Storage Temperature	T_{STG}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

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DC CHARACTERISTICS

V_{DD}–V_{SS} = 5V ±10%, T_A = 25° C, F_{OSC} = 20 MHz, unless otherwise specified.

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oper. Voltage	V_{DD}	-	4.5	5	5.5	V
Oper. Current	I_{DD}	*No load	-	-	30	mA
Idle Current	I_{IDLE}	Program idle mode	-	-	7	mA
Pwdn Current	I_{PWDN}	Program power-down mode	-	-	20	µA
Input Leakage current	I_{LK1}	$\overline{INT2}$, $\overline{INT3}$ Internal pull-high Notes 1, 2	-400	-	+10	µA
Input Leakage Current	I_{LK2}	RESET Internal pull-low Notes 1, 2	-10	-	+300	µA
Input Leakage Current	I_{LK3}	$\overline{EA}$, Port 0, DP4 Note 1	-10	-	+10	µA
Input Leakage Current	I_{LK4}	P1, P2, P3, P8 Note 1	-50	-	+10	µA
Output Low Voltage	V_{OL1}	I_{OL1} = 2 mA (Port 1, 2, 3, 8)	-	-	0.45	V
Output High Voltage	V_{OH1}	I_{OH1} = -100 µA (Port 1, 2, 3, 8)	2.4	-	-	V
Output Low Voltage	V_{OL2}	I_{OL2} = 4 mA Note 3 (ALE, $\overline{PSEN}$, P0, DP4)	-	-	0.45	V
Output High Voltage	V_{OH2}	I_{OH2} = -400 µA Note 3 (ALE, $\overline{PSEN}$, P0, DP4)	2.4	-	-	V
Output Low Voltage	V_{OL3}	I_{OL2} = 2 mA (AP5, AP6, AP7)	-	-	0.45	V
Output High Voltage	V_{OH3}	I_{OH2} = -100 µA (AP5, AP6, AP7)	2.4	-	-	V
Input Voltage	I_{ILT}	V_{DD} = 5V ±10%	0	-	0.8	V
Input Voltage	I_{IHT}	V_{DD} = 5V ±10%	2.4	-	Note 4	V
Input Voltage	I_{ILC}	V_{DD} = 5V ±10%, XTAL1 Note 5	0	-	0.8	V
Input Voltage	I_{IHC}	V_{DD} = 5V ±10%, XTAL1 Note 5	3.5	-	Note 4	V
Input Voltage	I_{ILR}	V_{DD} = 5V ±10%, RESET Note 5	0	-	0.8	V
Input Voltage	I_{IHR}	V_{DD} = 5V ±10%, RESET Note 5	2.4	-	Note 4	V

Notes:

1. 0 < V_{IN} < V_{DD}, for $\overline{INT2}$, $\overline{INT3}$, RESET, $\overline{EA}$, Port 0 and DP4 inputs in leakage.
2. Using an internal pull low/high resistor (approx. 30K).
3. ALE, $\overline{PSEN}$, P0 and DP4 in external program or data access mode.
4. The maximum input voltage is V_{DD} +0.2V.
5. XTAL1 is a CMOS input and RESET is a Schmitt trigger input.

AC CHARACTERISTICS

AC specifications are a function of the particular process used to manufacture the product, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a ±20 nS variation.

Clock Input Waveform

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Operating Speed	FOP	0	-	40	MHz	1
Clock Period	TCP	25	-	-	nS	2
Clock High	TCH	10	-	-	nS	3
Clock Low	TCL	10	-	-	nS	3

Notes:

1. The clock may be stopped indefinitely in either state.
2. The TCP specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Valid to $\overline{PSEN}$ Low	TAPL	2 TCP	-	-	nS
$\overline{PSEN}$ Low to Data Valid	TPDV	-	-	2 TCP	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Memory Read/Write Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Valid to $\overline{RD}$ Low	TARL	4 TCP	-	4 TCP +Δ	nS
$\overline{RD}$ Low to Data Valid	TRDV	-	-	4 TCP	nS
Data Hold after $\overline{RD}$ High	TRDQ	0	-	2 TCP	nS
$\overline{RD}$ Pulse Width	TRS	6 TCP -Δ	6 TCP	-	nS
Address Valid to $\overline{WR}$ Low	TAWL	4 TCP	-	4 TCP +Δ	nS
Data Valid to $\overline{WR}$ Low	TDWL	1 TCP	-	-	nS
Data Hold after $\overline{WR}$ High	TWDQ	1 TCP	-	-	nS
$\overline{WR}$ Pulse Width	TWS	6 TCP -Δ	6 TCP	-	nS

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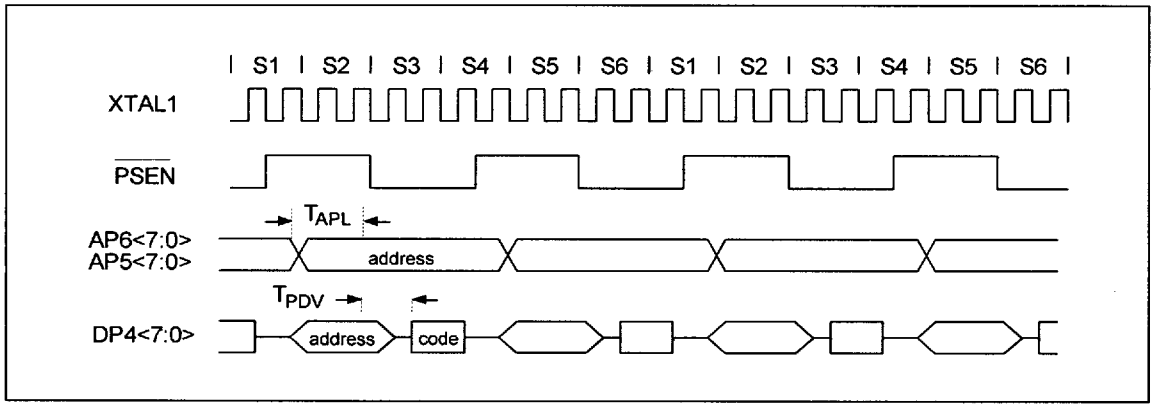
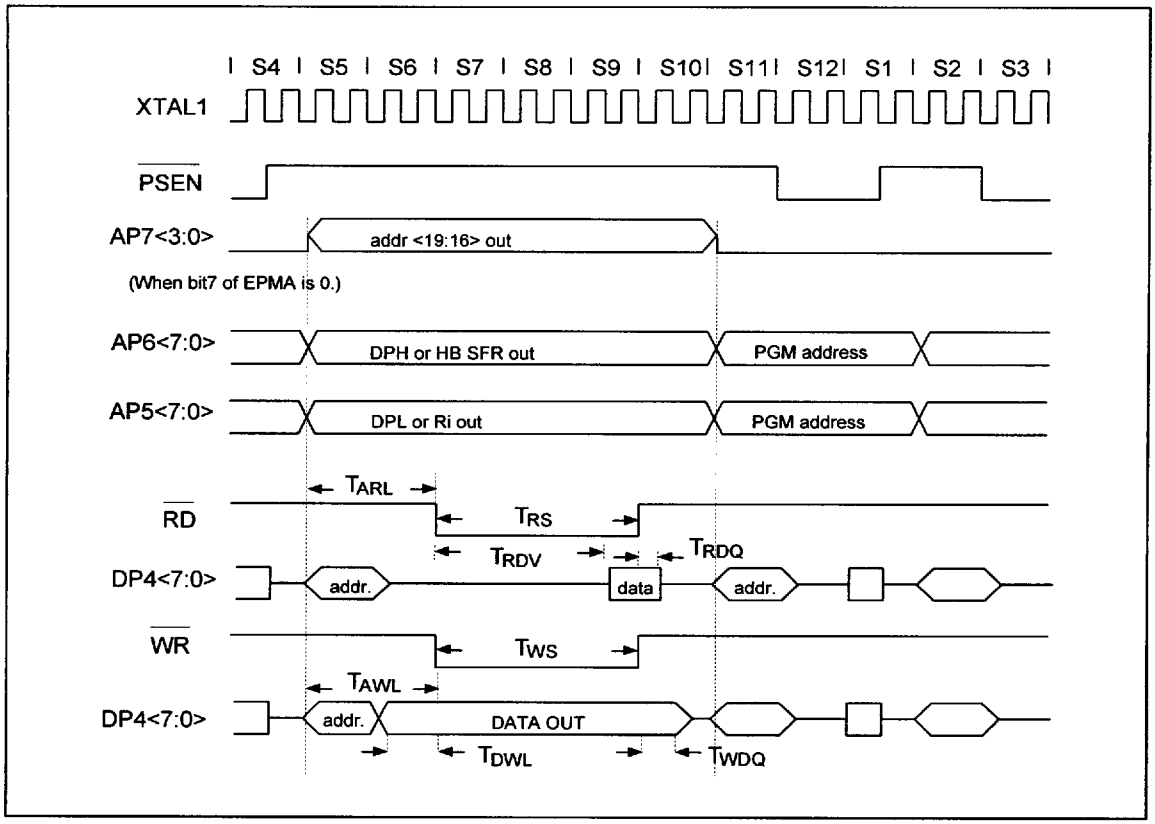
TIMING WAVEFORMS

Program Fetch Cycle



Data Memory Read/Write Cycle



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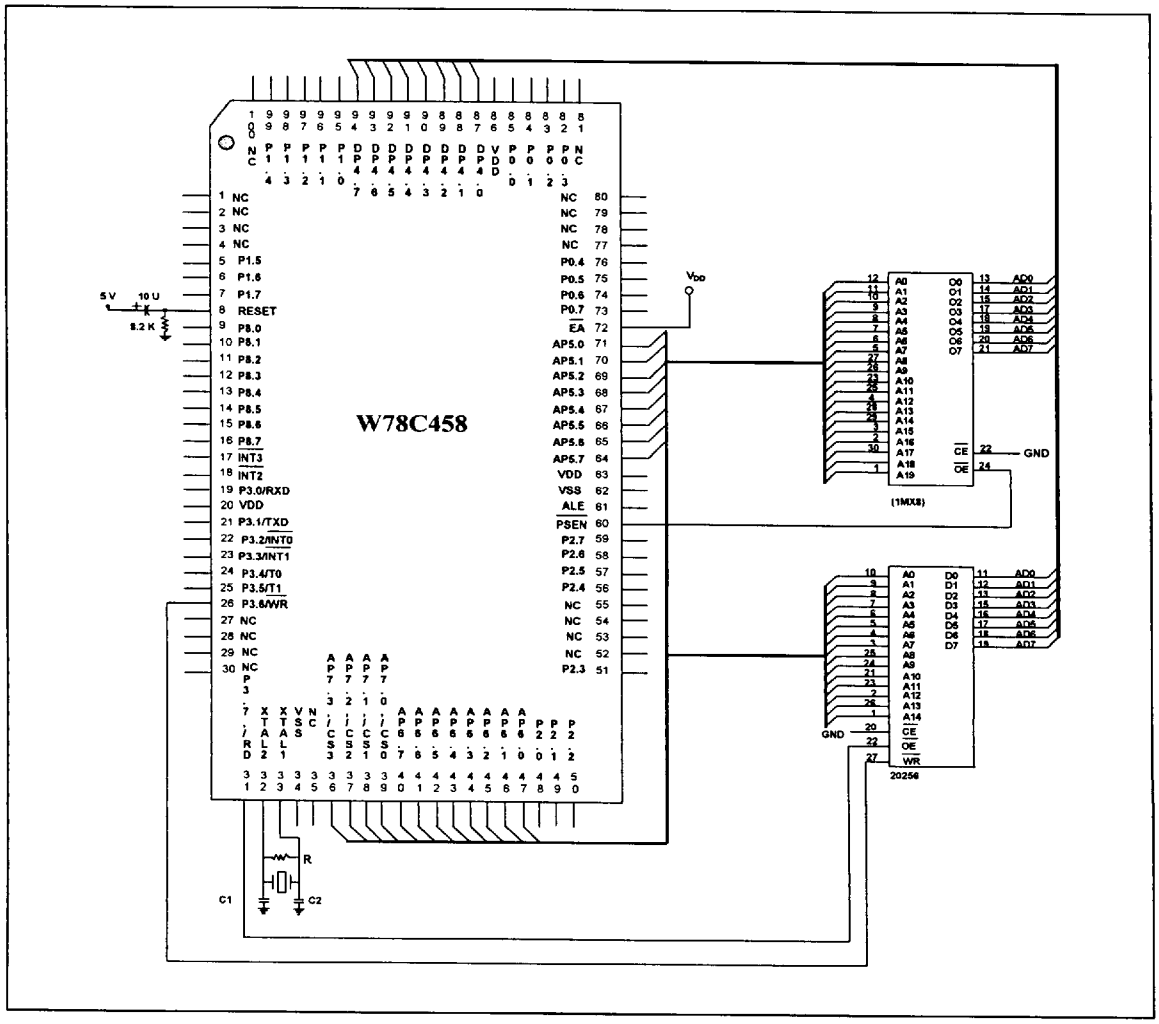
TYPICAL APPLICATION CIRCUIT



CRYSTAL	C1	C2	R
16 MHz	30P	30P	—
24 MHz	15P	15P	62K
33 MHz	15P	15P	20K
40 MHz	5P	5P	3.3K

Above table shows the reference values for crystal applications.

Notes:

1. For C1, C2, R components refer to Figure A and B.
2. For applications above 35 MHz, it is recommended that the crystals be replaced with oscillators.

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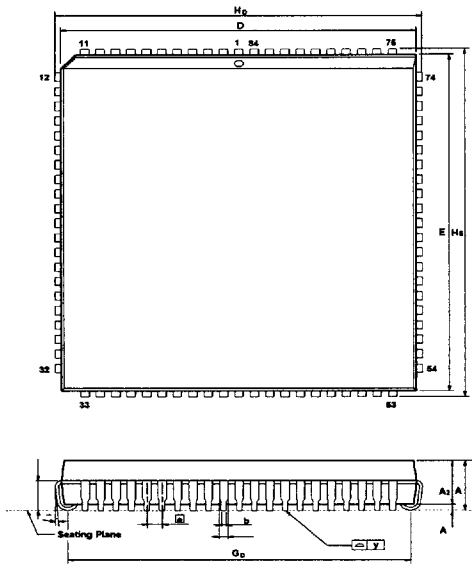
PACKAGE DIMENSIONS

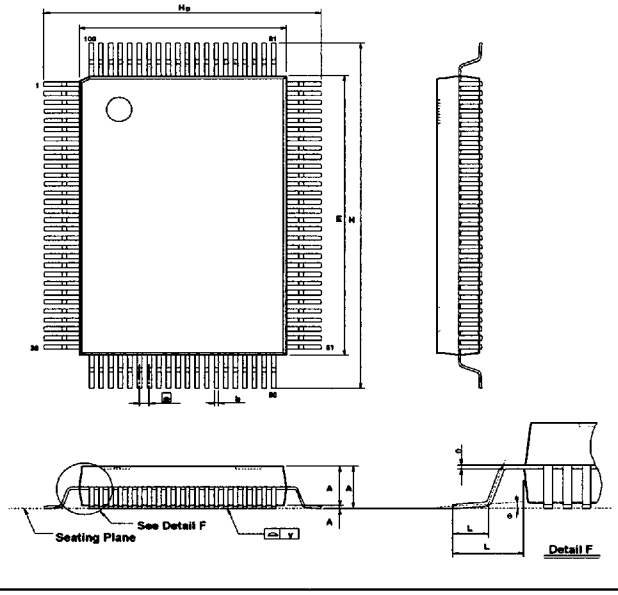
84-pin PLCC



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.70
A_1	0.020	—	—	0.51	—	—
A_2	0.143	0.148	0.153	3.63	3.76	3.89
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.006	0.008	0.012	0.15	0.20	0.30
D	1.148	1.153	1.158	29.17	29.29	29.41
E	1.148	1.153	1.158	29.17	29.29	29.41
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	1.095	1.115	1.135	27.81	28.32	28.83
G_E	1.095	1.115	1.135	27.81	28.32	28.83
H_D	1.180	1.190	1.200	29.98	30.23	30.48
H_E	1.180	1.190	1.200	29.98	30.23	30.48
L	0.090	0.100	0.110	2.29	2.54	2.79
y	—	—	0.004	—	—	0.10
θ	0	—	10	0	—	10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

100-pin QFP



	Dimension in inches			Dimension in mm		
	—	—	0.130	—	—	3.30
A_1	0.004	—	—	0.10	—	—
A_2	0.107	0.112			2.845	
		0.012	0.016	0.254	0.305	0.407
	0.004		0.010	0.101	0.152	0.254
	0.546					
E		0.787	0.792	19.87	20.00	20.13
□	0.020	0.026		0.496	0.65	
D				18.49		19.10
H_E	0.964	0.976	0.988		24.80	25.10
L	0.039	0.047	0.055	0.991	1.194	
L_1	0.067		0.103	2.21	2.413	2.616
y	—	—	0.004	—	—	
θ	°	—	12°	0°	—	°

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.