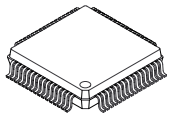
Product Preview

Twisted Pair Interface

for 100Base-TX Local Area Networks

MC68833



FA SUFFIX
TQFP PACKAGE
CASE 931–02

Overview

100Base–TX is a LAN standard under IEEE auspices. The twisted pair cable connecting two stations can be up to 100 meters in length. Users are encouraged to refer to the pertinent IEEE 802.3 standard documents for further information.

Introduction

The MC68833 Twisted Pair Interface Chip (TPIC) is a transceiver capable of transmitting and receiving MLT3 encoded datastreams, as well as handling clock and data recovery. The TPIC implements the lower portion of the physical layer (PHY) functions of the Fast Ethernet standard and, with its Auto Negotiation Fast Link Pulse “Pass Through” capability, is well suited for 100Base–TX applications. It performs a five–bit parallel to serial conversion during transmission, as well as a five–bit serial to parallel conversion during reception.

MC68833 Features

- Supports Twisted Pair Media
- Supports MLT–3 Line Code
- Selectable Auto Negotiation mode has FLP and NLP “Pass–Through” Capability
- Controlled Twisted Pair Output Transition Times May Eliminate Need for Transmit Filter
- Adaptive Receive Equalization supports TP line lengths of 0 to 100 meters
- TP Receiver Includes Circuitry Which Enables Error Free Reception of Data Distorted with Base Line Wander
- Twisted Pair (TP) Transceiver Complies with ANSI X3T9.5 TP–PMD Standard and the IEEE 802.3 100Base–TX Ethernet Draft Standard
- Meets Jitter Requirements of ANSI X3T9.5 TP–PMD
- Physical Layer Support for Fast Ethernet
- Digital Phase–Locked Loop (DPLL) Provides Run Length Immunity
- Transmit Off Capability for True Quiet Line State
- Uses a 25 Mhz External Frequency Reference
- Converts Received Serial Bit Stream to Five–Bit Parallel Form
- Recovers 125 Mhz Clock from Incoming Serial MLT3 Data Stream
- Generates 25 Mhz Receive Clock
- Small Number of Passive External Components Required
- Selectable Low Power Mode
- Loop Back Capability
- Single +5V Power Supply
- Utilizes 0.8uM BiCMOS Technology
- 10mM X 10mM, 64 Pin, TQFP Package (Power Enhanced Leadframe Package)

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Functional Description

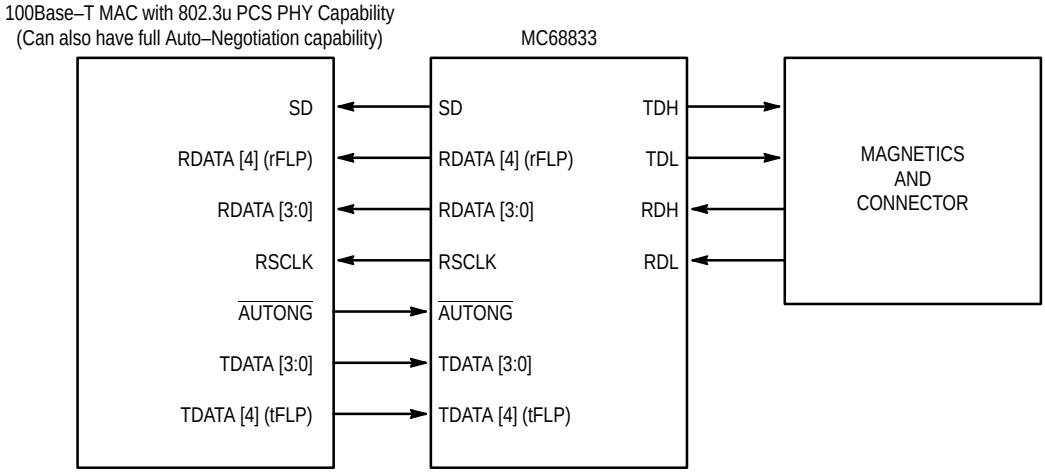


Figure 1. Simplified Block Diagram for Twisted Pair Applications of the MC68833 TPIC

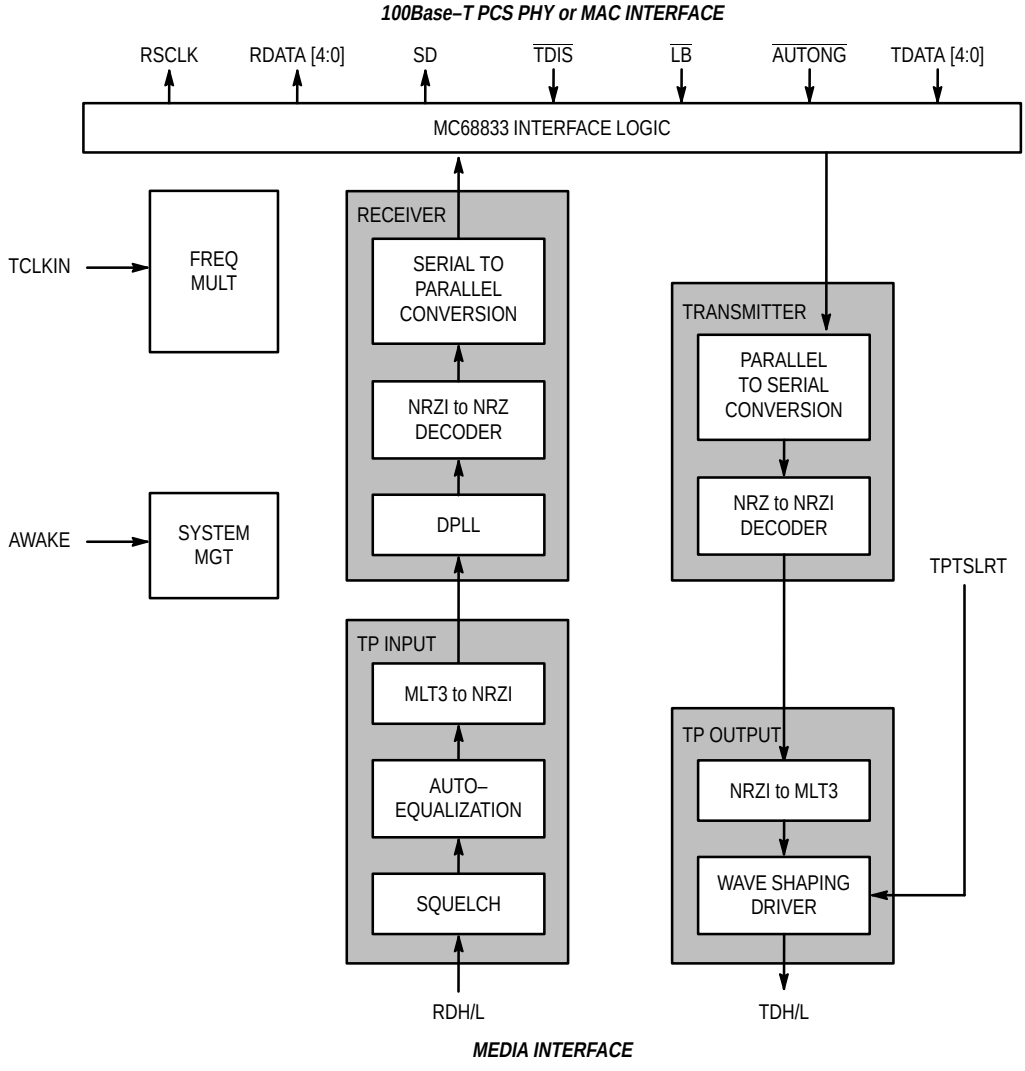


Figure 2. MC68833 Simplified Block Diagram

Pin Assignments

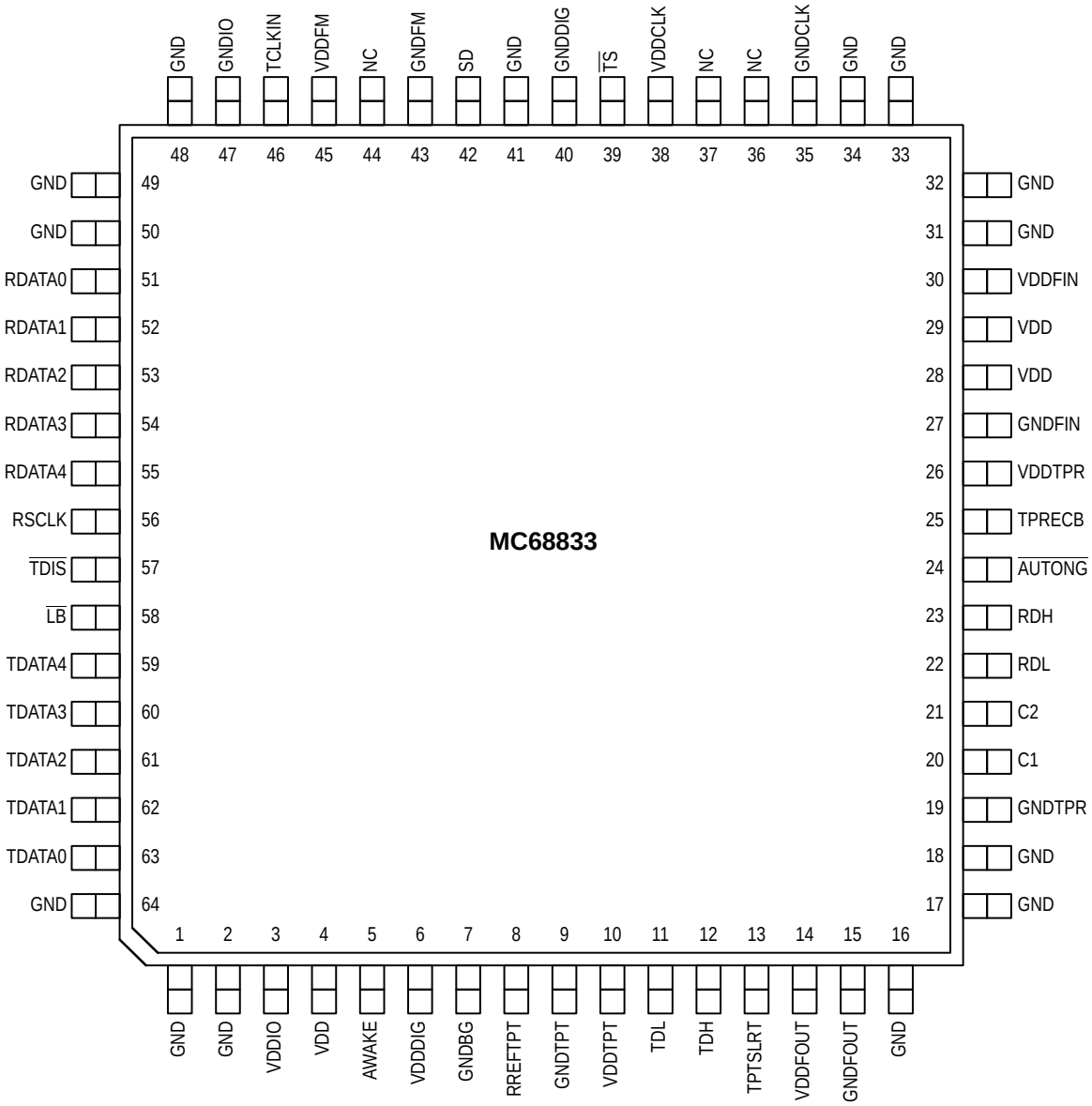


Figure 3. MC68833 Pinout: 64–Lead TQFP Package (Top View)

Pin Function Descriptions

Table 1. Media Interface Pins

Pin No.	Pin Name	Pin Type	Pin Description
11 12	TDL TDH	O	Differential Transmitter Outputs MLT–3 coding is used. MLT–3 data contains three logic states: +1, 0, and –1. The +1 logic state is produced when the TDH output is activated while the TDL output is off. The –1 logic state is produced when the TDL output is activated while the TDH output is off. The 0 logic state is produced when both outputs are active.
22 23	RDL RDH	I	Differential Receiver Inputs The receiver inputs are connected to a receiver which features adaptive equalization and squelch capabilities. The squelch capability blocks signals which do not meet a preset minimum level specification.

Table 2. Mode Select Pins

Pin No.	Pin Name	Pin Type	Pin Description
5	AWAKE	I TTL	Awake Input When the AWAKE input is set to the high logic state, the MC68833 operates in its normal mode. The AWAKE input may be driven to the low logic state in which the MC68833 operates in a low power “snooze” mode. In this low power mode the system clocks continue to operate.
13	TPTSLRT	I TTL	Twisted Pair Transmitter Slew Rate Select When the TPTSLRT input is set to the high logic state, the output slew rate will be at about 2.5ns/volt. When the TPTSLRT is set to the low logic state, the slew rate will be at about 4ns/volt.[1] In the low slew rate mode, it may be unnecessary to utilize an external transmit filter.
24	$\overline{\text{AUTONG}}$	I TTL	Auto Negotiation Mode Enable For Fast Ethernet applications which utilize the Auto Negotiation LAN autodetection scheme, this pin must be driven to the low logic state. For those applications which do not utilize the Auto Negotiation LAN autodetection scheme this pin must be driven to the high logic state.
39	$\overline{\text{TS}}$	I TTL	Three State Enable When low, this input causes all the RDATA outputs and the RSCLK and SD outputs to go to the high impedance state.

1 Specification established by design and laboratory characterization.

Table 3. PCS PHY or MAC Interface Pins

Pin No.	Pin Name	Pin Type	Pin Description
42	SD	O TTL	Signal Detect Output When the $\overline{\text{LB}}$ input is low, the SD output is high. When the $\overline{\text{LB}}$ input is high, a high logic state, on the SD output indicates the presence of a received Twisted Pair data signal with an amplitude exceeding a preset squelch threshold.
51 52 53 54 55	RDATA0 RDATA1 RDATA2 RDATA3 RDATA4	O TTL	Receive Data Bus Outputs These outputs deliver recovered receive data to the MAC. The data appearing at each output may change at a 25 Mbps rate. RDATA4 is received from the media first. Also, when $\overline{\text{AUTONG}}$ is low, the Fast Link Pulses (FLP) or Normal Link Pulses (NLP) received from the media will be present on RDATA4.
56	RSCLK	O TTL	Recovered Symbol Clock Output This clock signal is used to latch data received on RDATAx. The frequency of this signal is nominally 25 MHz.
57	$\overline{\text{TDIS}}$	I TTL	Transmit Output Disable Input When the $\overline{\text{TDIS}}$ input is low the Transmitter Differential Outputs, TDH and TDL are disabled.

Table 3. Elasticity Link Manager (MAC) Interface Pins (continued)

Pin No.	Pin Name	Pin Type	Pin Description
58	$\overline{LB}$	I TTL	Loopback Enable When low, this input enables Transmitter–Receiver loopback capability, which causes data appearing at the Transmit Data Bus Inputs (TDATAx) to be fed to the Receive Data Bus Outputs (RDATAx) and the Signal Detect output (SD) to be forced high. While in the Loopback mode, the MAC interface will not receive any data from the RDL and RDH inputs, however, the $\overline{TDIS}$ input must be forced low to prevent transmit data from appearing on the TDL and TDH outputs.
59 60 61 62 63	TDATA4 TDATA3 TDATA2 TDATA1 TDATA0	I TTL	Transmit Data Bus Inputs These inputs accept data from the MC68833's MAC interface which is to be transmitted to the attached media. The data appearing at each input may change at a 25 Mbps rate. TDATA4 is transmitted on the media first. Also, when $\overline{AUTONG}$ is low, the Fast Link Pulses (FLP) generated from the off–chip Auto Negotiation function must be present on TDATA4 in order to be transmitted over the media.

Table 4. Clock Pin

Pin No.	Pin Name	Pin Type	Pin Description
46	TCLKIN	I TTL	Transmit Clock Input Users must connect a 25MHz reference clock to this input.

Table 5. External Component Connection Pins

Pin No.	Pin Name	Pin Type	Pin Description
8	RREFTPT	X	Twisted Pair Transmitter External Reference Resistor Connection Pin An external precision resistor must be connected between this pin and ground to set the transmit output current amplitude. To meet the transmit signal levels specified by the ANSI X3T9.5 TP–PMD specification, RREFTPT should be set to 2KΩ ±1%. This value of RREFTPT yields an output current of +/– 40mA. For 100 ohm characteristic impedance UTP applications, this current results in a 1.0V peak differential output voltage.
20 21	C1 C2	X	Twisted Pair Adaptive Equalizer Feedback Capacitor Connection Pins The external capacitor connected to these pins controls the time constant of the adaptive receive equalizer. The recommended value is 400pF.
25	TPRECB	X	Twisted Pair Receiver Bias Resistor Connection Pin The external precision resistor connected to this pin and ground establishes an internal reference current. This resistor should be set to a value of 3KΩ ±1%.

Table 6. Power

Pin No.	Pin Name	Pin Type	Pin Description
3	VDDIO	P	CMOS I/O Power
47	GNDIO	G	CMOS I/O Ground
4	VDD	P	Power
6	VDDDIG	P	Digital Logic Power
40	GNDDIG	G	Digital Logic Ground
7	GNDBG	G	Band Gap Regulator Ground
10	VDDTPT	P	TP Transmit Power
9	GNDTPT	G	TP Transmit Ground
14	VDDFOUT	P	Output Power
13	GNDFOUT	G	Output Ground
24	VDDTPR	P	TP Receiver Power
19	GNDTPR	G	TP Receiver Ground
30	VDDFIN	P	Input Power
27	GNDFIN	G	Input Ground
28	VDD	P	Power
29	VDD	P	Power
45	VDDFM	P	Frequency Multiplier Power
43	GNDFM	G	Frequency Multiplier Ground
38	VDDCLK	P	Clock Power
35	GNDCLK	G	Clock Ground
1 2 16 17 18 31 32 33 34 41 48 49 50 64	GND	G	Substrate Grounds

Table 7. No Connect Pins

Pin No.	Pin Name	Pin Type	Pin Description
36 37 44	NC	–	No Connect– The No Connect pins must be left disconnected.

Operation of Circuit Blocks

(See Figure 2)

Twisted Pair Transmitter Output and Receiver Input

Output

The output transmits MLT3 coded signals to the twisted–pair transmit transformer as shown in Figure 1. Since transmit waveshaping is employed, an external transmit filter may not be required.

(MLT3 is a coding scheme in which every logical HIGH bit on the transmitter input stream produces alternately a positive or a negative pulse on the output and every logical LOW bit produces no positive nor negative pulse on the output.)

Input

MLT3 coded signals are received at the input from the twisted–pair receive transformer as shown in Figure 1. A squelch function is applied to determine if sufficient energy exists on the media to effect data recovery. If enough energy is detected, an equalizer filters the receive signal to undo the effects of the media including attenuation, phase distortion and base line wander. The receiver inputs must be driven differentially in order to assure proper operation.

IEEE 802.3u PCS PHY or MAC Interface

The MAC interface is a TTL–level interface composed of five parts: receive data, receive signal detect, transmit data, and two control signals, $\overline{\text{TDIS}}$ and $\overline{\text{LB}}$. The transmit and receive parts each have independent clocks.

Receive Data

A Digital–Phase–Lock–Loop is used to recover the incoming nominal 125 MHz data stream from the serial port data. The DPLL maintains frequency lock with the received data with only minimal transitions in the data stream. (The stream cipher algorithm, when combined with 4B/5B coding, can generate up to sixty bits, which is 480 nS, without a transition on the media). The recovered data and clock are used by the Decoder to extract the received NRZ data stream.

Data received is output on the RDATA4 – RDATA0 outputs. Five new bits are output on each rising edge of RSCLK. The serial data reception order is: RDATA4, first bit received, and RDATA0, last bit received. RSCLK is derived from the incoming bit stream. Data on RDATA4 – RDATA0 is not aligned to symbol boundaries.

When $\overline{\text{AUTONG}}$ is low, the Fast Link Pulses (FLP) and Normal Link Pulses (NLP) received from the media will be present on RDATA4.

Receive Signal Detect

The state of SD is determined by a combination of signals from the Squelch and Auto Equalization functions. For SD to be asserted, the squelch must detect sufficient energy on RDH and RDL, and the Equalizer must have equalized.

Transmit Data

The 5–bit data symbols to be transmitted are obtained from the MAC via the TDATA4 – TDATA0 inputs. A new 5–bit symbol is strobed in on each rising edge of TCLKIN and are output at the TDH/L output. The serial data transmission order is: TDATA4, first bit transmitted, TDATA0, last bit transmitted.

The NRZI data stream is converted to MLT3 coded data and output at the TDH/TDL outputs.

When $\overline{\text{AUTONG}}$ is low, the Fast Link Pulses (FLP) generated from the off–chip Auto–Negotiation function must be present on TDATA4 in order to be transmitted over the media.

Transmit Disable ($\overline{\text{TDIS}}$) and Parallel Loopback ($\overline{\text{LB}}$) Controls

When the $\overline{\text{TDIS}}$ and $\overline{\text{LB}}$ inputs are HIGH, the MC68833 is in its normal mode of operation. When $\overline{\text{TDIS}}$ is LOW, TDH and TDH are both forced LOW (quiet state).

When the $\overline{\text{LB}}$ input is HIGH, the MC68833 is in normal operation. When $\overline{\text{LB}}$ is LOW, the MC68833 is in LOOPBACK mode. In this mode, the serial transmit data stream that is normally delivered to the TDH and TDL outputs is also routed to the receive data circuit where it is recovered and delivered to the RDATA4 through RDATA0 outputs. If it is undesirable to place the serial data stream on the TDL and TDH outputs, the $\overline{\text{TDIS}}$ input must be driven to the low logic state. Additionally, when the $\overline{\text{LB}}$ input is LOW, the RDH and RDL inputs are ignored. Furthermore, the signal detect output, SD is driven high when $\overline{\text{LB}}$ is in the low logic state.

Auto–Negotiation ($\overline{\text{AUTONG}}$) “Pass–Through” Control

When this input is LOW, the off–chip auto–negotiation fast link pulses can be sent to the TDATA4 input and fast link pulses or normal link pulses can be received from the RDATA4 output. The MC68833 will “pass–through” these pulses.

Frequency Multiplier

The Frequency Multiplier block utilizes the external 25 MHz signal (TCLKIN) as a reference to produce the 125MHz signal which is needed for operation of the digital phase locked loop (DPLL) circuitry.

System Management

The System Management block controls the standby mode.

Electrical Characteristics

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those indicated in the operation sections of this data sheet. Exposure to Absolute Maximum Ratings conditions for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature Range	Tstg	–65	150	deg C
Power Supply Voltage Range	VDD	–0.3	7	V
Voltage on any TTL Compatible Input pin	V	–0.3	VDD+0.3	V
Voltage on RDH/RDL Input Pins with respect to Ground	V	–0.3	VDD+0.3	V
Differential voltage on RDH/RDL Input Pins	V			

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage Range	VDD	4.75	5.25	V
Ambient Operating Temperature Range	Ta	0	70	deg C

ESD

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Motorola employs a human–body model (resistance = 1500 W, capacitance – 100pF). The MC68833 will withstand exposure to 2KV standard human body model ESD testing.

TTL/CMOS Input and Output DC Characteristics

(Unless otherwise noted Minimum and Maximum limits apply over the recommended ambient operating temperature and power supply voltage ranges)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TTL Compatible Inputs						
Low State TTL Compatible Input Voltage	Vil (TTL)				0.8	V
High State TTL Compatible Input Voltage	Vih (TTL)		2.0			V
Input Current TTL Compatible Input Pins	Ii (TTL)				±10	uA
TTL/CMOS Compatible Outputs						
Low State TTL/CMOS Compatible Output Voltage	Vol	Iol = 4mA			0.45	V
High State TTL/CMOS Compatible Output Voltage	Voh	Ioh = –400uA	TBD			V
High State TTL/CMOS Compatible Output Voltage	Voh	Ioh = –4mA	2.4			V
Three State Output Leakage Current	Ioz	0V ≤ Voz ≤ VDD			50	uA

Twisted Pair Input and Output DC Characteristics

(Unless otherwise noted Minimum and Maximum limits apply over the recommended ambient operating temperature and power supply voltage ranges)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Twisted Pair Receiver Inputs						
Twisted Pair Common Mode Input Voltage Range	VICMTP	4.75V ≤ VDD ≤ 5.25V	2.2		TBD	V
Twisted Pair Peak Differential Input Voltage	VIDTP	4.75V ≤ VDD ≤ 5.25V			1	V
Twisted Pair Differential Input Resistance	RDIFFTP	4.75V ≤ VDD ≤ 5.25V	10			KΩ
Twisted Pair Common Mode Input Current	IICMTP	4.75V ≤ VDD ≤ 5.25V			10	uA
Twisted Pair Differential Input Squelch Threshold Voltage	VITPSQ	4.75V ≤ VDD ≤ 5.25V	TBD		TBD	V
Twisted Pair Transmitter Outputs						
Twisted Pair Differential Output Current High Current State	IODHTP	4.75V ≤ VDD ≤ 5.25V VO = VDD ± 0.5V RREFTPT =2KΩ ± 1%		40		mA
Twisted Pair Differential Output Current Low Current State	IODLTP	4.75V ≤ VDD ≤ 5.25V VO = VDD ± 0.5V	0	0.5	TBD	mA
Twisted Pair Differential Output Offset Current	IODOSTP	4.75V ≤ VDD ≤ 5.25V VO = VDD ± 0.5V			0.5	mA
Twisted Pair Differential Output Amplitude Error		4.75V ≤ VDD ≤ 5.25V VO = VDD	–5		5	%
Twisted Pair Differential Output Voltage Compliance		4.75V ≤ VDD ≤ 5.25V VO = VDD ± 1.1V	–2		–2	%

1. For a logic high, RDL must be at least Vidiff(min) but no more than Vidiff(max) lower than RDH. For a logic low, RDL must be at least Vidiff(min) but no more than Vidiff(max) higher than RDH.

Power Supply DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Current	IDD	VDD = 5.25V[2]			300	mA
Power Supply Current Standby Mode (AWAKE Input Low)	IDDSB	VDD = 5.25V			TBD	uA

2. The supply current consumption depends upon the mode of operation selected.

TCLKIN Timing (See Figure 4)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TCLKIN Period (1)	tCK1			40		nS
TCLKIN Time Low	tCK2		8			nS
TCLKIN Time High	tCK3		8			nS
TCLKIN Transition Time	tCK4				5	nS

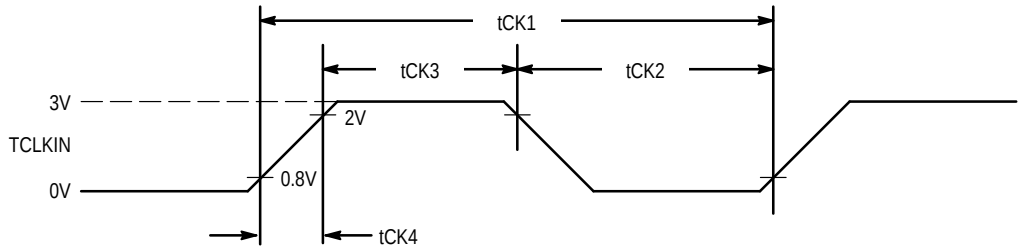


Figure 4. TCLKIN Input Voltage Levels for Timing Measurements

TP Transmit Switching Characteristics (See Figure 6)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Twisted Pair Differential Output Transition Time Zero to Positive	tTPT1	4.75V ≤ VDD ≤ 5.25V[1]		4		nS
Twisted Pair Differential Output Transition Time Zero to Negative	tTPT2	4.75V ≤ VDD ≤ 5.25V[1]		4		nS
Twisted Pair Differential Output Transition Time Positive to Zero	tTPT3	4.75V ≤ VDD ≤ 5.25V[1]		4		nS
Twisted Pair Differential Output Transition Time Negative to Zero	tTPT4	4.75V ≤ VDD ≤ 5.25V[1]		4		nS
Twisted Pair Differential Output Jitter	tTPT5	4.75V ≤ VDD ≤ 5.25V[1,2]		0.8		nS

1. Measured differentially across the output of test load A
2. Specification established by design and laboratory characterization

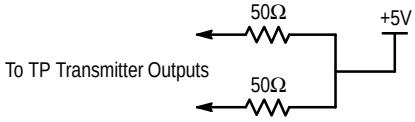


Figure 5. TP Tramitter Test Load

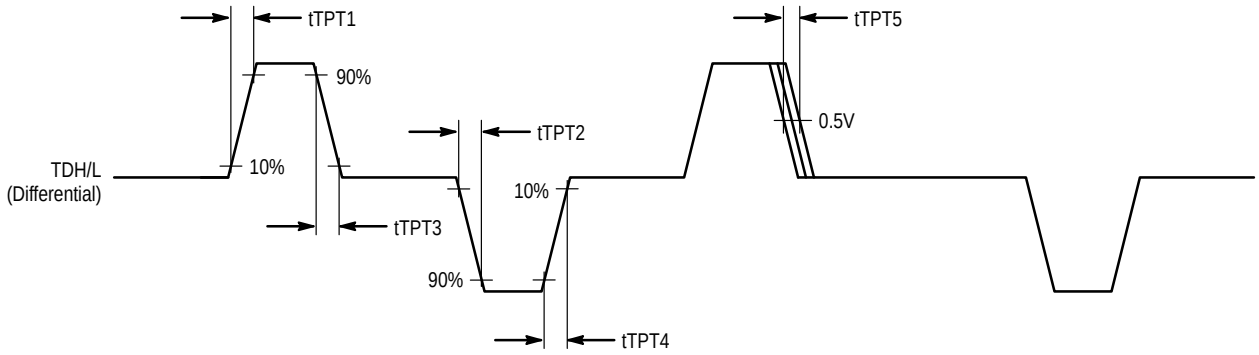


Figure 6. TDH/L Differential Twisted Pair Transmit Output Timing Characteristics
(NOTE: Specification established by design and laboratory characterization)

Parallel Interface Timing (See Figure 8)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
RSCLK Period	tPI1		36	40	44	nS
RSCLK Time Low	tPI2	**1**	18		22	nS
RSCLK Time High	tPI3	**1**	18		22	nS
Time to RDATA Invalid	tPI4		8			nS
Time to RDATA Valid	tPI5				32	nS
TCLKIN Period	tPI6		39		41	nS
TCLKIN Time Low	tPI7		18		22	nS
TCLKIN Time High	tPI8		18		22	nS
TDATA Setup Time	tPI10	**2**	12		40	nS
TDATA Hold Time	tPI11	**2**	0		28	nS

1. This parameter is specified with the receiver operating at 125 MHz.
2. This is with respect to TCLKIN

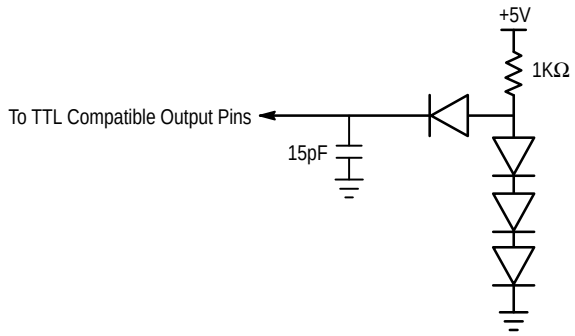


Figure 7. TTL Compatible Output AC Test Load

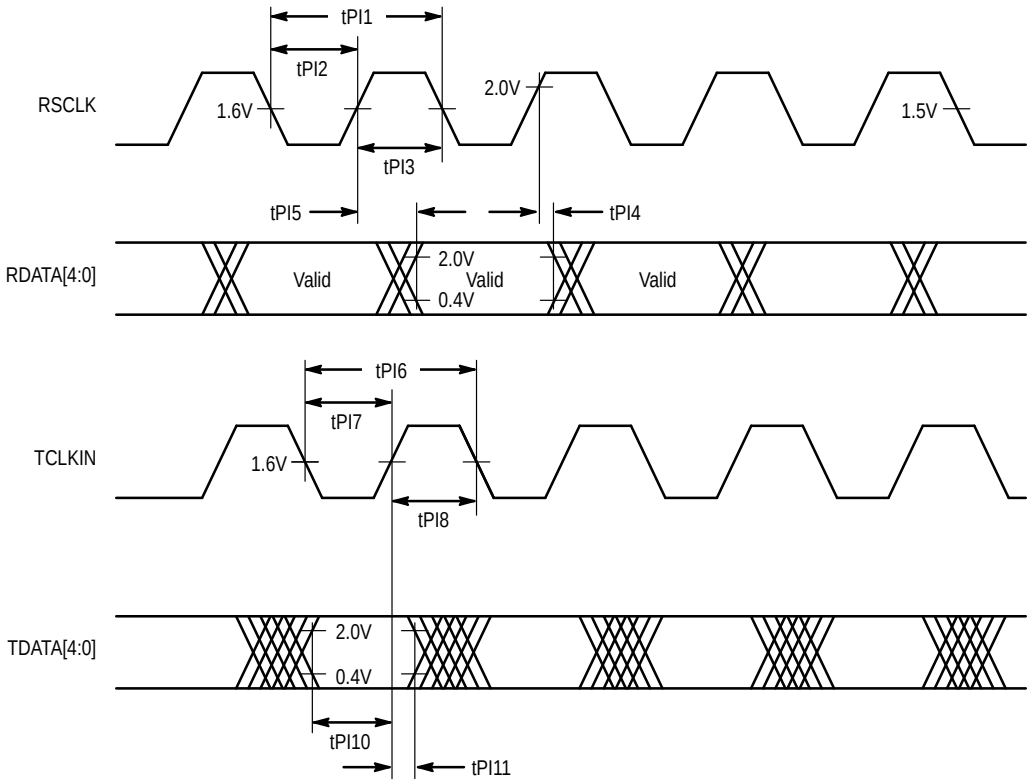
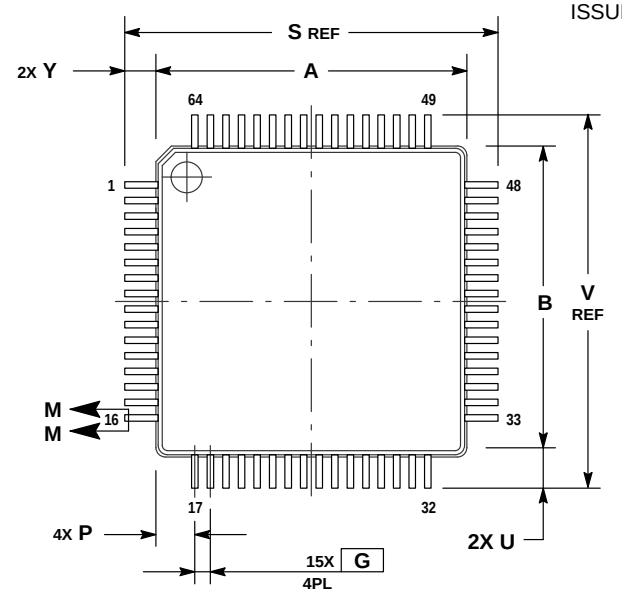
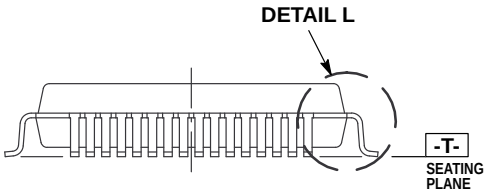


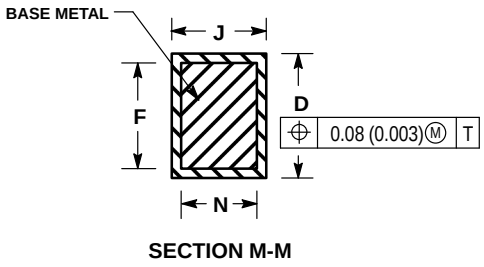
Figure 8. Parallel Interface Timing

OUTLINE DIMENSIONS

FA SUFFIX
PLASTIC TQFP PACKAGE
CASE 931–02
ISSUE D







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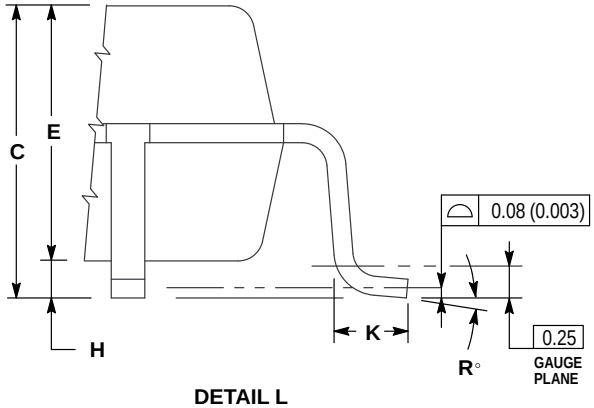

DETAIL L

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSTION. ALLOWABLE PROTRUSTION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED WHERE THE BOTTOM OF THE LEAD EXITS THE PLASTIC.
4. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.35 (0.014). DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 (0.003).
5. AS PLATED SOLDER THICKNESS SHALL BE 0.0076 (0.0003) / 0.0203 (0.008).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	—	2.45	—	0.096
D	0.17	0.27	0.007	0.011
E	1.80	2.20	0.071	0.087
F	0.17	0.24	0.007	0.009
G	0.50 BSC		0.020 BSC	
H	—	0.35	—	0.014
J	0.09	0.20	0.004	0.008
K	0.45	0.75	0.018	0.030
N	0.09	0.16	0.004	0.006
P	1.20	1.30	0.047	0.051
R	0°	9°	0°	9°
S	12.00 REF		0.472 REF	
U	0.95	1.05	0.037	0.041
V	12.00 REF		0.472 REF	
Y	0.95	1.05	0.037	0.041

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