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FAIRCHILD SEMICONDUCTOR™

Taking Advantage of ECL Minimum-Skew Clock Drivers

CLOCK DISTRIBUTION BACKGROUND

Digital systems have tended from their inception toward incorporation of higher speed elements rather than architectural changes as the solution to the computational speed problem. One result of this has been mounting pressure on the semiconductor elements of these systems for higher speed and all that this implies. Not only the operating frequency and signal propagation delay but also the relative timing relationships of devices performing parallel tasks were challenged. As semiconductor process improvements pushed operating speeds higher, the evolution from individually-packaged to multiply-packaged gates helped reduce delay and speed differences among like devices. Even so, areas still existed where system designers demanded ever greater improvements in performance uniformity of digital logic elements. The synchronization signal generation system, often referred to as the clock system, is one area in need of such improvement.

Most digital logic systems employ some means of synchronizing the actions carried out by the system's elements. The precision with which these various elements are regulated can be shown to have a direct effect on the overall speed of the system. The less time variation that must be allocated to the logic elements in the signal path, the faster that operation may be executed. Therefore, the overall time to perform all operations may be reduced or the system speed may be increased. In addition, the coordinated timing of the synchronizing system itself must benefit from an equivalent reduction in relative timing of its elements, or else only limited overall benefit to system performance is possible.

CLOCK NETWORK ELEMENTS

The typical synchronizing or clock system consists of several closely related elements:

- a primary signal source, usually a precisely regulated, high frequency oscillator,
- frequency dividers to derive lower frequencies from the primary source,
- distribution amplifiers to boost signal power or supply separated loads,
- signal delay, duty-cycle alteration or re-synchronizing elements,
- interconnect wiring, connectors and signal distribution network,
- and a power source and distribution system for the semiconductor devices in the system.

Each of these elements contributes a degree of variability to the overall timing precision capability of the system. By virtue of the fact that the physical properties of each element can be controlled only within certain limits, the complete system will exhibit a variability somewhat larger than its elements taken individually. The effect of the variations contributed by the elements to the overall system variability is a physical fact that may be demonstrated mathematically.

Among the factors affecting variability are:

- physical size such as the length of wiring,
- electrical properties such as resistance and charge,
- internally generated and externally induced noise,
- and environmental factors like temperature and altitude.

The visible effect of variability on the system timing is popularly termed "skew". Similarly, the individual variabilities of each element are likewise termed "skew". The term "skew" is used also to describe the difference in delay between like paths taken by signals in a logic device or system. However, as with many useful terms when carelessly applied, the term "skew" can lead to some confusion unless it is more precisely defined.

When applied to the differences in propagation of electrical signals through like paths in a logic system, the term "skew" will be taken to mean "differential timing error". In terms of the overall effect on the desired timing performance of the affected system or device, "skew" will be defined as "a deviation or asymmetry from the mean or desired timing value". The latter meaning of skew will assume greater importance in the prediction and analysis of system timing errors to be covered later in this note.

MEETING THE SKEW CHALLENGE

Control of skew in systems is at best a difficult challenge for design engineers. At its worst, skew can be the thing that makes or breaks a design. So, to give engineers an advantage in controlling skew, Fairchild offers ECL devices specifically designed to minimize the device-related component of skew. In addition, the skew properties of these devices are specified and tested. This has been done to reduce the design effort required to compensate for device-related skew effects. The results are tighter system timing margins, more reliable operation and faster operating speeds. This means greater system through-put and information processing efficiency.

300-SERIES ECL—The Best Weapon Against Skew

300-Series ECL has some natural advantages in the war on skew. ECL differential amplifiers are minimum-skew by their very circuit configuration. The fundamental property of the differential amplifier used as a logic element is balanced switching. The amplifier, Figure 1, is symmetrical. This results in identical switching delays regardless of output. Following stages are added symmetrically, Figure 2, so that overall balance is maintained internally. 300-Series devices designed for minimum-skew also employ a unique die layout to preserve the basic amplifier balance.

Another advantage of 300-Series ECL is its precise, stable V_{BB} reference supply with wide operating power supply range. This reference is compensated for stability from the effects of changes in temperature or supply voltage. 300-Series minimum-skew devices operate from –4.2V to –5.7V supplies as do all other 300-Series logic devices. Advanced semiconductor processing, design and manufacturing result in uniquely low power consumption for this ECL family.

300-SERIES ECL—The Best Weapon Against Skew (Continued)

Augmenting the inherent balanced design of the amplifier, 300-Series minimum-skew devices feature differential inputs and outputs. Selected devices have an additional single-ended input and input selector for use as a test input or auxiliary main input. However, skew tolerances are wider when using the single-ended input. The differential outputs are fully buffered emitter-followers. They are designed to have symmetrical transitions and skew performance under symmetrical loading conditions. Some devices also make an external V_{BB} reference available for use in situations where the inputs must be separately biased.

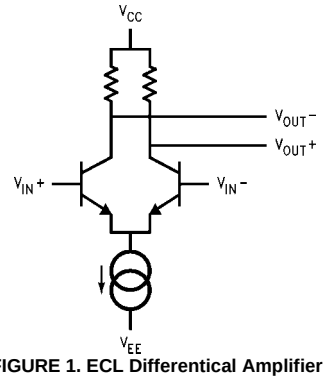

FIGURE 1. ECL Differentical Amplifier

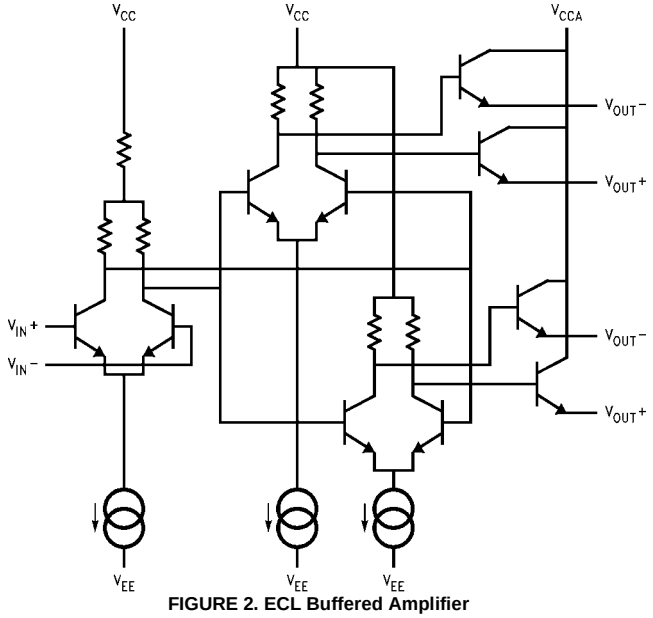

FIGURE 2. ECL Buffered Amplifier

Skew can be adversly affected by packaging. For this reason Fairchild has chosen to supply F100K minimum-skew devices in packaging complementing their inherent performance. F100K devices are supplied in SOIC and PCC packaging as appropriate for the intended class of service; commercial and industrial.

PACKAGE TYPE AND LAYOUT

Packaging and pinout also affect skew performance. Smaller, more symmetrical packaging like PLCC and SOIC types contribute less to skew than do DIP packages. Their smaller size reduces parasitic inductance, a contributor to noise and signal delay. Symmetrical pin layout equalizes path length for all signals from the die to the circuit board thereby reducing a skew component. And, additional output V_{CC} pins help reduce skew by providing extra paths for output signal return currents to ground.

TESTING

Despite careful design, packaging and advanced processing, skew performance is worth little unless its effect on device performance can be accurately known. Reliable skew values, guaranteed by test, are essential in predicting system performance. 300-Series ECL minimum-skew devices are fully tested and specified for all standard DC and AC parameters as well as all relevant skew parameters.

It should be appreciated that devices designed for minimum skew values of a few tens of picoseconds are difficult to test using ordinary IC test equipment. Therefore, Fairchild has developed advanced production test equipment capable of measuring the AC and skew characteristics of these high-performance devices. This results in more accurate and dependable data for design and greater uniformity of product.

SYSTEM DESIGN OBJECTIVES

The best way to take advantage of minimum-skew driver capabilities is through good system design. Minimum-skew specified devices cannot compensate for or improve on a poor system design. However, these devices can add extra margin to a good design. They also permit more predictable performance in well designed system environments.

The majority of problems that plague clock generation and distribution systems lies beyond the active devices and outside of their effect. These problems result from shortcomings in the signal transmission, power supply or mechanical systems. A good system design should give the minimum-skew driver a fighting chance to perform satisfactorily. This is the primary job of the system designer.

But, before the designer can effectively use these devices, a reasonable set of electrical and mechanical specification objectives for the overall system must first be developed. Next, the device specifications as they apply within the scope of the system specification must be understood thoroughly. Only then can devices with performance appropriate to the overall objectives be selected. Indeed, the process of resolving device and system objectives may reveal incompatibilities. Then either the system requirements or the choice of device must be changed. Lastly and most importantly, the active devices must not be overworked or handicapped by improper load conditions or the system environment.

A good set of system objective specifications will incorporate all of the following considerations:

- A stable, adequate, noise-free and well isolated DC power supply and power distribution system,
- Noise-resistant and RFI/EMI-proof design and suppression techniques,
- A carefully designed signal transmission and distribution system,
- Appropriate and efficient printed circuit board layout,
- Adequate cooling for all power-dissipative devices,
- Environmental requirements like altitude, humidity, and temperature:
- The appropriate active devices for the required performance.

The sections that follow present design techniques and guidelines formulated around the above objective specifications. Colateral sources where more complete or additional design information may be found will be noted or may be found listed in the Appendix.

POWER SUPPLY NETWORK DESIGN OBJECTIVES

ECL minimum-skew devices can benefit especially from a well designed power supply system. Though not unique for minimum-skew devices, the design of ECL power supply systems must achieve several important objectives.

1. The power system must supply constant, noise-free voltage at adequate current levels to all active devices in the system.
2. The power system must appear as a virtual battery to each device. That is, it must effectively isolate devices such that each appears to be independently powered. Thus, noise signals resulting from operations going on within each device will not propagate to other devices through the power supply system.
3. The power supply system also must propagate without distortion the return or image currents for all signal-carrying transmission lines.
4. The power distribution planes within each printed circuit board (FCP) should act as electrostatic shields to reduce RFI radiation from the transmission line system.

These objectives can be adequately met if reasonable care is taken in the design of the power supply feed system, the supply isolation and bypassing and the organization and layout of the PCB's.

More information on power supply design considerations can be found in the “F100K ECL Logic Databook and Design Guide”.

POWER SUPPLY BYPASSING

The topic of power system bypassing is generally given inadequate treatment in logic applications literature. The common approach taken is to simply recommend that a 0.1 μF ceramic capacitor be used for every so many devices. In systems with frequencies predominating below 10 MHz and edge rates on the order of 1V/ns or slower, this prescription may be adequate. However, for systems with frequencies above 10 MHz and edge rates less than 1V/ns, the above prescription is bad medicine. The reasons are easy to explain but require a look at the role and objective of bypassing.

Bypassing serves two general roles in the power supply system—filtering and energy storage. Both of these are related by the fact that, in performing filtering, the capacitor stores and releases energy. To be more specific, the four goals of an efficient bypassing scheme are:

1. Reducing the internal impedance of the power distribution wiring system,
2. Low-pass filtering of the DC being supplied to each active device,
3. Isolating active devices from each other, and
4. Controlling noise due to transient current demands on the supply system.

These four goals are interrelated and are parts of the primary objective of having each active device appear as though powered by an internal, ideal battery. In fact, goals 2, 3 and 4 can be considered as results of achieving goal 1. Reducing the impedance of the power system conductors at all frequencies in the system pass-band helps accomplish all goals of efficient bypassing.

The “F100K ECL Logic Databook and Design Guide”) recommends multi-layer PCB construction with entire layers assigned to each supply voltage and ground. While this might appear to be an ideal power distribution method for DC, it increasingly deviates from the ideal as frequency

POWER SUPPLY BYPASSING (Continued)

increases. For frequencies below about 10 MHz, the internal impedance of power plane layers may be in the range of 1Ω to 10Ω depending upon geometry. At higher frequencies, and especially above 50 MHz to 100 MHz, skin and striction effects cause a ten-fold or greater increase in internal impedance. This means that current changes resulting from switching of the active devices at high frequencies can induce large voltages in the power planes. These noise voltages affect nearby circuits and signals on transmission lines. To eliminate this interference, a means is needed for decreasing the impedance of the planes at high frequencies.

Restricting the pass-band of a wire transmission system to frequencies approaching DC is termed low-pass filtering. Suitably sized capacitors placed at regular intervals on a wire transmission system form a low-pass filter. As frequency increases, the capacitor's reactance decreases. This reduces the amplitude of the signal as it traverses the transmission line. Therefore, the effect of noise generated by an IC on the power supply voltage of its near neighbors is reduced. In addition, lowering the internal impedance of the power plane system reduces radiated RFI and the effects of external interference sources on the power supply system. And, the power plane system will appear as a more nearly uniform AC ground for signal-carrying transmission lines in adjacent layers of the PCB.

Another property of the transmission line, low-pass filter is that it delays signals traveling on the line. In addition to attenuating AC signals and noise generated by the active devices, the signals are also delayed. This effectively increases the isolation between devices in the time-domain. Naturally, as the delay of the power supply transmission system increases, the closer the bypass capacitors must be to the noise source in order for them to be optimally effective.

Supply bypassing is generally less critical in F100K ECL systems than in 10K systems, especially since output load balancing can be used. Bypassing still must perform the functions mentioned previously, but the balanced switching of F100K results in a quieter overall system to begin with. The primary suppression role of bypassing is in controlling noise from unbalanced output switching on the power system.

The selection of bypassing components for F100K systems should be based on the expected operating frequencies of the various networks as well as the output transition rates. Also, the choice of balanced versus unbalanced output loading plays a major role.

Capacitors bypass or suppress frequencies best near their self resonant frequency, Figure 3. At this frequency the capacitor appears to be more nearly a short-circuit. Below resonance the capacitive component of reactance dominates. Above resonance the inductive component plays a bigger role. The effective impedance at resonance is the resistive component or ESR (equivalent series resistance). It is normally desirable to minimize the ESR so that the capacitor is a good short circuit. However, it may be more desirable to have some resistance in series with the capacitor in order to broaden the range of frequencies where the capacitor is effective.

In the time domain, the capacitor's behavior becomes more complex. Fast risetime transient pulses contain frequencies generally far above the capacitor's self-resonant frequency. During these pulses, the capacitor has an instantaneous impedance value ten or more times its ESR. For this reason, it is often desirable to "bandspread" the bypass capacitor by using several different capacitor values in parallel. An example of this is placing 0.1 μF, 10 nF and 1 nF ceramic chip capacitors in parallel. The capacitors may be attached to the PCB in a sandwich, "piggyback" style, provided their lengths are equal. Leaded capacitors may be placed close together on the circuit board to achieve a similar result, also.

The signal frequencies being transmitted by the logic devices and the switching frequencies of device outputs are not the only signals that must be handled by the bypassing. There are also frequencies associated with the energy transfer between different functional groups of components on the PCB's and in the overall system. For instance, a memory system may be active at one-fourth of the rate of an associated CPU group. The peak energy exchange rate between the memory system and the power supply would be one-fourth that of the CPU and the supply. Though the memory may handle signals at the same frequency as the CPU during communications, the power supply system also sees the lower frequency as well. Therefore, the power supply system and the memory/CPU circuit board must have bypass capacitors for both sets of frequencies. For this reason, larger value capacitors, usually tantalum or similar electrolytic types, are found on circuit boards. These capacitors smooth energy transfers at lower frequencies.

CLOCK SOURCE NOISE CONTROL

The clock system is normally the source of most high frequency noise in digital systems. Part of the overall design objective for the clock system is that it not create interference with other parts of the system.

Isolation of the clock source and its associated distribution amplifiers is an effective way of reducing such interference. Insertion of a ferrite choke in the power supply feed to the active devices forms a noise filter that reduces interference from these devices to other logic through the power system. The filter may take the form of a Pi-network or longitudinal choke as in Figure 4. In selecting the inductor, the core must have sufficient current rating to handle the load without saturation. Also, the core material should be capable of operating over the frequency range of the oscillator and associated components. Type 3B or 4B core materials are typical for ECL applications. Suitable 6-hole ferrite chokes are available from Fair-Rite, Siemens, Ferroxcube and others.

CLOCK NETWORK TOPOLOGIES

The choice of clock network topology is intimately a part of the architecture and partitioning of the system. To recommend a particular topology would be presumptive. Therefore, the scope of this discussion will be limited to more general considerations of the networks.

CLOCK NETWORK TOPOLOGIES (Continued)

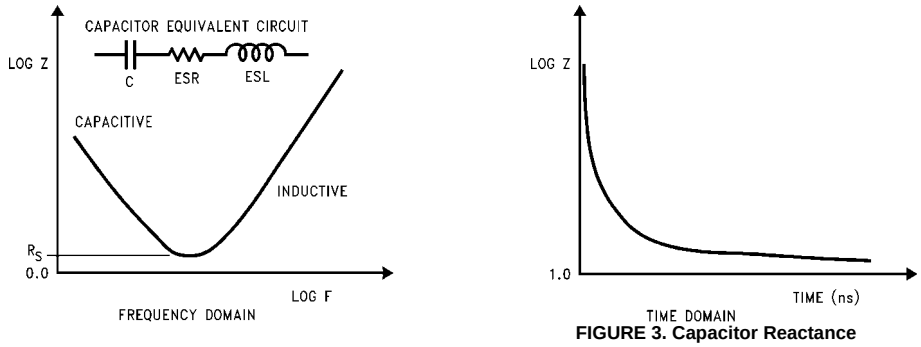

FIGURE 3. Capacitor Reactance

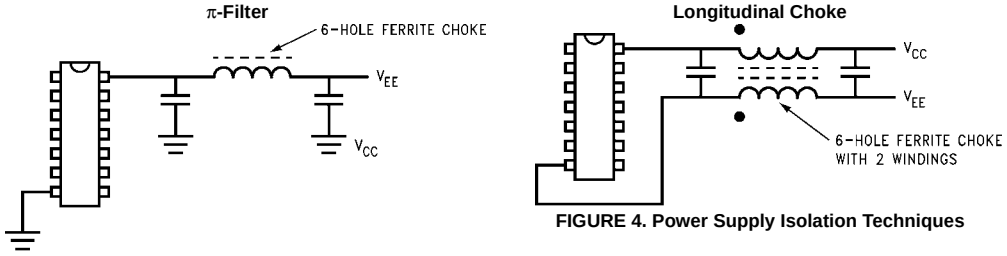

FIGURE 4. Power Supply Isolation Techniques

The general forms of networks suitable for clock distribution are: point-to-point, daisy-chain, radial (star), branching (tree), auxiliary main input and bus. Any of these can be implemented as single-wire-over-ground or balanced differential networks. The differential method has advantages of less suceptability to interference from noise, temperature effects, threshold shifts and common-mode signals. These, plus the network's inherent balance, mean lower skew. F100K is particularly suited to use in differential networks. It employs differential outputs on virtually all devices and differential inputs particularly on clock distribution devices.

Naturally, to benefit from the advantages of the differential network, its balance must be maintained. Loading and terminations should be applied equally to both conductors of the differential pair. If loading is not balanced, the propagation delay of each conductor will be different. This can lead to differences in the arrival time of the complementary signals thereby increasing skew.

Regardless of the network topology, the relationships of network impedance, drive capability, critical loading and termination must always be considered.

IMPEDANCE, LOADING AND INTERFERENCE

The equivalent generator resistance of the F100K output emitter follower is approximately 7Ω. With this low value, the output is nearly an ideal voltage source capable of driving almost any reasonable value of load impedance or transmission line type. High impedance transmission lines (above 50Ω) are difficult to achieve in practice on PCB's with thin dielectrics. However, high impedances are more common with twisted-pair lines. The propagation velocity of energy is more affected by capacitive loading on high impedance lines. And high impedance lines are more susceptable to crosstalk and noise interference.

Low impedances (less than 50Ω) require wide line widths, a problem where small packages and dense PCB layout are desirable. Also, lower impedances require more energy from the driver. For a given output type, this results in lower voltage swings into the line and higher DC and AC power since the termination value is lower, also. An advantage of lower impedances is that of their being less affected by capacitive loading and crosstalk.

The effect of loading versus line impedance is easily illustrated. A 50Ω line in FR-4 material has an unloaded propagation delay of about 56 ps/cm. Unloaded 25Ω and 100Ω lines in this material have the same delay. By adding only 1 pF/cm load to the 50Ω line, the delay is increased by 21 ps. The 25Ω line's delay increases 11 ps and the 100Ω line by 38 ps. Clearly, skew-versus-loading is easier to control if the line impedance is kept low. This is the reason that, from all practical standpoints, 50Ω is widely considered as the best line impedance choice.

Controlling the chosen impedance and skew in practical networks can be difficult in practice. This is particularly true where many loads need to be driven in precise phase relationship to a source. Ideally, it would be best to drive each load in a point-to-point connection. Except for the most exacting applications, this can be costly in terms of board space, power and components.

Series-terminated radial or star networks can be used in many cases to drive multiple loads from one output. As long as the load impedance driven does not exceed output drive capability, 2, 3 or 4 lines may be driven. Radial nets may also be driven from the end of another transmission line connected to the driver output. In this case, the impedance of the line between the driver output and the star-point must be less than the impedance of any line connected to it. Each line radiating from the star-point is driven through a series termination. The value of the resistor is

DIFFERENTIAL LINE LAYOUT (Continued)

chosen to give the minimum required voltage swing at the input connected at the receiving end of the line. More details for designing radial networks may be found in of the "F100K Logic Databook and Design Guide".

Timing and skew are more difficult to control with the daisy-chain network and its bi-directional equivalent, the bus network. Differences in the individual load values attached to the net contribute to increased skew. This is especially true in parallel-path buses where there is another complicating factor. The bus is normally bi-directional. Whereas the daisy-chain net has one source and multiple loads, the bus has multiple sources. Delay from one source to a given destination, relative to another source to the same destination, may create difficult timing situations, especially where all sources share a common distributed clock. In such situations, consideration should be given to re-synchronization of the common clock relative to the other signals being transmitted from the particular location on the bus. This re-timed clock will then be properly synchronized to its related signals and a reduction in location-dependent skew on the bus will result.

TERMINATION NETWORKS

Minimum-skew drivers cannot correct the behavior of improperly terminated networks. In fact, operation of any driver-network combination is impaired by faulty termination. Faulty termination corrupts signals and contributes to skew, timing and noise problems. A brief look at the goals of basic series and parallel termination networks will clarify their use.

The goal of parallel termination is absorbtion of all transmitted energy at the network terminus with none reflected to the source. Any signal distortion occurring is solely due to reflections from the loads attached to the line. The parallel termination should have a resistive value close to that of the network's impedance to be optimally effective. Parallel terminations may be simply a single resistor from the terminus of the network to a voltage source (normally −2V) or they may be Thevenin networks equivalent to the single resistor and voltage source values.

The series termination operates on the principle of Ohm's Law. As a voltage divider, the goal of the series termination is to reduce the driver's output voltage transmitted into the line by about one-half. When this voltage (referred to as the incident wave voltage) reaches the opposite end or terminus of the network, which is unterminated and approximately an open circuit, the voltage level doubles. A receiver at the terminus of the line sees its full input voltage swing. However, receivers between the input and terminus ends see only the voltage transmitted into the line. All of the voltage arriving at the terminus is reflected back to the source with the same polarity as that of the incident wave voltage. As this reflected wave voltage transits the line toward the source end, the voltage level along the line is raised to the full swing voltage of the driver's output. Only at the instant when this voltage wave reaches each input will that input see its full voltage swing. Therefore, intermediate loads experience a period where input voltage is at or near threshold level. Consequently, there is a delay of more than one line transit time until the input voltage reaches a proper level. For this reason, series terminations are used almost exclusively in point-to-point networks.

In some cases, networks may require combinations of series and parallel terminations to achieve satisfactory performance. Networks of this type must be carefully designed and tested on an individual basis to assure correct operation. The laws governing such networks are the same as for the basic networks and terminations. Further information on terminations, other network configurations and their design requirements can be found in the "F100K ECL Logic Databook and Design Guide".

PC BOARD LAYOUT RECOMMENDATIONS

Proper PC board layout is high on the list of important considerations when using ECL minimum-skew devices. The performance enhancement offered by minimum-skew devices can be wasted by inadequate layout. So, a look at some additional layout recommendations aimed at maintaining the high performance that these ECL devices are capable is essential.

F100K ECL minimum-skew devices are available standardly in surface mount packaging. Devices use either SOIC and PCC packages. Each package type has its own unique mounting requirements. However, there are some common areas where both types can benefit from attention to layout. These areas are bypassing location, power and ground connections, differential line layout and power plane isolation.

Literature available from Fairchild Semiconductor is listed in the Appendix.

BYPASS CAPACITOR PLACEMENT

The placement of bypass capacitors is as important as their electrical characteristics. Placement and connection into the system can significantly alter the effectiveness and electrical performance of the bypassing elements. Ideally, the capacitor is placed as close as possible to the device requiring the bypass. Only an absolute minimum of wire length should connect the capacitor to the power planes or the IC leads. If surface mount capacitors are used, the mounting lands are connected directly to the power planes through vias and omit any extra wiring. Figure 5 shows the recommended placement and connection methods for PCC layouts on conventional multi-layer PCB's. Figure 6 shows the recommended application where SOIC packaging is used.

POWER AND GROUND CONNECTIONS

Power and ground connection paths must be kept short otherwise excess inductance is introduced in the IC's power leads. Excess inductance reduces the effectiveness of any associated bypassing and makes the power supply seen by the IC less stable. Where multiple power or ground pins are provided on the IC package, all should be connected to the appropriate supply potential. Figure 7 shows examples of correct and incorrect power connections to PCC and SOIC packaged devices.

DIFFERENTIAL LINE LAYOUT

Fairchild's minimum-skew devices generally employ differential inputs and outputs as an aid in combating skew. When combined with properly designed differential transmission line layouts, precise system timing is possible. However, careless layout of differential lines can cause serious timing and skew problems. By observing a few simple rules, effective differential transmission systems can be easily designed.

1. Differential transmission lines must be organized in pairs. Lines originating at complementary outputs must

DIFFERENTIAL LINE LAYOUT (Continued)

be paired throughout their lengths. Additional spacing should be allowed between pairs in all layers. Approximately twice the spacing between the lines of the pair should be used between pairs.

2. Both lines of a differential pair must be of equal length. Changes of direction must be accompanied by either an equal and opposite change of direction or additional length must be added to the resulting shorter line.
3. Differential lines should be paired (run parallel) in the same layer. When a direction change dictates a change of layer, both conductors should change layers. In general, there should be an equal number of vias in each line as the result of layer changes. The width of the lines may be adjusted according to preserve line impedance.
4. Corners in lines with angles greater than 45° should be mitered or radiused to preserve impedance uniformity.

Figure 8 illustrates these rules with several ways in which differential lines may be implemented correctly and incorrectly.

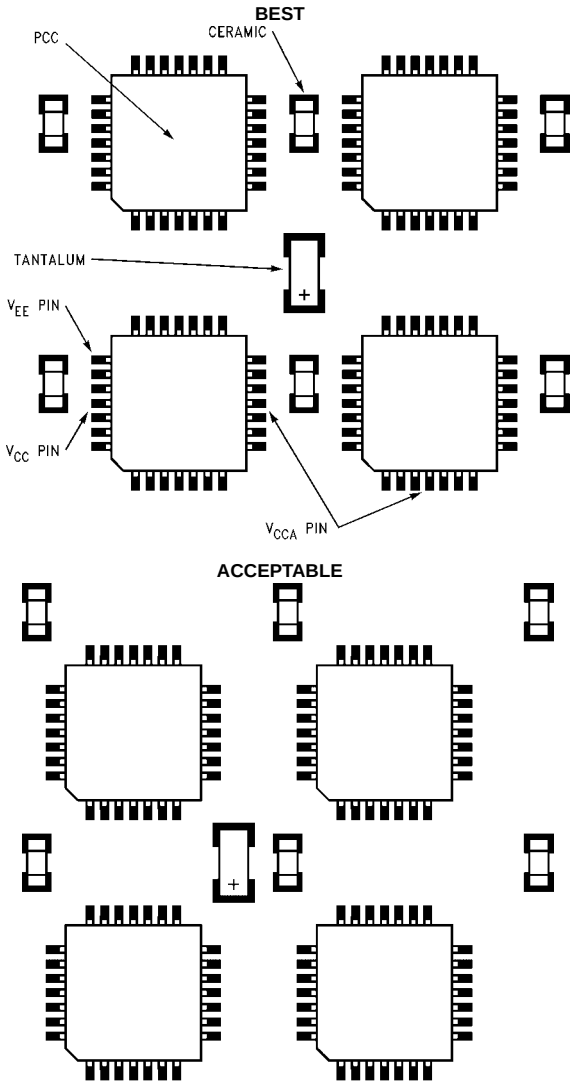

FIGURE 5. PCC Bypass Capacitor Placement

DIFFERENTIAL LINE LAYOUT (Continued)

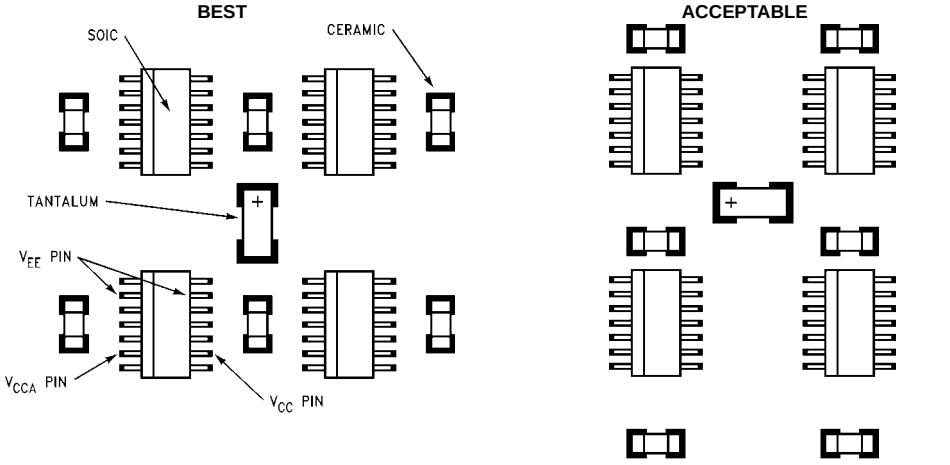

FIGURE 6. SOIC Bypass Capacitor Placement

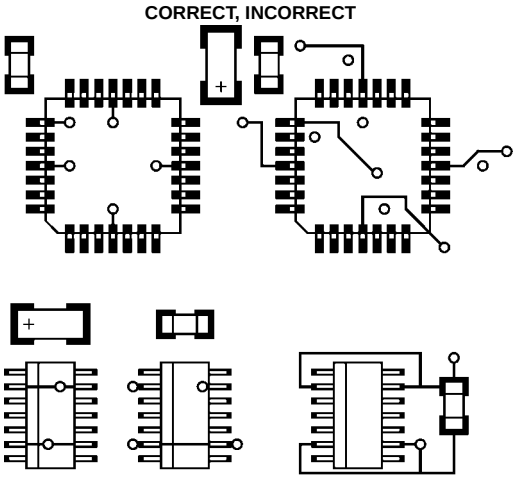

FIGURE 7. Power Pin Connection

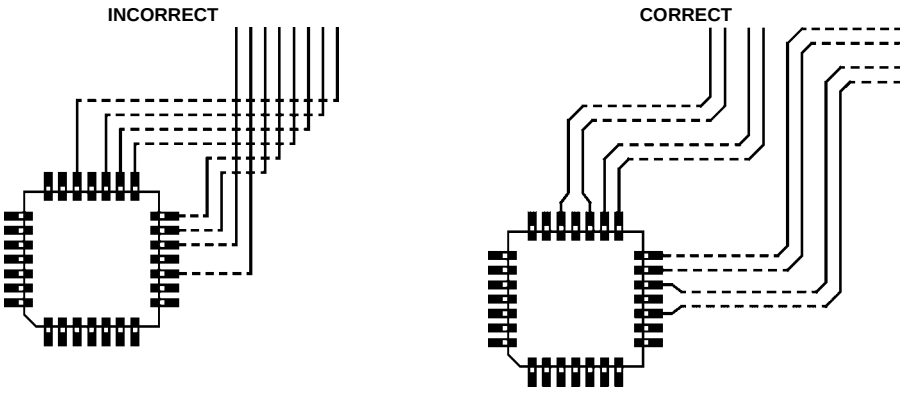

FIGURE 8. Differential Line Layout

AVOIDING SKEW TOLERANCE BUILD-UP

There are additional steps that can be taken to avoid skew build-up. Perhaps the simplest is to observe the rule of equal loading and termination. Briefly stated, all matching delay paths must be loaded equally, both resistively and reactively. Complementary outputs must have equal resistive termination values. Capacitive loading must be equal for both outputs, also. This is especially true of differential lines.

For example and using the delay value for 50Ω lines mentioned previously, a loading difference of 5 pF between the conductors of a differential line can result in a skew of 105 ps, or about one-fifth of a risetime. When combined with other effects like crosstalk and impedance discontinuities, significant skew can occur.

Path delay distribution is another step that can be taken to avoid skew build-up, Figure 9. This means that, if a clock distribution path must pass through several amplifiers, steps should be taken to assure that the signal does not use the same path, pin-wise, through all amplifiers. To illustrate, assume that the path passes through three F100311, 1:9 differential drivers. The input pins in all cases are 28 (in) and 2 (in/). If the first output pair is 25 (D0) and 24 (D0/), then choose pins 23 (D1) and 22 (D1/) for amplifier #2 and pins 20 (D2) and 19 (D2/) for the third amplifier. Additional variation can be achieved by reversing the input phase through each amplifier. Of course, the output phase must be similarly reversed to match the input. These points may seem minor, but all contribute to reducing the mathematical probability of skew tolerance build-up.

TESTING MINIMUM-SKEW CLOCK SYSTEMS

As with all types of electronic systems, the performance of minimum-skew circuits must be verifiable and testable. The very nature of these systems calls for more care and precision in testing than other types of logic systems. And, greater precision is required from the test equipment and its use.

Certainly the oscilloscope is the most frequently used piece of test equipment for logic systems. While it does provide much information about the quality of signals, it may be the cause of error if improperly applied. Perhaps the single largest error source and the least recognized is the place where scope and circuit meet, the probe. To do justice to the subject of probing and probes in pulse application would require a book unto itself. One very useful book from Tektronix is “ABC's of Probes”. In it are emphasized some essentials for choosing a suitable probe for the job. Some of these are:

- Compatibility with the scope system,
- Adequate bandwith and risetime capability exceeding that of the system to be tested,
- Low circuit loading, which implies low capacitance at the tip,
- High enough impedance so as to not unduly load the circuit being probed (This does not mean that FET probes are the best choice!),
- And delay matching when multiple probes are used for relative delay measurements.

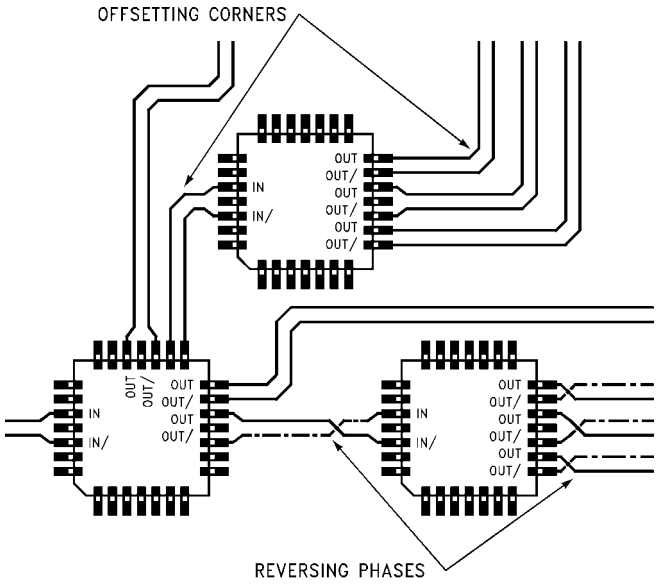

FIGURE 9. Avoiding Skew Tolerance Buildup

The choice of scope is equally important and the list of its basic features is similar to that for the probe. Where the precise nature of the signal to be measured is unknown, the analog scope may provide the most useful information initially. While it does not have all of the sophistication of digital scopes, it offers fewer complications and a fidelity that is hard to beat. The digital scope, especially if it has storage capability, can be an asset where comparison of signals taken at different times and places in the circuit is important.

Additional useful information on scopes and in-circuit measurements may be found in the series “Troubleshooting Analog Circuits” by Fairchild Semiconductor's Bob Pease in “EDN” and available as a reprint from Fairchild.

A final consideration and one that is often overlooked is the incorporation of test points in the circuit. The increasing

use of surface mount devices and dense layouts makes probing these circuits more difficult. Inclusion of test points or test connectors can ease the job considerably. Just remember to make sure that the test points do not corrupt the signals and are themselves designed for minimum-skew. Test points may even be provided by reserving one output of an ECL minimum-skew device at each critical point in the circuit. This provides isolation for the probe and minimal loading on the monitored circuit. And, of course it should go without saying that test points should be accessible without the need to mechanically or electrically alter normal operation of the equipment being tested.

APPENDIX

Available Literature

Application Notes

AN-467 — Surface Mount: From Design to Delivery

AN-468 — Wave Soldering of Surface Mount Components

AN-469 — Reliability of Small Outline Surface Mount Packages

AN-470 — Wave Soldering: Is SOIC Reliability Compromised?

Datasheets

113295-001 — Plastic Chip Carrier Technology

113615-001 — A Basic Guide to Surface Mounting of Electronic Components

Other Literature

570430-001 — Reliability Report Update Small Outline (SO) Package

570435-001 — Getting Started in Surface Mount

980040-001 — Reliability Report Update — Plastic Chip Carrier (PCC) Package

980045-001 — Reliability Report Update — Small Outline (SO) Package

980055-004 — Surface Mount Availability Guide

F100K ECL 100 Series to 300 Series Conversion Book

Troubleshooting Analog Circuits (EDN Article Series Reprint)

Databooks

400080 — Reliability Handbook

400028 — F100K ECL Logic Databook and Design Guide

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"Electronic Circuit Calculations Simplified, Part 5 - RC combinations in A.C. circuits", S.W. Amos; "Wireless World"; 10/1975; pp. 475–478