Features

- Fast 5V Read Access Time - 35 ns
- Command Table Architecture
  - Internal Program Control and Timer
- 12V Program and Erase
  - Fast Chip Erase Time - 0.5 Second Maximum
  - Word-by-word Programming - 20 µs/Word Typical
- Hardware Data Protection
- Low-power CMOS Operation
  - 100 µA Maximum Standby
  - 30 mA Maximum Active at 5 MHz
- JEDEC Standard Packages
  - 44-lead PLCC
  - 40-lead VSOP (10 mm x 14 mm)
- Pin-compatible with Atmel's AT27C1024 and AT49F1024/1025
- High-reliability CMOS Technology
  - 2000V ESD Protection
  - 200 mA Latchup Immunity
- CMOS and TTL Compatible Inputs and Outputs
- 100 Write Cycles Guaranteed

Description

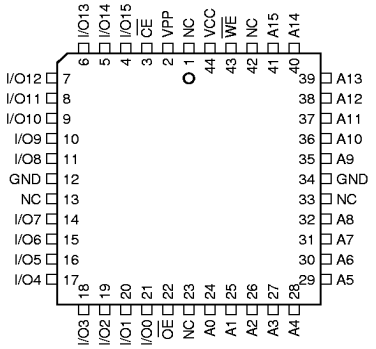
The AT27RW1024 is a low-power, high-performance 1,048,576-bit electrically-rewriteable programmable read-only memory (RWPROM) organized 64K x 16 bits. It requires only one 5V power supply in normal read mode operation. Any word can be accessed in less than 35 ns, eliminating the need for speed reducing WAIT states.

(continued)

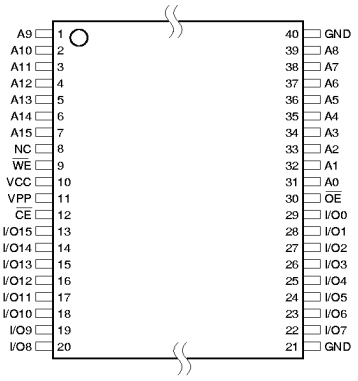
Pin Configurations

Pin Name	Function
A0 - A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O15	Data Inputs/Outputs
NC	No Connect

PLCC Top View



VSOP Type 1
10 x 14 mm



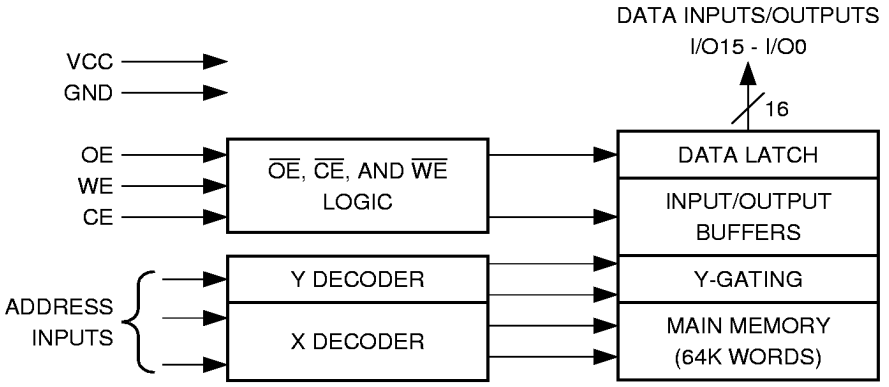
1-megabit (64K x 16) Rewriteable PROM

AT27RW1024

Rev. 1415A–06/99

The x16 organization makes this part ideal for high-performance 16- and 32-bit DSP and microprocessor systems. The AT27RW1024 is pin-compatible with Atmel's AT49F1024/1025 and AT27C1024. In read mode, the AT27RW1024 typically consumes 15 mA. Standby mode supply current is typically less than 10 µA. Reprogramming the AT27RW1024 is performed by erasing the entire chip and then programming on a word-by-word basis. The program and erase functions are performed with V_{CC} = 5V and V_{PP} = 12V. Programming time is 20 µs per word typical. 100 program and erase cycles are guaranteed.

Block Diagram



Device Operation

READ: When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

CHIP ERASE: The chip erase will erase all words to an FFFFH. The chip erase command is a six bus cycle operation. The address (5555H) is latched on the falling edge of the sixth cycle while the 10H data input is latched on the rising edge of $\overline{WE}$. The chip erase starts after the rising edge of $\overline{WE}$ of the sixth cycle. Please see "Chip Erase Cycle Waveforms" on page 7. The chip erase operation is internally controlled; it will automatically time to completion. After a chip erase, the device will return to the read mode. Chip erase requires V_{CC} = 5V and V_{PP} = 12V.

WORD PROGRAMMING: Once the memory array is erased, the device is programmed (to a logical "0") on a word-by-word basis. Please note that a data "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s. Programming is accomplished via the internal device command register and is a 4 bus cycle operation (please refer to the Command Definitions table). The device will automatically generate the required internal program pulses.

The program cycle has addresses latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last, and the data latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Programming is completed after the specified t_{BP} cycle time. Programming requires V_{PP} = 12V and V_{CC} = 5V.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT27RW1024 in the following ways: (a) V_{CC} sense: if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) Program inhibit: holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (c) Noise filter: Pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

Command Definition (in Hex)

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Word Program	4	5555	AA	2AAA	55	5555	A0	Addr	D_{IN}				
Product ID Entry	3	5555	AA	2AAA	55	5555	90						
Product ID Exit	1	xxxx	F0										

Note: The DATA FORMAT in each bus cycle is as follows: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex).

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT27RW1024-35	AT27RW1024-45	AT27RW1024-55	AT27RW1024-70
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	X(1)(7)	Ai	D_{OUT}
Program/Erase(2)	V_{IL}	V_{IH}	V_{IL}	V_{PP}	Ai	D_{IN}/X
Standby	V_{IH}	X(1)	X(1)	X(1)(7)	X(1)	High Z
Program/Erase Inhibit	V_{IL}	V_{IH}	V_{IL}	X(1)(7)	X(1)	
	X(1)	X(1)	V_{IH}	V_{PP}	X(1)	
Program/Erase Verify	X(1)	V_{IL}	X(1)	V_{PP}	Ai	D_{OUT}
Output Disable	X(1)	V_{IH}	X(1)	X(1)(7)		High Z
Product Identification						
Hardware	V_{IL}	V_{IL}	V_{IH}	X(4)	A1 - A15 = V_{IL}, A9 = V_H,(3) A0 = V_{IL}	Manufacturer Code(6)
				X(4)	A1 - A15 = V_{IL}, A9 = V_H,(3) A0 = V_{IH}	Device Code(6)
Software(5)				X(4)	A0 = V_{IL}, A1 - A15 = V_{IL}	Manufacturer Code(6)
				X(4)	A0 = V_{IH}, A1 - A15 = V_{IL}	Device Code(6)

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming and Erasing Waveforms.
3. V_H = 12.0V ± 0.5V.
4. X can be V_{CC} or V_{PP}.
5. See details under Software Product Identification Entry/Exit.
6. Manufacturer Code: 001EH, Device Code: 0051H.
7. For customers building field-upgradable systems, X can be 12.0V.

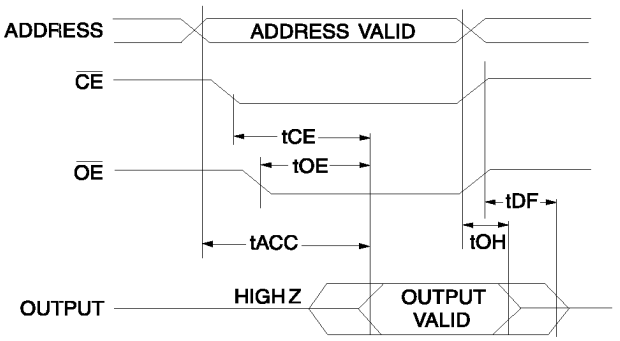
DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		30	mA
I_{PP}	Program or Erase Current	Word Program, Chip Erase in Progress		25	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V

AC Read Characteristics

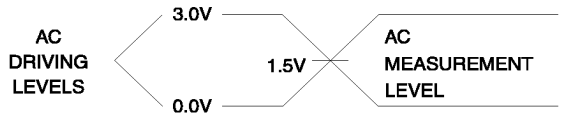
Symbol	Parameter	AT27RW1024-35		AT27RW1024-45		AT27RW1024-55		AT27RW1024-70		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		35		45		55		70	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		35		45		55		70	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	15		18		25		25	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	15		18	0	25		25	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	7		7		7		7		ns

AC Read Waveforms[1][2][3][4]



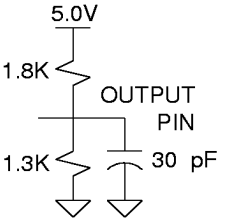
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

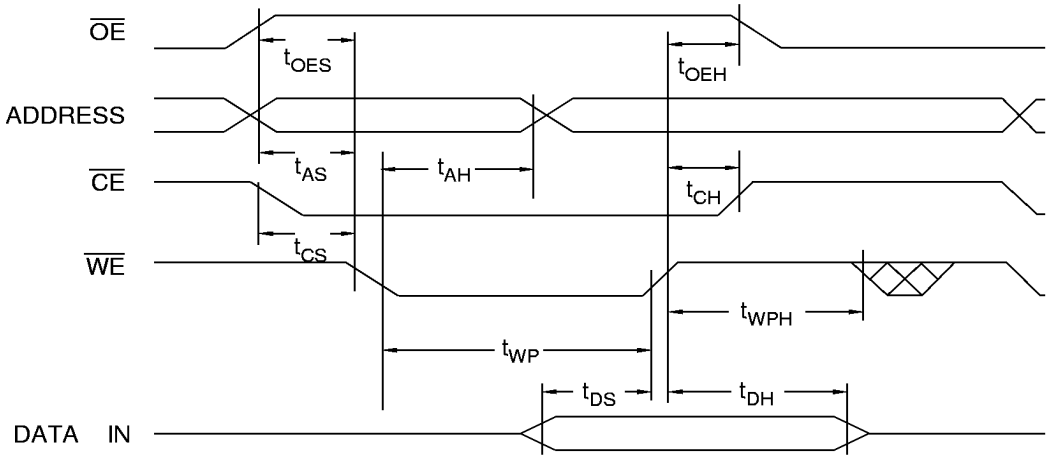
Note: 1. This parameter is characterized and is not 100% tested.

AC Word Load Characteristics

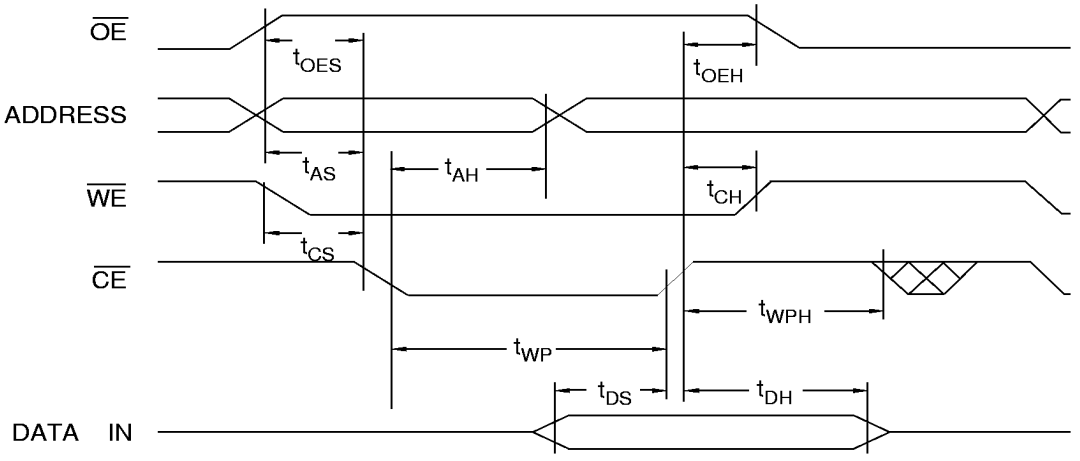
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	90		ns

AC Word Load Waveforms

$\overline{WE}$ Controlled



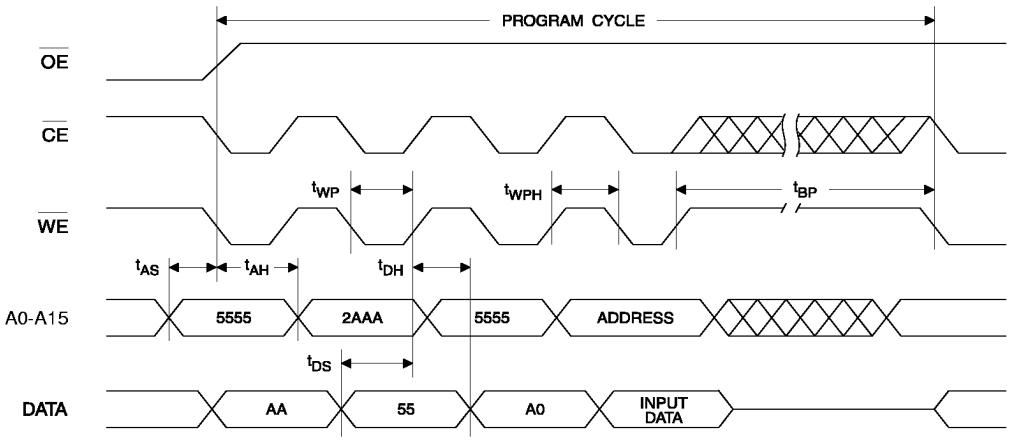
$\overline{CE}$ Controlled



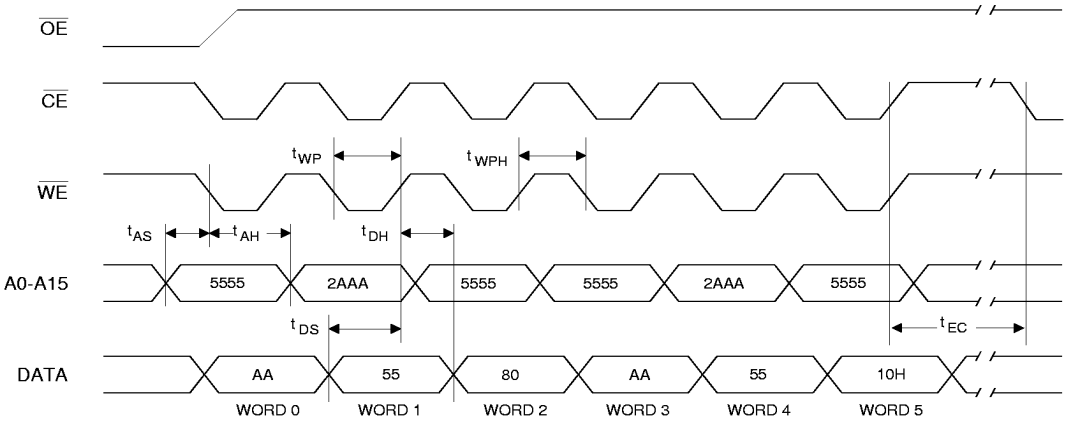
Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Word Programming Time		20	50	µs
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	90			ns
t_{WPH}	Write Pulse Width High	90			ns
t_{EC}	Erase Cycle Time			500	ms

Program Cycle Waveforms

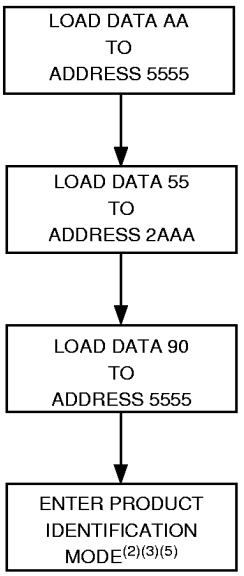


Chip Erase Cycle Waveforms

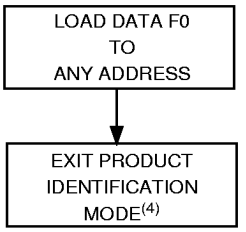


Notes: 1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Software Product Identification Entry[1]



Software Product Identification Exit[1]



Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A15 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 001EH
   Device Code: 0051H

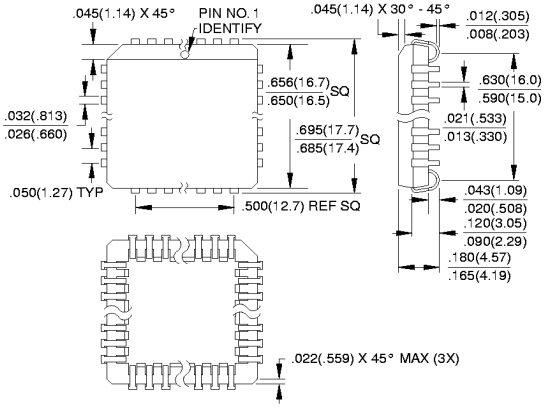
Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
35	30	0.1	AT27RW1024-35JC AT27RW1024-35VC	44J 40V	Commercial (0° to 70°C)
	30	0.1	AT27RW1024-35JI AT27RW1024-35VI	44J 40V	Industrial (-40° to 85°C)
45	30	0.1	AT27RW1024-45JC AT27RW1024-45VC	44J 40V	Commercial (0° to 70°C)
	30	0.1	AT27RW1024-45JI AT27RW1024-45VI	44J 40V	Industrial (-40° to 85°C)
55	30	0.1	AT27RW1024-55JC AT27RW1024-55VC	44J 40V	Commercial (0° to 70°C)
	30	0.1	AT27RW1024-55JI AT27RW1024-55VI	44J 40V	Industrial (-40° to 85°C)
70	30	0.1	AT27RW1024-70JC AT27RW1024-70VC	44J 40V	Commercial (0° to 70°C)
	30	0.1	AT27RW1024-70JI AT27RW1024-70VI	44J 40V	Industrial (-40° to 85°C)

Package Type	
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40V	40-lead, Thin Small Outline Package (VSOP) (10 mm x 14 mm)

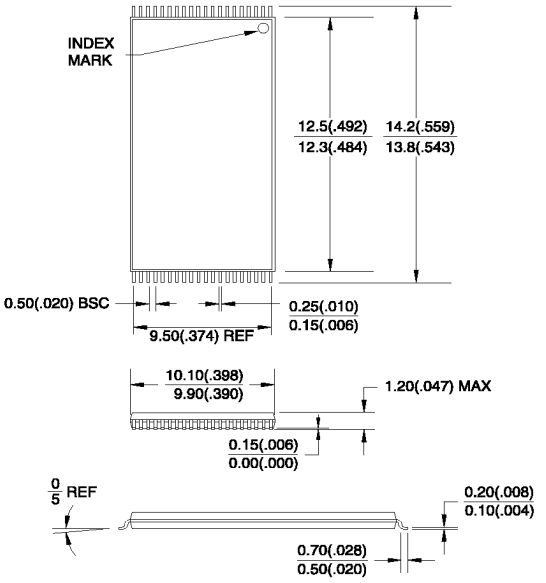
Packaging Information

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)*
JEDEC STANDARD MS-018 AC



*Controlling dimension: millimeters

40V, 40-lead, Plastic Thin Small Outline Package (VSOP)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters