CLEAR LOGIC

CL7096

Laser Processed Logic Device Family

Key Features

- Laser Processed Logic Device (LPLD™) technology offers the ultimate combination of performance, flexibility, and low cost
- Functionally, architecturally, and electrically compatible with industry-standard Altera® MAX® 7000™
- High Density
  - 1,800 Usable gates
  - 96 Macrocells
  - 76 Maximum user I/O pins
- Laser fuse technology provides very fast, dense interconnect routing
- Fabricated using 0.45 micron CMOS process
- Low current consumption
- 3.3 volt or 5.0 volt operation
- Alpha particle immune

CL7000 Product Family Overview

Parameter	CL7096	CL7128E CL7128S	CL7160E CL7160S	CL7192E CL7192S	CL7256E CL7256S
Useable Gates	1,800	2,500	3,200	3,750	5,000
Macrocells	96	128	160	192	256
Logic Blocks	6	8	10	12	16
Max user I/O pins	76	120	136	152	184
Packages	68 pin PLCC 84 pin PLCC 100 pin TQFP	84 pin PLCC 100 pin PQFP 100 pin TQFP 160 pin PQFP	84 pin PLCC 100 pin PQFP 100 pin TQFP 160 pin PQFP	160 pin PQFP	160 pin PQFP 208 pin PQFP 208 pin RQFP

Description

The Clear Logic CL7000 Laser Processed Logic Device (LPLD™) family offers the ultimate combination of performance, flexibility, and cost. This family is a system level second source to Altera MAX® 7000™, 7000E™, and 7000S™ products. For designs not requiring in-system reprogrammability, design verification can be performed using the programmable Altera devices, and Clear Logic LPLDs can be used for low cost, high volume production.

Clear Logic's innovative laser ASIC technology eliminates NRE costs, test vector development, ordering minimums and long lead times. No re-simulation or re-layout is required, as the device uses a cell-based, PLD-like architecture. Clear Logic's TestCell™ technology ensures complete test coverage through the use of specialized testing modes which are transparent to the user.

The Clear Logic CL7000 Laser Processed Logic Device family is based upon a large array of macrocells. Each macrocell contains a logic array with five product terms, a product-term select matrix, and a configurable register. A group of sixteen macrocells forms a block. Laser-configured metal fuses implement logical functions and control signal routing.

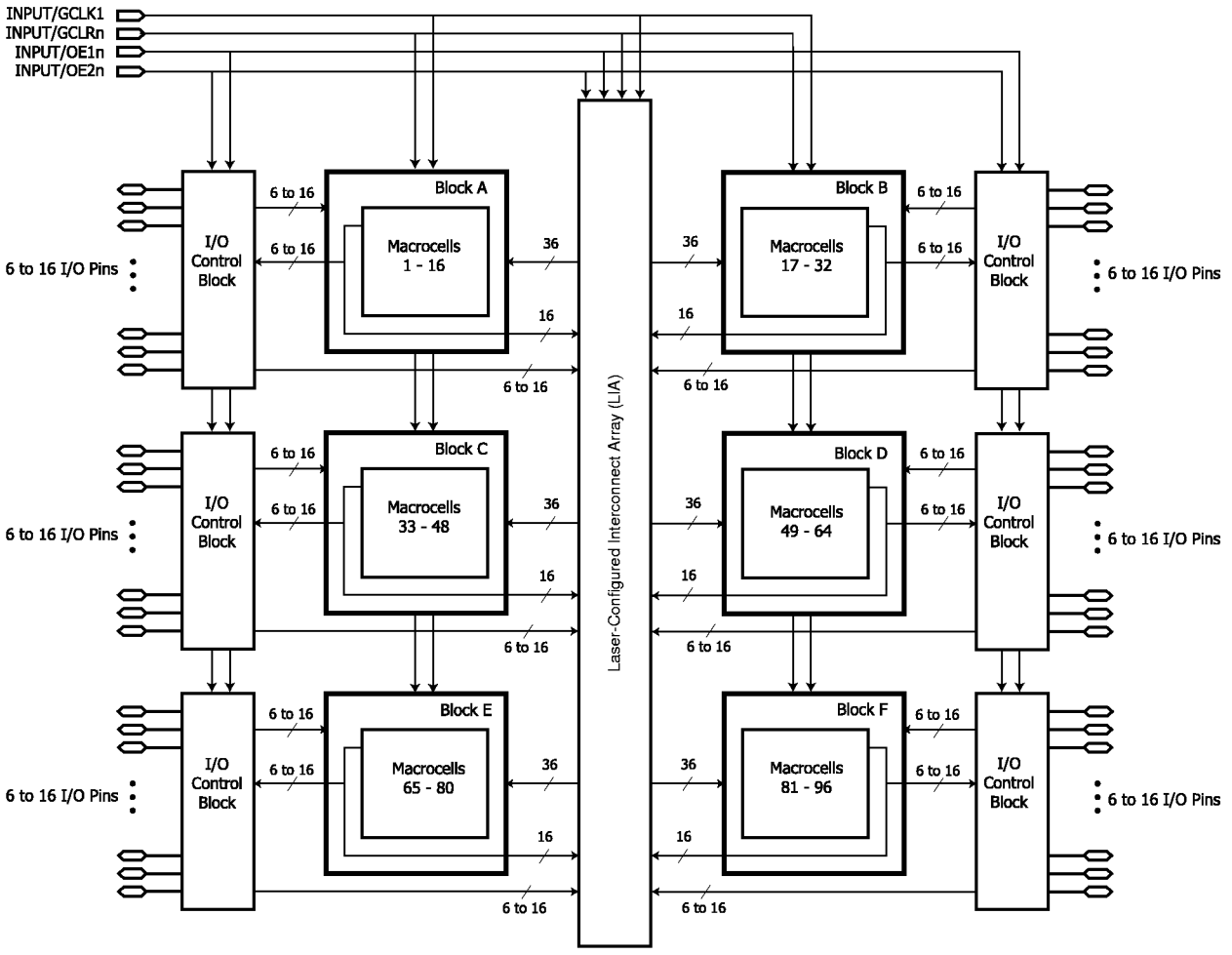
Laser configuration provides reduced cost and enhanced performance. These inherent performance benefits include extremely consistent propagation delays, reduced power consumption, and improved immunity to noise and upset events.

Additional Information

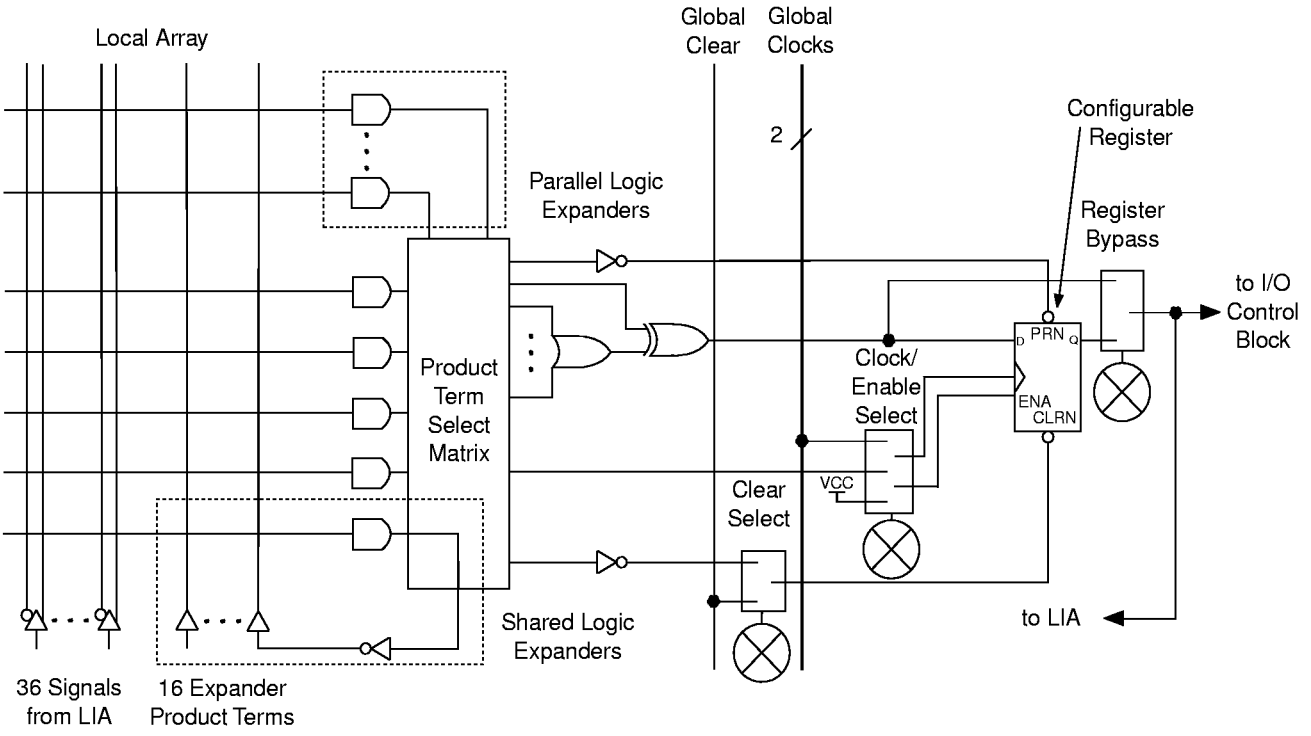
For further information on designing with the CL7000 LPLD family, please consult the following documents:

- *CL7K01: CL7000 Packaging Guide*. This document provides specifications and drawings for packages used by the CL7000 family.
- *CL7K02: CL7000 Technology White Paper*. This document outlines the technologies employed by the CL7000 LPLD family.
- *CL7K03: Requesting a CL7000 First Article*. This document provides instructions on how to submit a bitstream file for generation of first articles.
- *CL7K04: Calculating CL7000 Power Consumption*. This document provides guidelines for calculating power consumption based on design characteristics.

Block Diagram



Macrocell Diagram



Pin Configuration

Pin Name	68 pin PLCC	84 pin PLCC	100 pin PQFP
INPUT/GCLK1	67	83	89
INPUT/GCLRn	1	1	91
INPUT/OE1	68	84	90
INPUT/OE2/GCLK2	2	2	92
GND	6, 16, 26, 34, 38, 48, 58, 66	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97
VCCINT	3, 35	3, 43	41, 93
VCCIO	11, 21, 31, 43, 53, 63	13, 26, 38, 53, 66, 78	5, 20, 36, 53, 68, 84
NC (No Connect)	-	6, 39, 46, 79	9, 24, 37, 44, 57, 72, 85, 96
Total user I/O pins	48	60	72

DC Electrical Specifications

Recommended Operating Conditions[2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage, internal logic and input buffers Commercial Grade Devices Industrial Grade Devices		 4.75 4.50	 5.25 5.50	V
V_{CCIO}	DC input voltage 5.0 volt commercial 5.0 volt industrial 3.3 volt operation		 4.75 4.50 3.00	 5.25 5.50 3.60	V
V_I	Input voltage		0	V_{CCINT}	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Operating temperature Commercial temperature range Industrial temperature range		 0 -40	 70 85	°C
t_R	Input signal rise time			40	ns
t_F	Input signal fall time			40	ns
t_{RVCC}	V_{CC} rise time			100	ms

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		-2.0	7.0	V
V_I	DC input voltage [1]		-2.0	7.0	V
I_{OUT}	DC output current, per pin		-25	25	mA
T_{STG}	Storage temperature	No bias	-65	150	°C
T_{AMB}	Ambient temperature	Under bias	-65	135	°C
T_J	Junction temperature	Under bias		135	°C

DC Electrical Characteristics (over the operating range)

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		-0.3		0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = 0.1 mA	V_{CC}-0.2			V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.45	V
I_{IN}	Input Leakage Current	V_I = V_{CC} or GND	-10		10	µA
I_{OZ}	Output Leakage Current	V_I = V_{CC} or GND	-40		40	µA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

AC Electrical Specifications

External Timing Parameters

			speed: -7		speed: -10		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Unit
t_{PD1}	Input to non-registered output	C_L = 35 pF		7.5		10	ns
t_{PD2}	I/O input to non-registered output	C_L = 35 pF		7.5		10	ns
t_{SU}	Global clock setup time		6		8		ns
t_H	Global clock hold time		0		0		ns
t_{FSU}	Global clock setup time of fast input		3		3		ns
t_{FH}	Global clock hold time of fast input		0.5		0.5		ns
t_{CO1}	Global clock to output delay	C_L = 35 pF		4.5		5	ns
t_{CH}	Global clock high time		3		4		ns
t_{CL}	Global clock low time		3		4		ns
t_{ASU}	Array clock setup time		3		3		ns
t_{AH}	Array clock hold time		2		3		ns
t_{ACO1}	Array clock to output delay	C_L = 35 pF		7.5		10	ns
t_{ACH}	Array clock high time		3		4		ns
t_{ACL}	Array clock low time		3		4		ns
t_{ODH}	Output data hold time after clock	C_L = 35 pF	1		1		ns
t_{CNT}	Minimum global clock period			8		10	ns
f_{CNT}	Maximum internal global clock frequency		125		100		MHz
t_{ACNT}	Minimum array clock period			8		10	ns
f_{ACNT}	Maximum internal array clock frequency		125		100		MHz

External Timing Parameters

			speed: -12		speed: -15		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Unit
t_{PD1}	Input to non-registered output	C_L = 35 pF		12		15	ns
t_{PD2}	I/O input to non-registered output	C_L = 35 pF		12		15	ns
t_{SU}	Global clock setup time		10		11		ns
t_H	Global clock hold time		0		0		ns
t_{FSU}	Global clock setup time of fast input		3		3		ns
t_{FH}	Global clock hold time of fast input		0		0		ns
t_{CO1}	Global clock to output delay	C_L = 35 pF		6		8	ns
t_{CH}	Global clock high time		4		5		ns
t_{CL}	Global clock low time		4		5		ns
t_{ASU}	Array clock setup time		4		4		ns
t_{AH}	Array clock hold time		4		4		ns
t_{ACO1}	Array clock to output delay	C_L = 35 pF		12		15	ns
t_{ACH}	Array clock high time		5		6		ns
t_{ACL}	Array clock low time		5		6		ns
t_{ODH}	Output data hold time after clock	C_L = 35 pF	1		1		ns
t_{CNT}	Minimum global clock period			11		13	ns
f_{CNT}	Maximum internal global clock frequency		90.9		76.9		MHz
t_{ACNT}	Minimum array clock period			11		13	ns
f_{ACNT}	Maximum internal array clock frequency		90.9		76.9		MHz

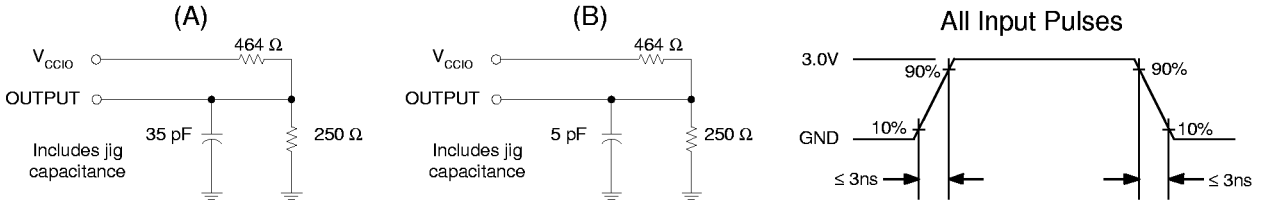
Internal Timing Parameters [4]

			speed: -7		speed: -10		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Unit
t_{IN}	Input pad and buffer delay			0.5		1	ns
t_{IO}	I/O input pad and buffer delay			0.5		1	ns
t_{FIN}	Fast input delay			1		1	ns
t_{SEXP}	Shared expander delay			4		5	ns
t_{PEXP}	Parallel expander delay			0.8		0.8	ns
t_{LAD}	Logic array delay			3		5	ns
t_{LAC}	Logic control array delay			3		5	ns
t_{IOE}	Internal output enable delay			2		2	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 5.0 V	C_L = 35 pF		2		2	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 3.3 V	C_L = 35 pF		2.5		2.5	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C_L = 35 pF		7		6	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off, V_{CCIO} = 5.0 V	C_L = 35 pF		4		5	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off, V_{CCIO} = 3.3 V	C_L = 35 pF		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C_L = 35 pF		9		9	ns
t_{XZ}	Output buffer disable delay	C_L = 35 pF		4		5	ns
t_{SU}	Register setup time		3		3		ns
t_{H}	Register hold time		2		3		ns
t_{FSU}	Register setup time of fast input		3		3		ns
t_{FH}	Register hold time of fast input		0.5		0.5		ns
t_{RD}	Register delay			1		1	ns
t_{COMB}	Combinatorial delay			1		1	ns
t_{IC}	Array clock delay			3		5	ns
t_{EN}	Register enable time			3		5	ns
t_{GLOB}	Global control delay			1		1	ns
t_{PRE}	Register preset time			2		3	ns
t_{CLR}	Register clear time			2		3	ns
t_{LIA}	LIA delay			1		1	ns

Internal Timing Parameters [4]

			speed: -12		speed: -15		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Unit
t_{IN}	Input pad and buffer delay			2		2	ns
t_{IO}	I/O input pad and buffer delay			2		2	ns
t_{FIN}	Fast input delay			1		2	ns
t_{SEXP}	Shared expander delay			7		8	ns
t_{PEXP}	Parallel expander delay			1		1	ns
t_{LAD}	Logic array delay			5		6	ns
t_{LAC}	Logic control array delay			5		6	ns
t_{IOE}	Internal output enable delay			2		3	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 5.0 V	C_L = 35 pF		3		4	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 3.3 V	C_L = 35 pF		4		5	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C_L = 35 pF		7		8	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off, V_{CCIO} = 5.0 V	C_L = 35 pF		6		6	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off, V_{CCIO} = 3.3 V	C_L = 35 pF		7		7	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C_L = 35 pF		10		10	ns
t_{XZ}	Output buffer disable delay	C_L = 35 pF		6		6	ns
t_{SU}	Register setup time		4		4		ns
t_{H}	Register hold time		4		4		ns
t_{FSU}	Register setup time of fast input		2		2		ns
t_{FH}	Register hold time of fast input		2		2		ns
t_{RD}	Register delay			1		1	ns
t_{COMB}	Combinatorial delay			1		1	ns
t_{IC}	Array clock delay			5		6	ns
t_{EN}	Register enable time			5		6	ns
t_{GLOB}	Global control delay			0		1	ns
t_{PRE}	Register preset time			3		4	ns
t_{CLR}	Register clear time			3		4	ns
t_{LIA}	LIA delay			1		2	ns

AC Test Conditions



Notes to Tables

1. During transitions, inputs may undershoot to -2.0v for periods shorter than 20ns. Otherwise, minimum DC input voltage is 0.3v.

2. Typical values are at V_{CC} of 5.0 volts and ambient temperature of 25 °C.

3. Guaranteed but not tested. Characterized initially, and after any design changes which may affect these parameters.

4. Internal timing delays are based on characterization, and cannot be explicitly tested. Internal timing parameters should be used for performance estimation only.

Ordering Information

Part Number	Temperature Range	Package Type	Speed	Altera Equivalent
CL7096LC68-15	Commercial	68-pin Plastic LCC	-15	EPM7096LC68-15
CL7096LC68-12			-12	EPM7096LC68-12
CL7096LC68-10			-10	EPM7096LC68-10
CL7096LC68-7			-7	EPM7096LC68-7
CL7096LI68-15	Industrial		-15	EPM7096LI68-15
CL7096LC84-15	Commercial	84-pin Plastic LCC	-15	EPM7096LC84-15
CL7096LC84-12			-12	EPM7096LC84-12
CL7096LC84-10			-10	EPM7096LC84-10
CL7096LC84-7			-7	EPM7096LC84-7
CL7096LI84-15	Industrial		-15	EPM7096LI84-15
CL7096QC100-15	Commercial	100-pin Plastic QFP	-15	EPM7096QC100-15
CL7096QC100-12			-12	EPM7096QC100-12
CL7096QC100-10			-10	EPM7096QC100-10
CL7096QC100-7			-7	EPM7096QC100-7
CL7096QI100-15	Industrial		-15	EPM7096QI100-15

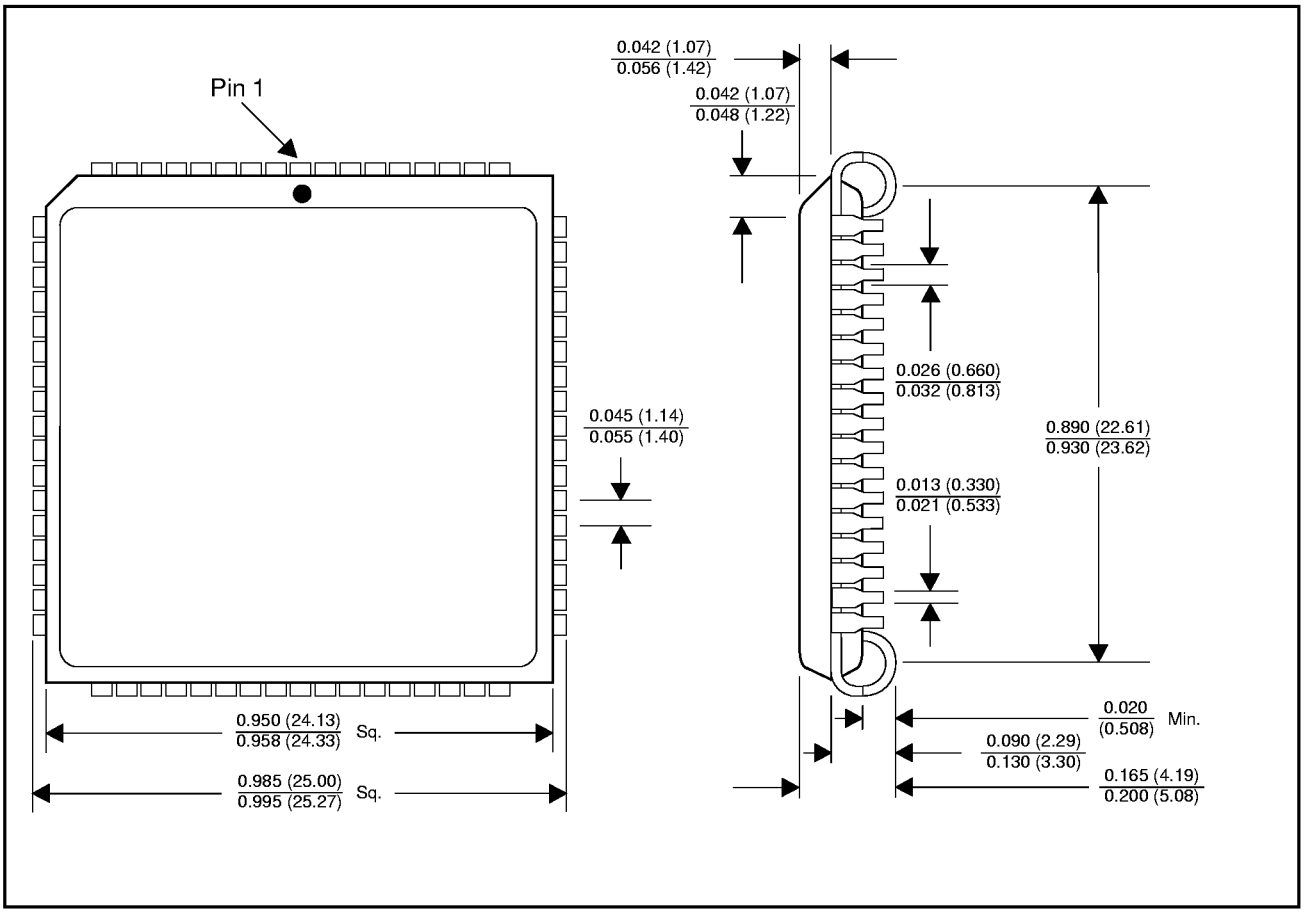
CL7000 PACKAGING GUIDE

Introduction

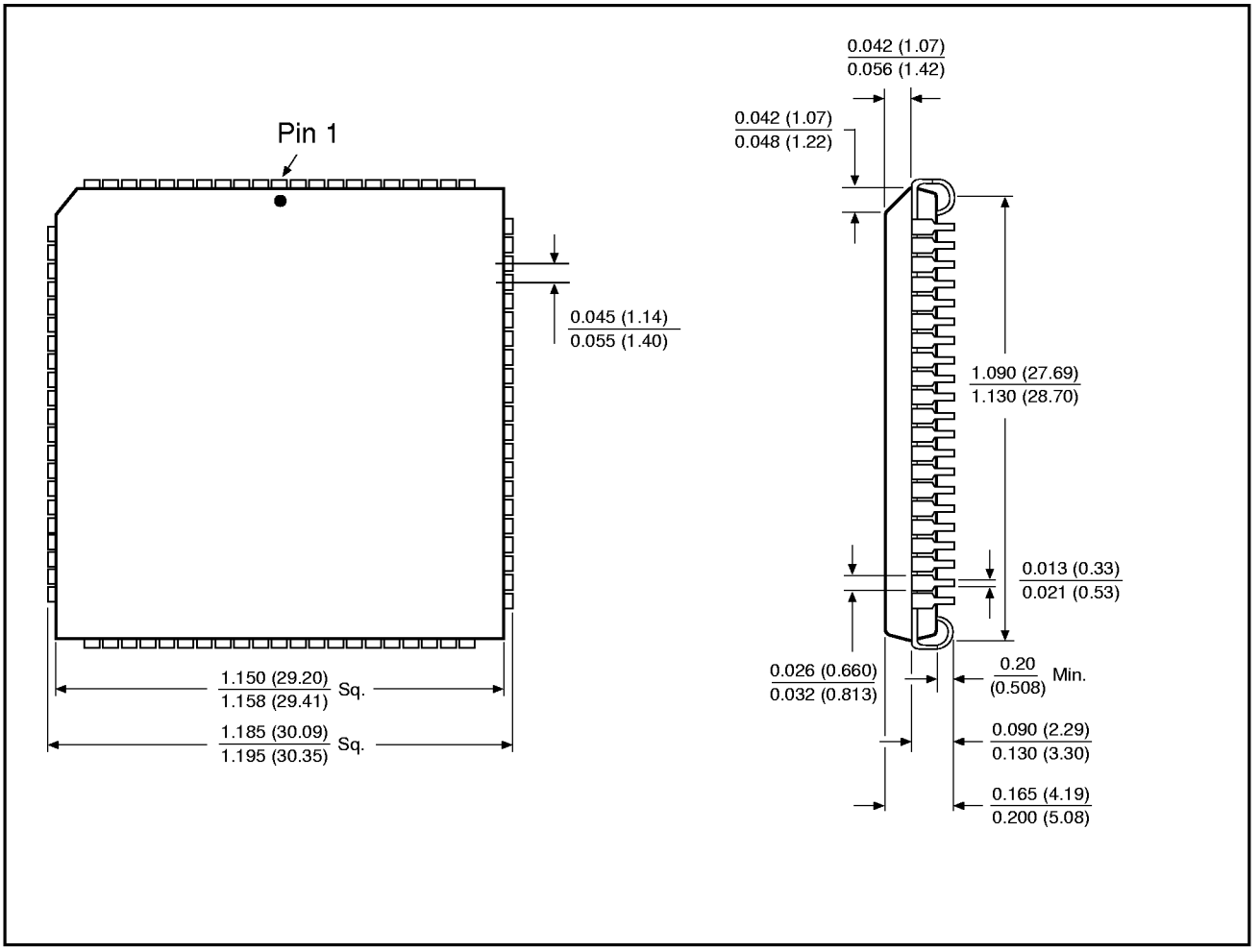
This document will provide you with package outlines for all available CL7000 packages. It also provides information regarding lead finish and package mass.

Package Outlines

LC68: 68-Pin Plastic Leaded Chip Carrier (PLCC)



LC84: 84-Pin Plastic Leaded Chip Carrier (PLCC)



QC100: 100-Pin Plastic Quad Flat Pack (PQFP)