## ATA Flash card

WEDC ATA10 Series (ATA10) flash memory cards are ATA compatible cards and are suitable for usage as a data storage memory medium for PC's or any other electronic equipment.

Packaged in a PCMCIA type I or type II housing, the WEDC ATA series cards provide a lightweight, low power, reliable nonvolatile storage medium.

Built in to the card controller, Error Correcting Code (ECC) provides a high level of reliability and MTBF (Mean Time Between Failures)

WEDC's standard cards are shipped with the WEDC FLASH Logo. Cards are also available with blank housings (no Logo). The blank housings are available in both a recessed (for label) and flat housing. Please contact your WEDC sales representative for further information on Custom artwork.

## Features

• PC Card ATA compatible
- 68 pin two piece connector and type I or type II housing (5mm)
- PCMCIA/JEIDA 4.1

• x8/x16 PCMCIA standard interface

• Single 3 Volt / 5 Volt Supply

• ISA standard, Read/Write unit is 1 sector (512 bytes)
- Sector Read/Write transfer rate: 8 MB/s burst
- High reliability based on internal ECC function (Error Correcting Code) and wear leveling functions.

• Card Capacity
- 8 MB to 512 MB (unformatted)

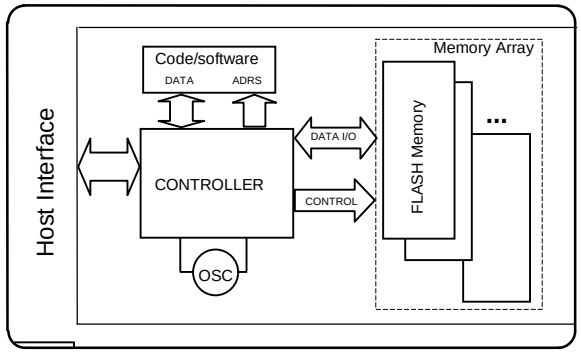
• Card Access mode:
- Memory card mode
- I/O card mode
- True-IDE mode

• Data Write Endurance is 100k program/erase cycles

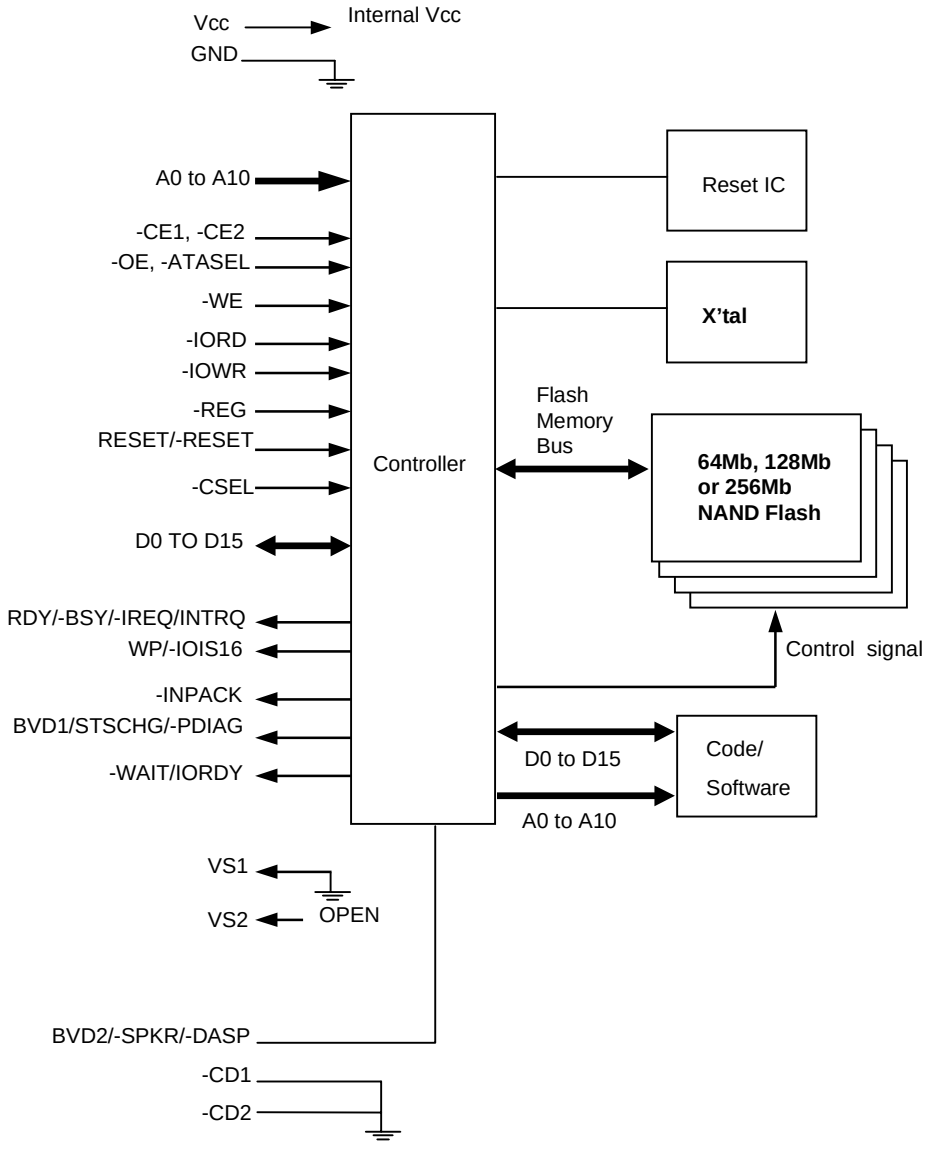
• Data reliability is 1 error in $10^{14}$ bits read

• Auto Sleep Function

## Block Diagram

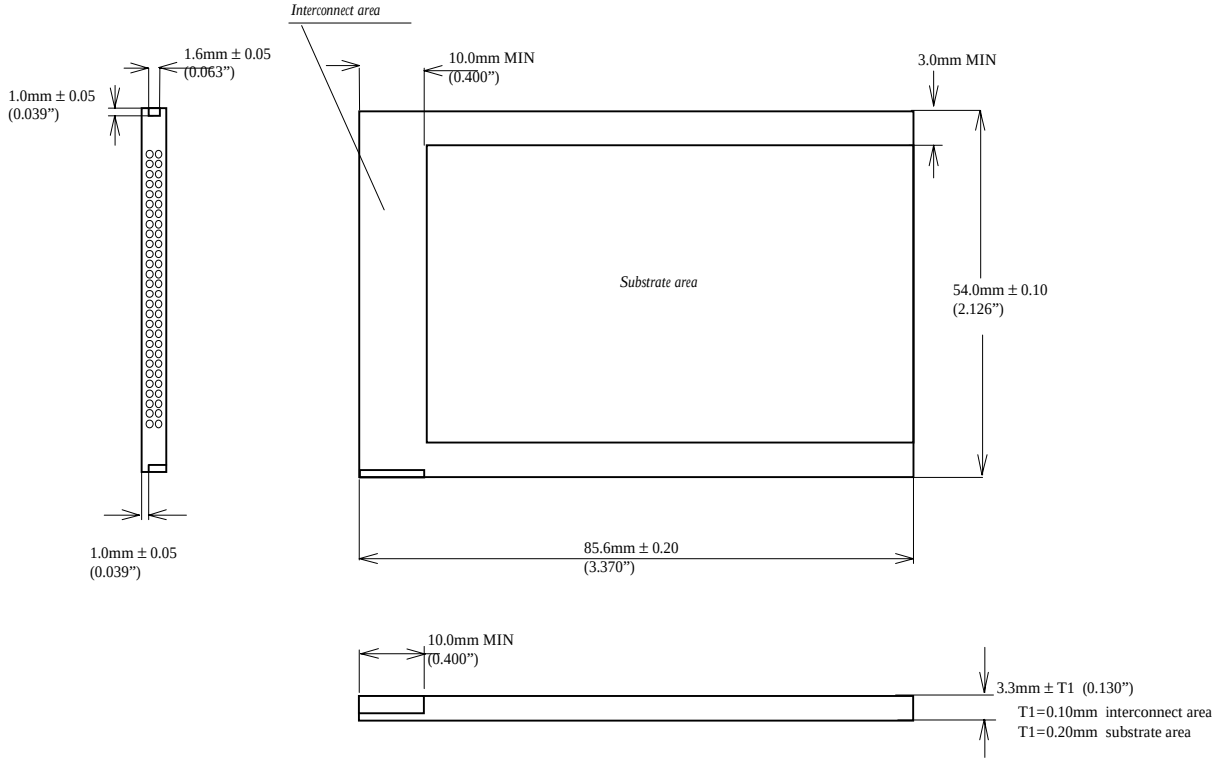


## Block Diagram

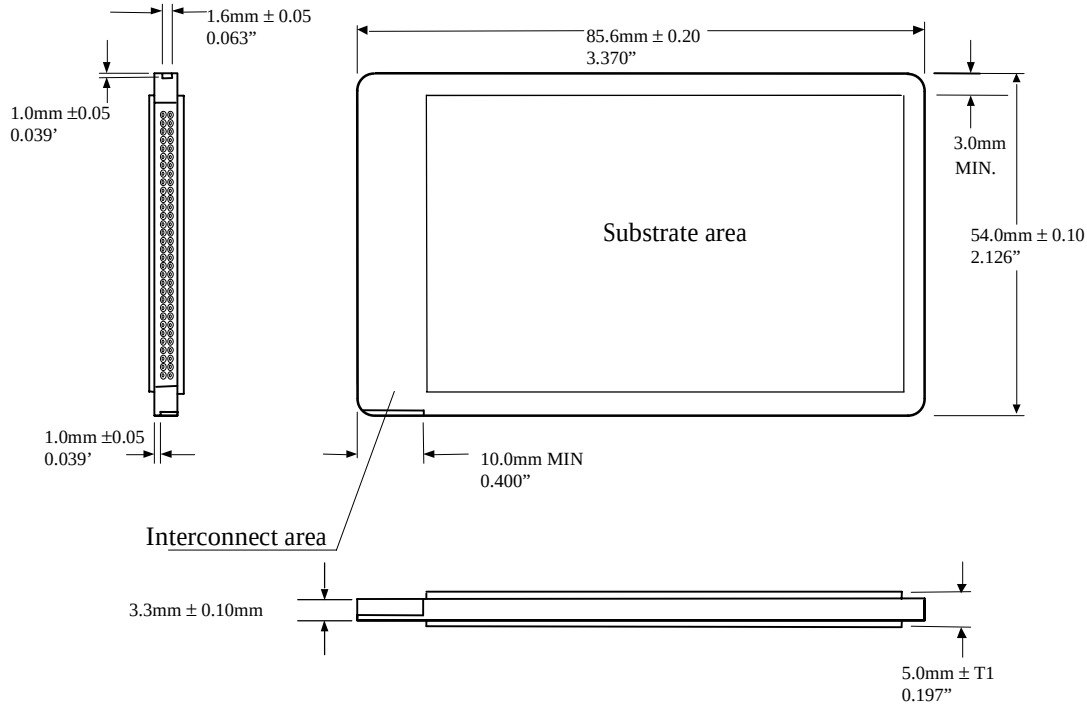


## Mechanical

Type I




Type II



## Card Capacity

Because of card formatting, user available capacity is smaller than the original memory size. The table below presents the relation between card capacity and formatted capacity.

**Note:** Other capacities are available: contact your company sales representative for details.

| Card type | Capacity | Formatted Capacity |
|---|---|---|
| 7P008ATA1003C25 | 8MB | 7.38MB |
| 7P016ATA1003C25 | 16MB | 15.42MB |
| 7P032ATA1003C25 | 32MB | 30.88MB |
| 7P048ATA1003C25 | 48MB | 47.23MB |
| 7P064ATA1003C25 | 64MB | 63.07MB |
| 7P080ATA1003C25 | 80MB | 76.00MB |
| 7P096ATA1003C25 | 96MB | 91.20MB |
| 7P112ATA1003C25 | 112MB | 106.40MB |
| 7P128ATA1003C25 | 128MB | 121.60MB |
| 7P192ATA1003C25 | 192MB | 183MB |
| 7P256ATA1003C25 | 256MB | 244MB |

## System Performance

| Item | Performance |
|---|---|
| Data transfer rate | 8.0 MB/s burst |
| | 1.0 MB/s sustained read |
| | 600 kB/s sustained write |
| Data reliability | recoverable error in 10^14 bits read. |
| Start up time (Sleep to Idle) | 2ms (max) |
| Start up time (Reset to Ready) | 50ms (typ) |

Card controller provides PCMCIA compatibility.

Card supports fast ATA host to buffer burst transfer rates up to 20MB/s (with PIO mode 4) and fast transfer rate to/from flash memory up to 8MB/s

## Absolute Maximum Ratings (1)

| | |
|---|---|
| Operating Temperature TA (ambient) | |
| Commercial | 0°C to +60 °C |
| Industrial | -40°C to +85 °C |
| Storage Temperature | |
| Commercial | -20°C to +85 °C |
| Industrial | -40°C to +85 °C |
| Voltage on any pin relative to VSS | -0.5V to VCC+0.5V (1) |
| VCC supply Voltage relative to VSS | -0.5V to +7.0V |

**Note:**
(1) Stress greater than those listed under "Absolute Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended DC Operating Conditions

| Parameter | Symbol | Min | | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Operating temp | Ta | 0 | 25 | 60 | C | |
| Vcc voltage | Vcc | 4.5 | 5 | 5.5 | V | |

## DC Characteristics (1)

CMOS Test Conditions: VIL = VSS ± 0.2V, VIH = VCC ± 0.2V

| Symbol | Parameter | Notes | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| Vcc | Power Supply Voltage | | 4.5V | | 5.5V | | |
| ICC1 | Sector READ current | 2 | | 50 | | mA | CMOS level |
| ICC2 | Sector WRITE current | 2 | | 50 | | mA | CMOS level |
| ICCS | VCC Sleep/Standby Current | 1, 2 | | 0.5 | | mA | Control Signals = VCC |
| ILI | Input Leakage Current | 1, 3 | | | ±20 | µA | VCC = VCCMAX<br>Vin =VCC or VSS |
| ILO | Output Leakage Current | | | | ±20 | µA | VCC = VCCMAX<br>Vout =VCC or VSS |
| VIL | Input Low Voltage | | | | 0.8 | V | |
| VIH | Input High Voltage | | 2.0 | | | V | |
| VOL | Output Low Voltage | | | | 0.4 | V | IOL = 3.2mA |
| VOH | Output High Voltage | | 2.4 | | | V | IOH = -2.0mA |

**Notes:**
1. Control Signals: $CE_1$#, $CE_2$#, OE#, WE#, REG#, IORD#, IOWR#.
2. Typical: VCC = 5V, T = +25C.
3. Exceptions: Leakage currents on control signals will be < 500 µA when VIN = GND due to internal pull-up resistors.

## Pinout

| | Memory card mode | | I/O Card Mode | | True IDE Mode | |
|---|---|---|---|---|---|---|
| Pin Number | Signal Name | I/O | Signal Name | I/O | Signal Name | I/O |
| 1 | GND | | GND | | GND | |
| 2 | D3 | I/O | D3 | I/O | D3 | I/O |
| 3 | D4 | I/O | D4 | I/O | D4 | I/O |
| 4 | D5 | I/O | D5 | I/O | D5 | I/O |
| 5 | D6 | I/O | D6 | I/O | D6 | I/O |
| 6 | D7 | I/O | D7 | I/O | D7 | I/O |
| 7 | CE1# | I | CE1# | I | CE1# | I |
| 8 | A10 | I | A10 | I | A10 | I |
| 9 | OE# | I | OE# | I | ATASEL# | I |
| 10 | N.C. | - | N.C. | - | N.C. | - |
| 11 | A9 | I | A9 | I | A9 | I |
| 12 | A8 | I | A8 | I | A8 | I |
| 13 | N.C. | - | N.C. | - | N.C. | - |
| 14 | N.C. | - | N.C. | - | N.C. | - |
| 15 | WE# | I | WE# | I | WE# | I |
| 16 | RDY/BSY | O | IREQ# | O | INTRQ | O |
| 17 | Vcc | | Vcc | | Vcc | |
| 18 | N.C. | - | N.C. | - | N.C. | - |
| 19 | N.C. | - | N.C. | - | N.C. | - |
| 20 | N.C. | - | N.C. | - | N.C. | - |
| 21 | N.C. | - | N.C. | - | N.C. | - |
| 22 | A7 | I | A7 | I | A7 | I |
| 23 | A6 | I | A6 | I | A6 | I |
| 24 | A5 | I | A5 | I | A5 | I |
| 25 | A4 | I | A4 | I | A4 | I |
| 26 | A3 | I | A3 | I | A3 | I |
| 27 | A2 | I | A2 | I | A2 | I |
| 28 | A1 | I | A1 | I | A1 | I |
| 29 | A0 | I | A0 | I | A0 | I |
| 30 | D0 | I/O | D0 | I/O | D0 | I/O |
| 31 | D1 | I/O | D1 | I/O | D1 | I/O |
| 32 | D2 | I/O | D2 | I/O | D2 | I/O |
| 33 | WP | O | IOIS16# | O | IOIS16# | O |
| 34 | GND | | GND | | GND | |

## Pinout (Cont.)

| | Memory card mode | | I/O Card Mode | | True IDE Mode | |
|---|---|---|---|---|---|---|
| Pin Number | Signal Name | I/O | Signal Name | I/O | Signal Name | I/O |
| 35 | GND | | GND | | GND | |
| 36 | CD1# | O | CD1# | O | CD1# | O |
| 37 | D11 | I/O | D11 | I/O | D11 | I/O |
| 38 | D12 | I/O | D12 | I/O | D12 | I/O |
| 39 | D13 | I/O | D13 | I/O | D13 | I/O |
| 40 | D14 | I/O | D14 | I/O | D14 | I/O |
| 41 | D15 | I | D15 | I | D15 | I |
| 42 | CE2# | I | CE2# | I | CE2# | I |
| 43 | VS1 | O | VS1 | O | VS1 | O |
| 44 | IORD# | I | IORD# | I | IORD# | I |
| 45 | IOWR# | I | IOWR# | I | IOWR# | I |
| 46 | NC | - | NC | - | NC | - |
| 47 | NC | - | NC | - | NC | - |
| 48 | NC | - | NC | - | NC | - |
| 49 | NC | - | NC | - | NC | - |
| 50 | NC | - | NC | - | NC | - |
| 51 | Vcc | | Vcc | | Vcc | |
| 52 | NC | - | NC | - | NC | - |
| 53 | NC | - | NC | - | NC | - |
| 54 | NC | - | NC | - | NC | - |
| 55 | NC | - | NC | - | NC | - |
| 56 | CSEL# | I | CSEL# | I | CSEL# | I |
| 57 | VS2 | O | VS2 | O | VS2 | O |
| 58 | RESET | I | RESET | I | RESET# | I |
| 59 | Wait# | O | Wait# | O | IORDY | O |
| 60 | INPACK# | O | INPACK# | O | INPACK# | O |
| 61 | REG# | I | REG# | I | REG# | I |
| 62 | BVD2 | I/O | SPKR# | I/O | DASP | I/O |
| 63 | BVD1 | I/O | STSCHG# | I/O | PDIAG# | I/O |
| 64 | D8 | I/O | D8 | I/O | D8 | I/O |
| 65 | D9 | I/O | D9 | I/O | D9 | I/O |
| 66 | D10 | O | D10 | O | D10 | O |
| 67 | CD2# | O | CD2# | O | CD2# | O |
| 68 | GND | | GND | | GND | |

**Note:** CD1# and CD2# are grounded internal to PC Card.

## Card Signal Description

| Symbol | Type | Name and Function |
|---|---|---|
| A0 – A10 | INPUT | **ADDRESS INPUTS:** A0 through A10 Signal A0 is not used in word access mode. A10 is the most significant bit. In True IDE Mode only HA[2..0] are used for selecting the eight registers in the Task File, the remaining address lines should be grounded. |
| D0 - D15 | INPUT/OUTPUT | **DATA INPUT/OUTPUT:** D0 THROUGH D15 constitute the bi-directional databus. D0 - D7 constitute the lower (even) byte and D8 - D15 the upper (odd) byte. D15 is the MSB. |
| CE1#, CE2# | INPUT | **CARD ENABLE 1 AND 2:** active low signals; CE1# enables even byte accesses, CE2# enables odd byte accesses. In True IDE Mode CE2# is used to select the Alternate Status Register and the Device control Register while CE1# is the cheap select for the other task file registers. |
| OE#,<br>ASTEL# | INPUT | **OUTPUT ENABLE, ATA Select:** Active low signal enabling read data from Attribute and Common memory area. To enable True IDE Mode this input should be grounded by the host. |
| WE# | INPUT | **WRITE ENABLE:** Active low signal gating write data to the memory card. In true IDE Mode this input signal is not used and should be connected to Vcc. |
| RDY/BSY#<br>IREQ#<br>INTRQ | OUTPUT | **Ready/Busy, Interrupt Request:** In I/O mode this signal is is IREQ# pin. The signal of low level indicates that the card is requesting software service to host, and high level indicate that the card is not requesting. In memory mode, the signal is set high when the ATA card is ready to accept new data transfer operation and held low when card is busy.<br>At power up and at Reset, the RDY/BSY is low until (busy) until the card has completed its power up or reset function.<br>Host should provide a pull up resistor |
| CD1#, CD2# | OUTPUT | **CARD DETECT 1 and 2:** Provide card insertion detection. These signals are connected to ground internally on the memory card. The host socket interface circuitry shall supply 10K-ohm or larger pull-up resistors on these signal pins. |
| WP<br>IOIS16# | OUTPUT | **Write Protect, 16 bit I/O port:** In memory mode, WP is held low: always writable). In I/O mode , IOIS16# is asserted low when Task File Registers are accessed in 16 bit mode. In True IDE mOde this signal is asserted low when this device is expecting a word data transfer cycle. |
| VPP1, VPP2 | N.C. | **PROGRAM/ERASE POWER SUPPLY:** No Connection for ATA card. |
| VCC | | **CARD POWER SUPPLY:** 5.0V for all internal circuitry. |
| GND | | **GROUND:** for all internal circuitry. |
| REG# | INPUT | **ATTRIBUTE MEMORY SELECT:** Used to enable access to Attribute space. Should be in high level during common memory area access. In True IDE Mode input signal is not used and should be connected to Vcc. |
| Reset<br>Reset# | INPUT | **Reset, Reset#:** Active signal will clear all registers on the card (power on default). In True IDE Mode Reset# is the active low hardware reset from the host. |

## Card Signal Description (Cont.)

| Symbol | Type | Name and Function |
|---|---|---|
| WAIT # | OUTPUT | **WAIT:** This signal outputs low level for purpose of delaying memory or I/O access cycle. In True IDE Mode this signal can be used as IORDY. |
| BVD2<br>SPKR #<br>DASP # | Input/Output | **Battery Voltage Detect 2, Data audio output, Disk active/slave present:** In memory card mode, BVD2 is always high. In I/O mode, SPKR # is held high: no digital audio signals. In True IDE Mode DASP # is Disk Active/Slave Present signal in Master/Slave handshake protocol. |
| BVD1<br>STSCHNG #<br>PDIAG # | Input/Output | **Battery Voltage Detect 1, Status Change, Pass Diagnostic:** In memory card mode BVD1 Is set to high level. In I/O mode STSCHNG # is used to alert the host to changes in Status registers. In True IDE mode PDIG is the Pass Diagnostic signal in Master/Slave handshake protocol. |
| VS1, VS2 | OUTPUT | **VOLTAGE SENSE:** Notifies the host socket of the card's VCC requirements. VS1 and VS2 are open to indicate a 5V, 16 bit card has been inserted. |
| CSEL # | Input | **Card Select:** This signal is not used in memory and I/O mode. With internal pull up resistor this signal is used to configure this card as Master or Slave when configured in True IDE Mode. When this pin is GND, selected Master config, when pin is open the card is configured as a Slave. |
| INPACK # | Output | **Input Acknowledge**: This signal is not used in memory mode. It is asserted by the card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used for the input data buffer control. In True IDE Mode this signal is not used and should not be connected at the host. |
| IORD # | Input | **I/O Read:** is used for control of read data in Task File area. This card respond to this signal only in I/O interface mode |
| IOWR # | Input | **I/O Write:** is used for control of data write in Task File area. This card respond to this signal only in I/O interface mode |

## Card Function Explanation

### Register Construction

- Attribute Region
  - Configuration Register
    - — Configuration Option Register
    - — Configuration and Status Register
    - — Pin Replacement Register
    - — Socket and Copy Register
  - CIS (Card Information Structure)

- Task File Region
  - Error Register
  - Feature Register
  - Sector Count Register
  - Sector Number Register
  - Cylinder Low Register
  - Cylinder High Register
  - Drive/Head Register
  - Status Register
  - Command Register
  - Disk Address Pointer
  - Buffer RAM Size Control Register
  - Host Interrupt Status Register
  - Host Interrupt Enable Register
  - ECC Control Register
  - ECC 0-2 Registers
  - DMA Control Register

## Host Access Specification

### 1. Attribute Access Specification

When the CIS-ROM region or Configuration register region is accessed, read and write operations are executed under the condition of REG# = Low as follows. That region can be accessed by Byte/Word/Odd-byte modes which are defined by the PC card standard specification.

**Attribute Read Access Mode**

| Mode | REG# | CE2# | CE1# | A0 | OE# | WE# | D15 - D8 | D7 - D0 |
|---|---|---|---|---|---|---|---|---|
| Standby Mode | X | H | H | X | X | X | High Z | High Z |
| Byte access | L | H | L | L | L | H | High Z | even byte |
| | L | H | L | H | L | H | High Z | invalid |
| Word access (16 bit) | L | L | L | X | L | H | invalid | even byte |
| Odd Byte access (8 bi | L | L | H | X | L | H | invalid | High Z |

**Attribute Write Access Mode**

| Mode | REG# | CE2# | CE1# | A0 | OE# | WE# | D15 - D8 | D7 - D0 |
|---|---|---|---|---|---|---|---|---|
| Standby Mode | X | H | H | X | X | X | Don't care | Don't care |
| Byte access | L | H | L | L | H | L | Don't care | even byte |
| | L | H | L | H | H | L | Don't care | Don't care |
| Word access (16 bit) | L | L | L | X | H | L | Don't care | even byte |
| Odd Byte access (8 bi | L | L | H | X | H | L | Don't care | Don't care |

## 2. Task File Register Access Specification

There are two cases of Task File register mapping, one is the mapped I/O address area, the other is the Mapped Memory address area. Each case of the Task File register read and write operation is executed under the following conditions. The area can be accessed by Byte/Word/Odd Byte mode which is defined by the PC card standard specification.

### (a) I/O address map

Task File Register Read Access Mode (a)

| Mode | REG# | CE2# | CE1# | A0 | IORD# | IOWR# | OE# | WE# | D15 - D8 | D7 - D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Standby Mode | X | H | H | X | X | X | X | X | High Z | High Z |
| Byte access | L | H | L | L | L | H | H | H | High Z | even byte |
| | L | H | L | H | L | H | H | H | High Z | odd byte |
| Word access (16 bit) | L | L | L | X | L | H | H | H | odd byte | even byte |
| Odd Byte access (8 bi | L | L | H | X | L | H | H | H | odd byte | High Z |

Task File Register Write Access Mode (a)

| Mode | REG# | CE2# | CE1# | A0 | IORD# | IOWR# | OE# | WE# | D15 - D8 | D7 - D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Standby Mode | X | H | H | X | X | X | X | X | Don't care | Don't care |
| Byte access | L | H | L | L | H | L | H | H | Don't care | even byte |
| | L | H | L | H | H | L | H | H | Don't care | odd byte |
| Word access (16 bit) | L | L | L | X | H | L | H | H | odd byte | even byte |
| Odd Byte access (8 bi | L | L | H | X | H | L | H | H | odd byte | Don't care |

### (b) Memory address map

Task File Register Read Access Mode (b)

| Mode | REG# | CE2# | CE1# | A0 | IORD# | IOWR# | OE# | WE# | D15 - D8 | D7 - D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Standby Mode | X | H | H | X | X | X | X | X | High Z | High Z |
| Byte access | H | H | L | L | H | H | L | H | High Z | even byte |
| | H | H | L | H | H | H | L | H | High Z | odd byte |
| Word access (16 bit) | H | L | L | X | H | H | L | H | odd byte | even byte |
| Odd Byte access (8 bi | H | L | H | X | H | H | L | H | odd byte | High Z |

Task File Register Write Access Mode (b)

| Mode | REG# | CE2# | CE1# | A0 | IORD# | IOWR# | OE# | WE# | D15 - D8 | D7 - D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Standby Mode | X | H | H | X | X | X | X | X | Don't care | Don't care |
| Byte access | H | H | L | L | H | H | H | L | Don't care | even byte |
| | H | H | L | H | H | H | H | L | Don't care | odd byte |
| Word access (16 bit) | H | L | L | X | H | H | H | L | odd byte | even byte |
| Odd Byte access (8 bi | H | L | H | X | H | H | H | L | odd byte | Don't care |

### 3. True IDE Mode

The card can be configured in a True IDE Mode of operation. This card is configured in this mode only when the OE# input signal is asserted low by the host during the power off to power on cycle. In this True IDE Mode the PCMCIA protocol and configuration are disabled and only an I/O operation to the Task File registers is allowed. In this mode no Memory or Attribute registers are accessible to the host. The card permits 8 bit access if the user issues a Set feature Command to put the device in the 8 bit Mode.

**True IDE Mode Read I/O function**

| Mode | CE2# | CE1# | A0..A2 | IORD# | IOWR# | D15 - D8 | D7 - D0 |
|---|---|---|---|---|---|---|---|
| Invalid Mode | L | L | X | X | X | High Z | High Z |
| Standby Mode | H | H | X | X | X | High Z | High Z |
| Data Register Access | H | L | 0h | L | H | odd byte | even byte |
| All status access | L | H | 6h | L | H | High Z | status out |
| Other task file access | H | L | 1-7h | L | H | High Z | data |

**True IDE Mode Read I/O function**

| Mode | CE2# | CE1# | A0..A2 | IORD# | IOWR# | D15 - D8 | D7 - D0 |
|---|---|---|---|---|---|---|---|
| Invalid Mode | L | L | X | X | X | Don't care | Don't care |
| Standby Mode | H | H | X | X | X | Don't care | Don't care |
| Data Register Access | H | L | 0h | H | L | odd byte | even byte |
| All status access | L | H | 6h | H | L | Don't care | control in |
| Other task file access | H | L | 1-7h | H | L | Don't care | data |

## Configuration Register Specifications

This card supports four Configuration registers for the purpose of the configuration and observation of this card.

### 1. Configuration Option Register (Address 200H)

This register is used for the configuration of the card configuration status and for the issuing the soft reset to the card.

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|
| SRESET | LevlREQ | INDEX | | | | | |

Note: initial value: 00H

| Name | R/W | Function |
|---|---|---|
| SRESET (HOST->) | R/W | Setting this bit to "1", places the card in the reset state (Card Hard Reset). This operation is equal to Hard Reset, except this bit is not cleared. Then this bit is set to "0", places the card in the reset state of Hard Reset (This bit is set to "0" by Hard Reset) . Card configuration status is reset and the card internal initialized operation starts when Card Hard Reset is executed, so the next access to the card should be the same sequence as the power on sequence. |
| LevlREQ (HOST->) | R/W | This bit sets to "0" when pulse mode interrupt is selected, and "1" when level mode interrupt is selected. |
| INDEX (HOST->) | R/W | This bit is used to select the operation mode of the card as follows. When Power on, Card Hard Reset and Soft Reset, this data is "000000" for the purpose of Memory card interface recognition. |

### INDEX bit assignment

| INDEX bit | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 | 0 | Card mode | Task File register address | Mapping mode |
| 0 | 0 | 0 | 0 | 0 | 0 | Memory card | 0H to FH, 400H to 7FFH | memory mapped |
| 0 | 0 | 0 | 0 | 0 | 1 | I/O card | xx0H to xxFH | contiguous I/O mapped |
| 0 | 0 | 0 | 0 | 1 | 0 | I/O card | 1F0H to 1F7H, 3F6H to 3F7H | primary I/O mapped |
| 0 | 0 | 0 | 0 | 1 | 1 | I/O card | 170H to 177H, 376H to 377H | secondary I/O mapped |

## 2. Configuration and Status Register (Address 202H)

This register is used for observing the card state.

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|
| CHGED | SIGCHG | IOIS8 | 0 | 0 | PWD | INTR | 0 |

Note: initial value: 00H

| Name | R/W | Function |
|---|---|---|
| CHGED (CARD->) | R | This bit indicates that the CRDY/-BSY bit on the Pin Replacement register is set to "1". When CHGED bit is set to "1", the -STSCHG pin is held "L" at the condition of SIGCHG bit set to "1" and the card configured for the I/O interface. |
| SIGCHG (HOST->) | R/W | This bit is set or reset by the host for enabling and disabling the status-change signal (-STSCHG pin). When the card is configured I/O card interface and this bit is set to "1", -STSCHG pin is controlled by the CHGED bit. If this bit is set to "0", the -STSCHG pin is kept "H". |
| IOIS8 (HOST->) | R/W | The host sets this field to "1" when it can provide I/O cycles only with on 8 bit data bus (D7 to D0). |
| PWD (HOST->) | R/W | When this bit is set to "1", the card enters the sleep state (Power Down mode). When this bit is reset to "0", the card transfers to the idle state (active mode). RRDY/-BSY bit on the Pin Replacement Register becomes BUSY when this bit is changed. RRDY/-BSY will not become Ready until the power state requested has been entered. This card automatically powers down when it is idle, and powers back up when it receives a command. |
| INTR (CARD->) | R | This bit indicates the internal state of the interrupt request. This bit state is available whether the I/O card interface has been configured or not. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the -IEN bit in the Device Control Register, this bit is a zero. |

### 3. Pin Replacement Register (Address 204H)

| t7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | CRDY/-BSY | 0 | 1 | 1 | RRDY/-BSY | 0 |

Note: initial value: 0CH

| Name | R/W | Function |
|---|---|---|
| CRDY/-BSY (HOST->) | R/W | This bit is set to "1" when the RRDY/-BSY bit changes state. This bit may also be written by the host. |
| RRDY/-BSY (HOST->) | R/W | When read, this bit indicates +READY pin states. When written, this bit is used for CRDY/-BSY bit masking. |

### 4. Socket and Copy Register (Address 206H)

This register is used for identification of the card from the other cards. The host can read and write this register. This register should be set by the host before this card's Configuration Option register set.

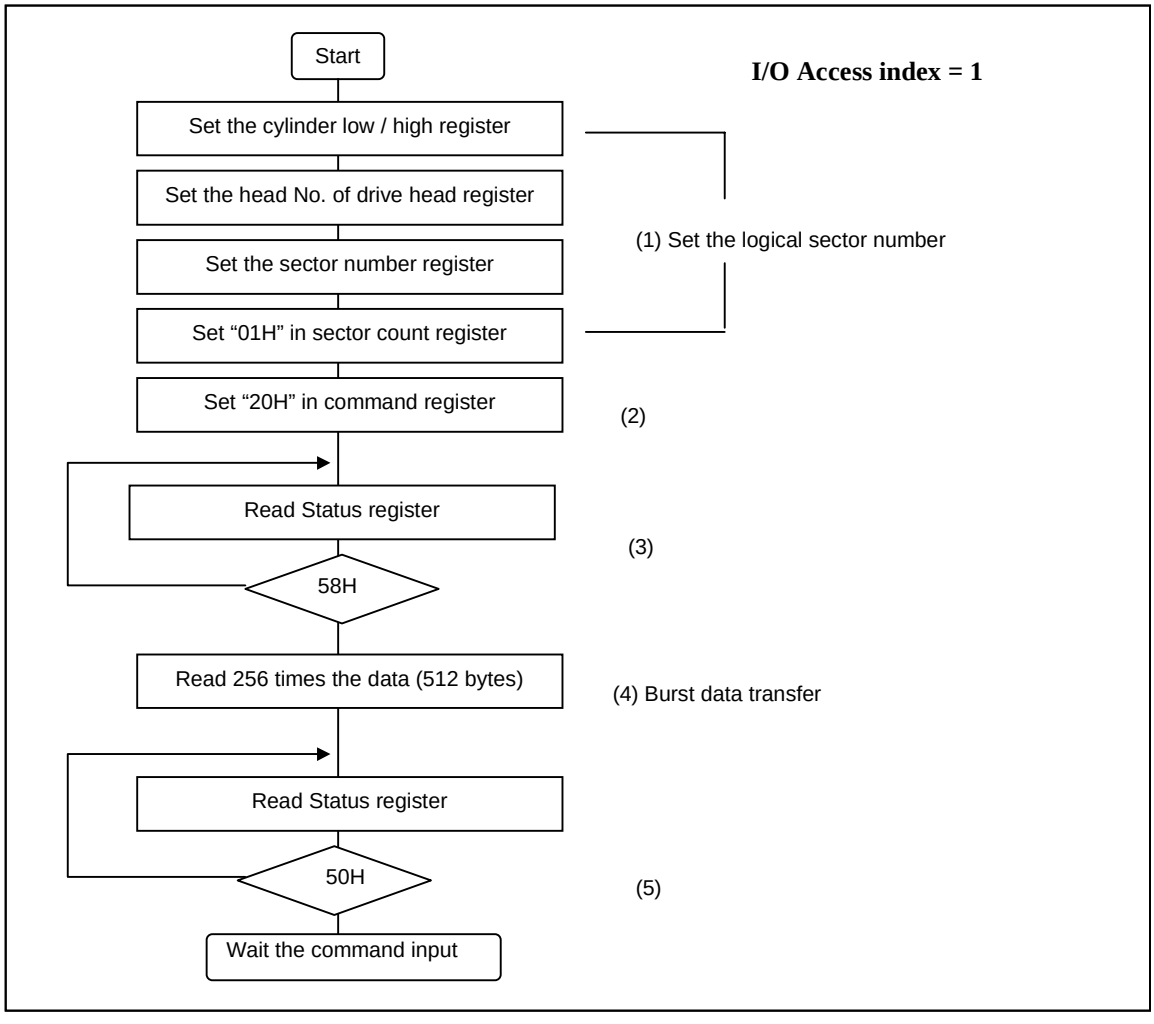
| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | DRV# | 0 | 0 | 0 | 0 |

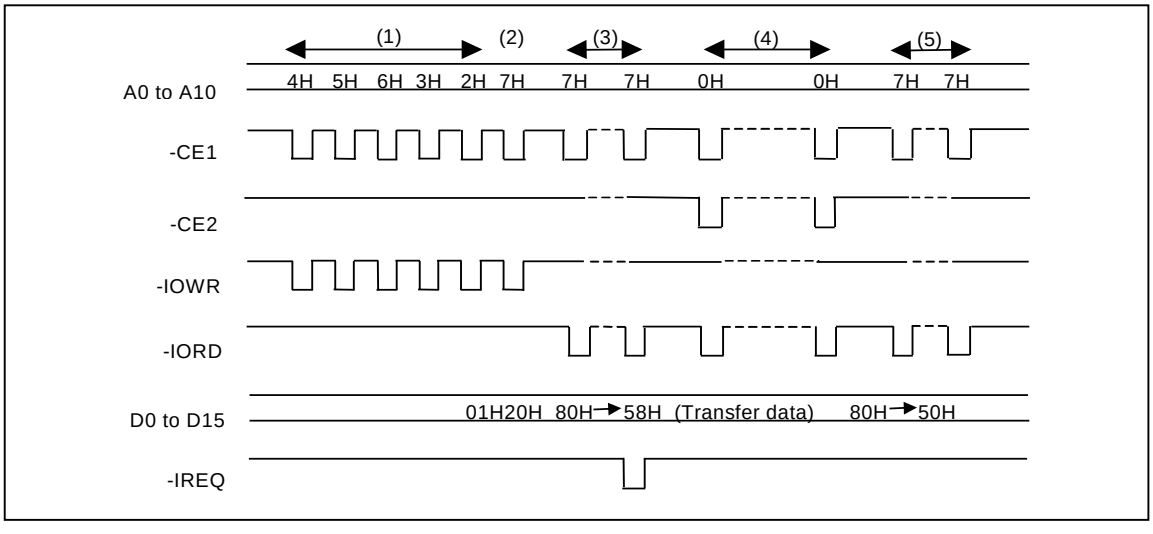
Note: initial value: 00H

| Name | R/W | Function |
|---|---|---|
| DRV# (HOST->) | R/W | This field is used for the configuration of the plural cards. |

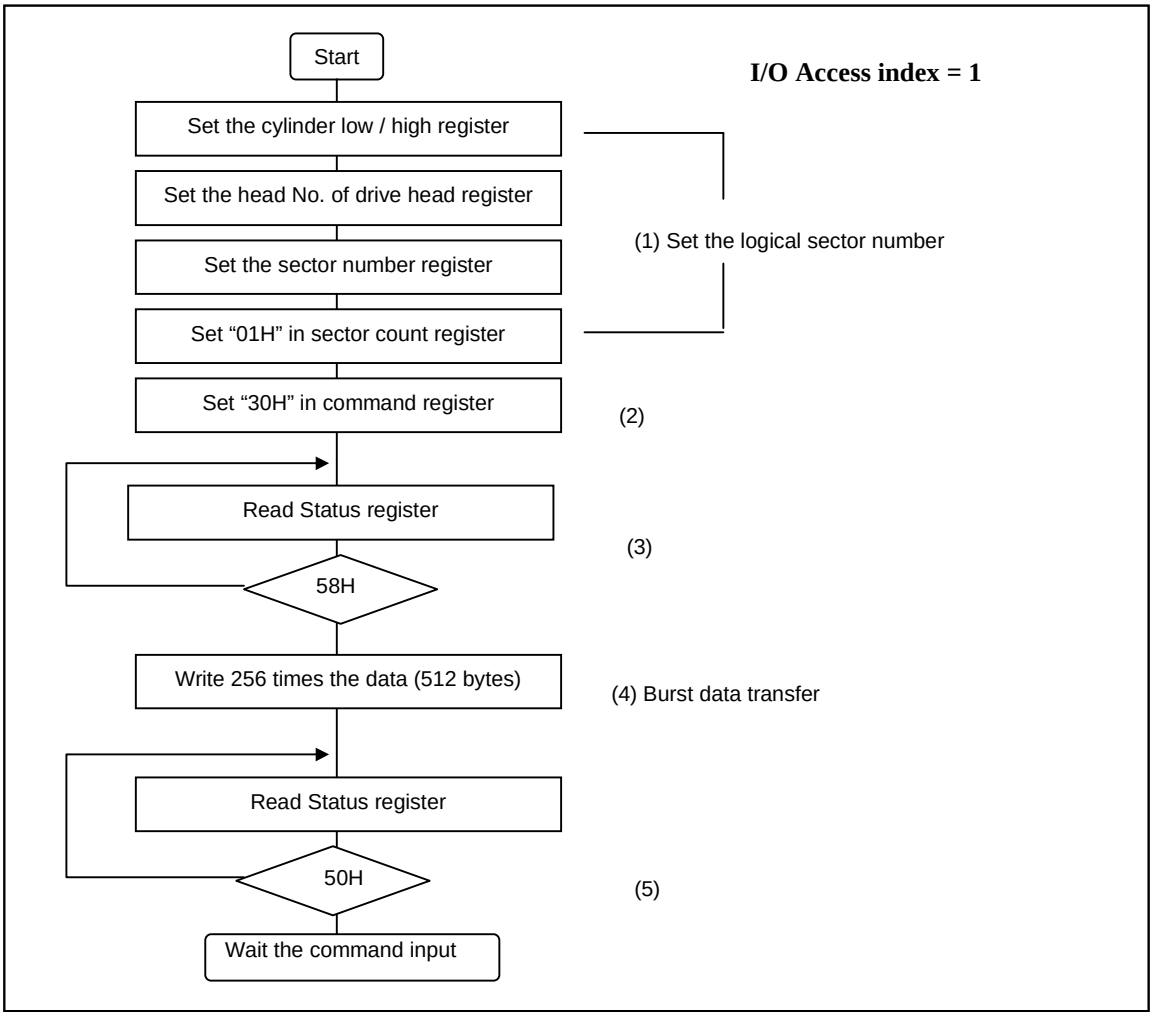
## Sector Transfer Protocol

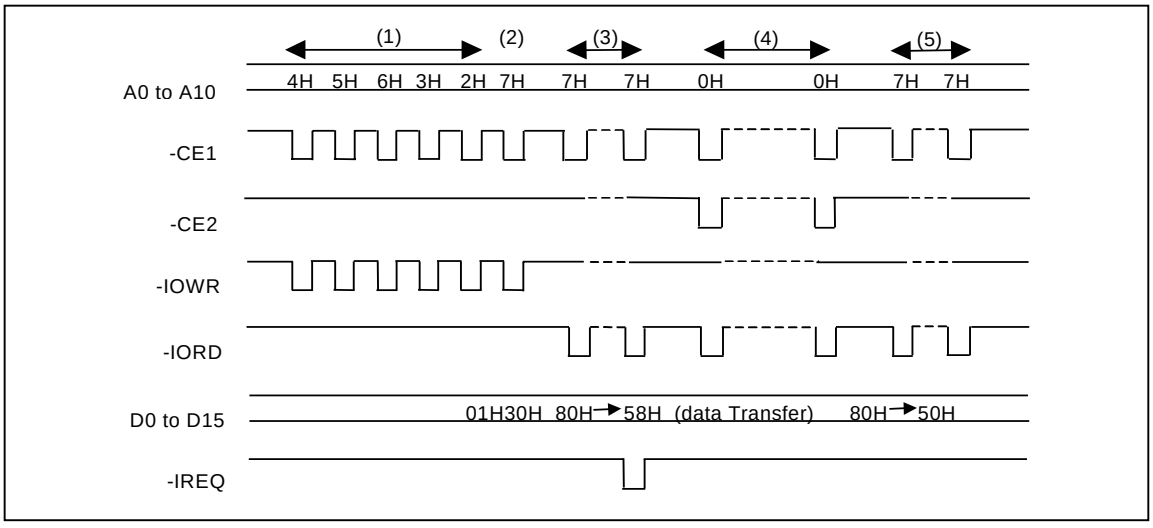
**1. Sector read: 1 sector read procedure after the card configured I/O interface is shown as follows.**



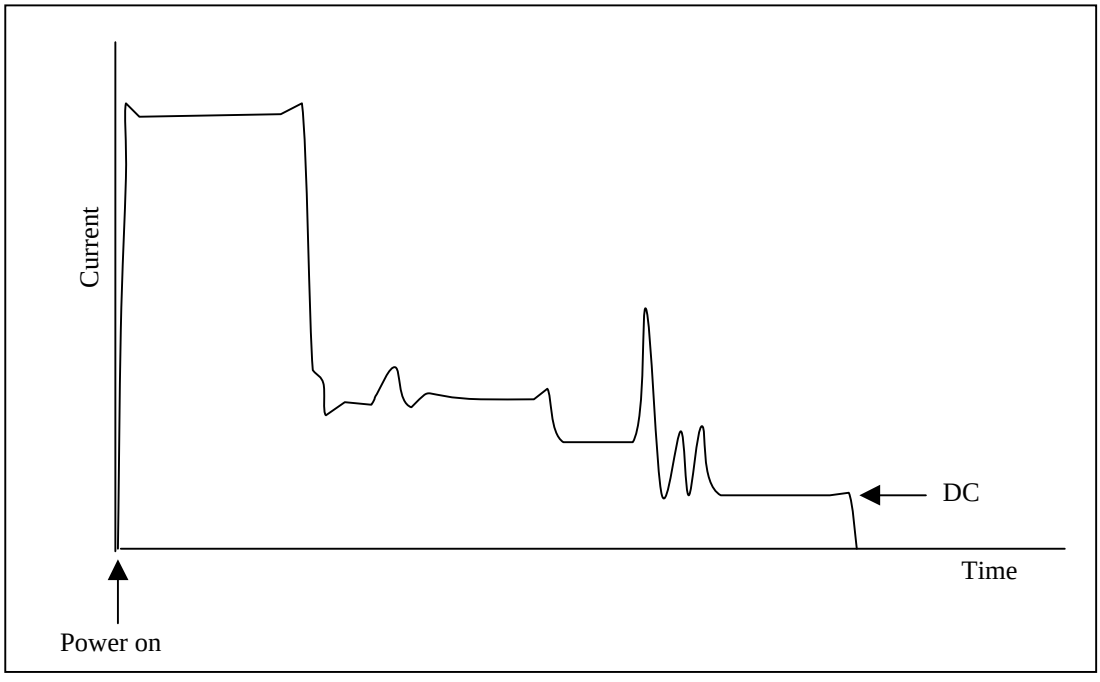
**2. Sector write: 1 sector write procedure after the card configured I/O interface is shown as follows.**



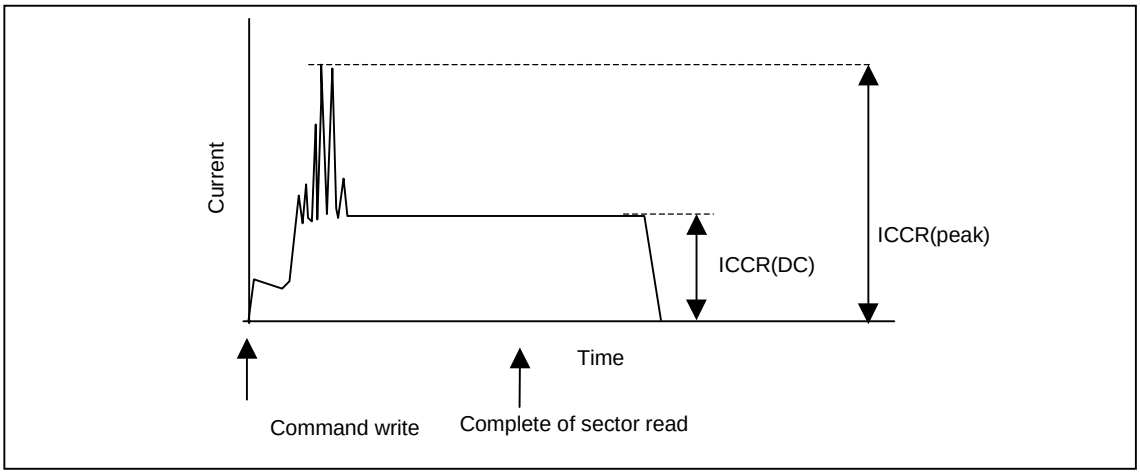



**DC Current Waveform** (Example of sector read or write: $V_{CC}$ = 5 V, Ta = 25°C)

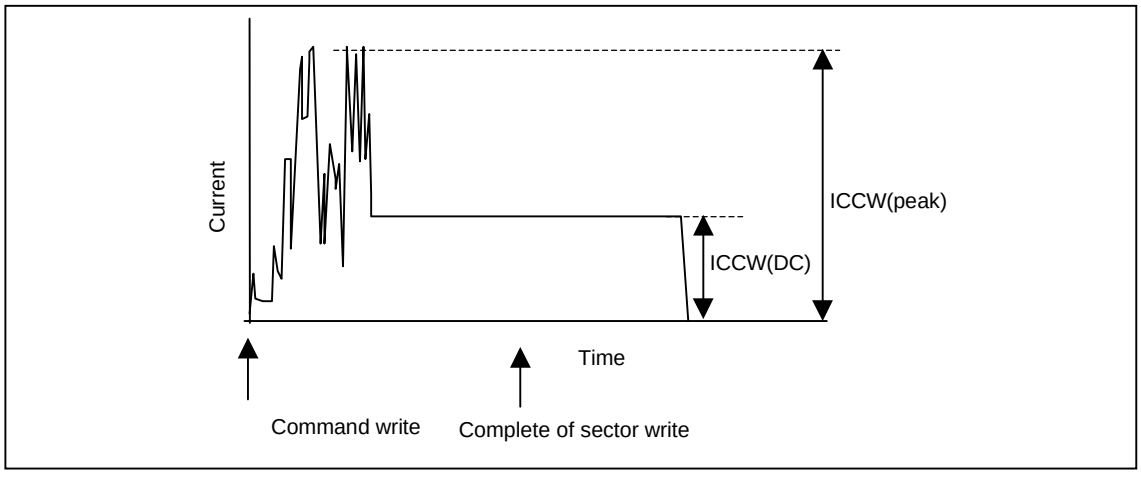
**Power on Operation** (Reference Only)



### Sector Read




### Sector Write



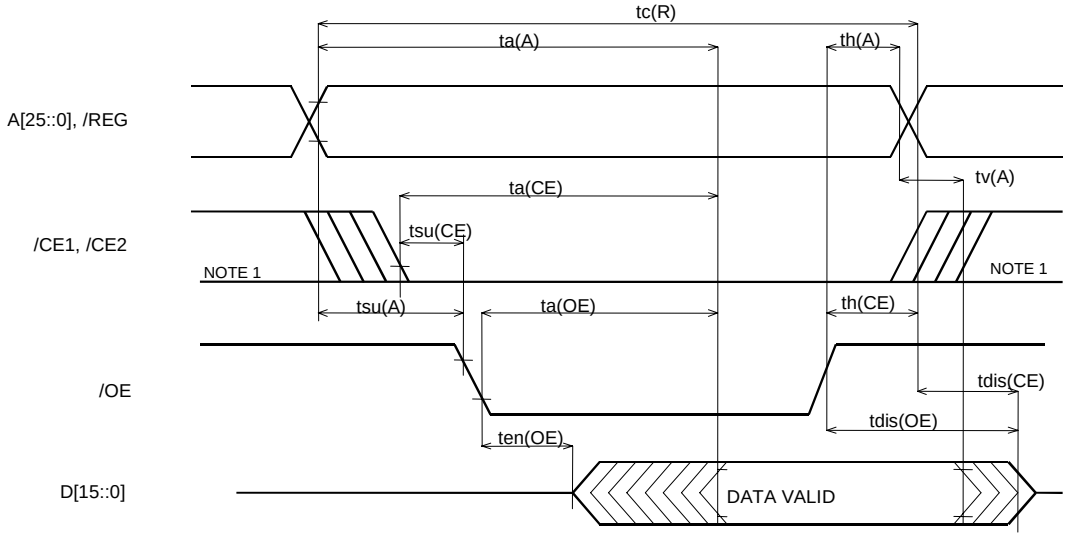
## AC Characteristics

### Read Timing Parameters

| | | 250ns | | |
|---|---|---|---|---|
| **SYM (PCMCIA)** | **Parameter** | **Min** | **Max** | **Unit** |
| $T_C(R)$ | Read Cycle Time | 250 | | ns |
| $t_a(A)$ | Address Access Time | | 250 | ns |
| $t_a(CE)$ | Card Enable Access Time | | 250 | ns |
| $t_a(OE)$ | Output Enable Access Time | | 150 | ns |
| $t_{su}(A)$ | Address Setup Time | 30 | | ns |
| $t_{su}(CE)$ | Card Enable Setup Time | 0 | | ns |
| $t_h(A)$ | Address Hold Time | 20 | | ns |
| $t_h(CE)$ | Card Enable Hold Time | | 20 | ns |
| $t_v(A)$ | Output Hold from Address Change | | 0 | ns |
| $t_{dis}(CE)$ | Output Disable Time from CE# | | 100 | ns |
| $t_{dis}(OE)$ | Output Disable Time from OE# | | 100 | ns |
| $T_{en}(CE)$ | Output Enable Time from CE# | 5 | | ns |
| $T_{en}(OE)$ | Output Enable Time from OE# | 5 | | ns |

**Note:** AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

### Read Timing Diagram



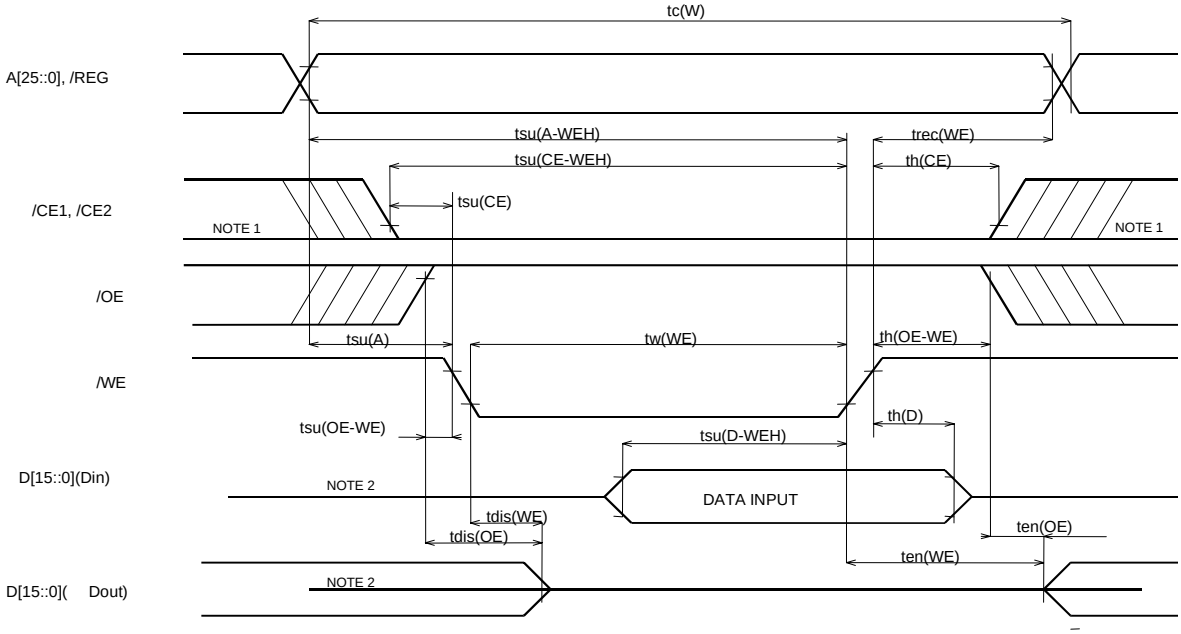

**Note:** Signal may be high or low in this area.

## Write Timing Parameters

| | | 250ns | | |
|---|---|---|---|---|
| **SYM (PCMCIA)** | **Parameter** | **Min** | **Max** | **Unit** |
| $t_C$(W) | Write Cycle Time | 250 | | ns |
| $t_w$(WE) | Write Pulse Width | 150 | | ns |
| $t_{su}$(A) | Address Setup Time | 30 | | ns |
| $t_{su}$(A-WEH) | Address Setup Time for WE# | 180 | | ns |
| $t_{su}$(CE-WEH) | Card Enable Setup Time for WE# | 180 | | ns |
| $t_{su}$(D-WEH) | Data Setup Time for WE# | 80 | | ns |
| $t_h$(D) | Data Hold Time | 30 | | ns |
| $t_{rec}$(WE) | Write Recover Time | 30 | | ns |
| $t_{dis}$(WE) | Output Disable Time from WE# | | 100 | ns |
| $t_{dis}$(OE) | Output Disable Time from OE# | | 100 | ns |
| $t_{en}$(WE) | Output Enable Time from WE# | 5 | | ns |
| $T_{en}$(OE) | Output Enable Time from OE# | 5 | | ns |
| $t_{su}$(OE-WE) | Output Enable Setup from WE# | 10 | | ns |
| $t_h$(OE-WE) | Output Enable Hold from WE# | 10 | | ns |
| $t_{su}$(OE) | Card Enable Setup Time from OE# | 0 | | ns |
| $t_h$(CE) | Card Enable Hold Time | 20 | | ns |

**Note:** AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

## Write Timing Diagram




**Notes:**
1. Signal may be high or low in this area.
2. When the data I/O pins are in the output state, no signals shall be applied to the data pins (D15 - D0) by the host system.

# PRODUCT MARKING

**WED 7P016ATA1000C15 C995 9915**

- **EDI** — Company Name
- **7P016ATA1000C15** — Part number
- **C995** — Lot code / trace number
- **9915** — Date code

Note:
Some products are currently marked with our pre-merger company name/acronym (EDI). During our transition period, some products will also be marked with our new company name/acronym (WED). Starting October 2000 all PCMCIA products will be marked only with the WED prefix.

# PART NUMBERING

**7 P 016 ATA10 00 C 15**

**Card access time**

| | |
|---|---|
| 15 | 150ns |
| 25 | 250ns |

**Temperature range**

| | | |
|---|---|---|
| C | Commercial | 0°C to +70°C |
| I | Industrial | -40°C to +85°C |

**Packaging option**

| | |
|---|---|
| 00 | Standard, type 1 |

**Card family and version**

- See Card Family and Version Info. for details (next page)

**Card capacity**

| | |
|---|---|
| 016 | 16MB |

**PC card**

| | |
|---|---|
| P | Standard PCMCIA |
| R | Ruggedized PCMCIA |

**Card technology**

| | |
|---|---|
| 7 | FLASH |
| 8 | SRAM |

## Ordering Information

**7P** XXX **ATA** YY SS T ZZ

**where**

| | | | |
|---|---|---|---|
| **XXX:** | **008** | **8MB** | |
| | **016** | **16MB** | |
| | **032** | **32MB** | |
| | **048** | **48MB** | |
| | **064** | **64MB** | |
| | **080** | **80MB** | |
| | **096** | **96MB** | |
| | **112** | **112MB** | |
| | **128** | **128MB** | |
| | **192** | **192MB** | |
| | **224** | **224MB** | |
| | **256** | **256MB** | |
| | **320** | **320MB** | |
| | **384** | **384MB** | |
| | **448** | **448MB** | |
| | **512** | **512MB** | |
| **YY:** | **10** | **Standard, 5V Only: (Controller type = MX)** | |
| **SS:** | **00** | **WEDC FLASH Logo,** | **Type I** |
| | **01** | **Blank Housing,** | **Type I** |
| | **02** | **Blank Housing,** | **Type I Recessed** |
| | **03** | **WEDC FLASH Logo,** | **Type II** |
| | **04** | **Blank Housing,** | **Type II** |
| | **05** | **Blank Housing,** | **Type II Recessed** |
| | **14** | **Blank Housing,** | **Type III** |
| **T:** | **C** | **Commercial** | |
| | **I** | **Industrial** | |
| **ZZ:** | **25** | **250ns** | |

## Revision History:

| *rev level* | *description* | *date* |
|---|---|---|
| **rev 0** | **initial release** | **June 1, 1998** |
| **rev 1** | **Logo change**<br>**New card capacity** | **May 27, 1999** |
| **rev 2** | **New flowcharts added**<br>**New timing diagrams added** | **Sep 10, 1999** |
| **rev 3** | **New form factor options added**<br>**New Flowcharts added**<br>**New current waveforms added**<br>**Register list added** | **Oct. 18, 1999** |
| **rev 4** | **Max capacity change to 512MB** | **Dec 19, 1999** |
| **rev 5** | **Timing corrections on Pgs 21 & 22. Page 23 added, Page Header changed** | **June 2, 2000** |

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