

NEC

MOS FIELD EFFECT POWER TRANSISTOR 2SK1992/2SK1993

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK1992/2SK1993 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} \leq 0.9/1.0 \Omega$ ($V_{GS} = 10 \text{ V}$, $I_D = 3.0 \text{ A}$)
- Low C_{iss} $C_{iss} = 1060 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

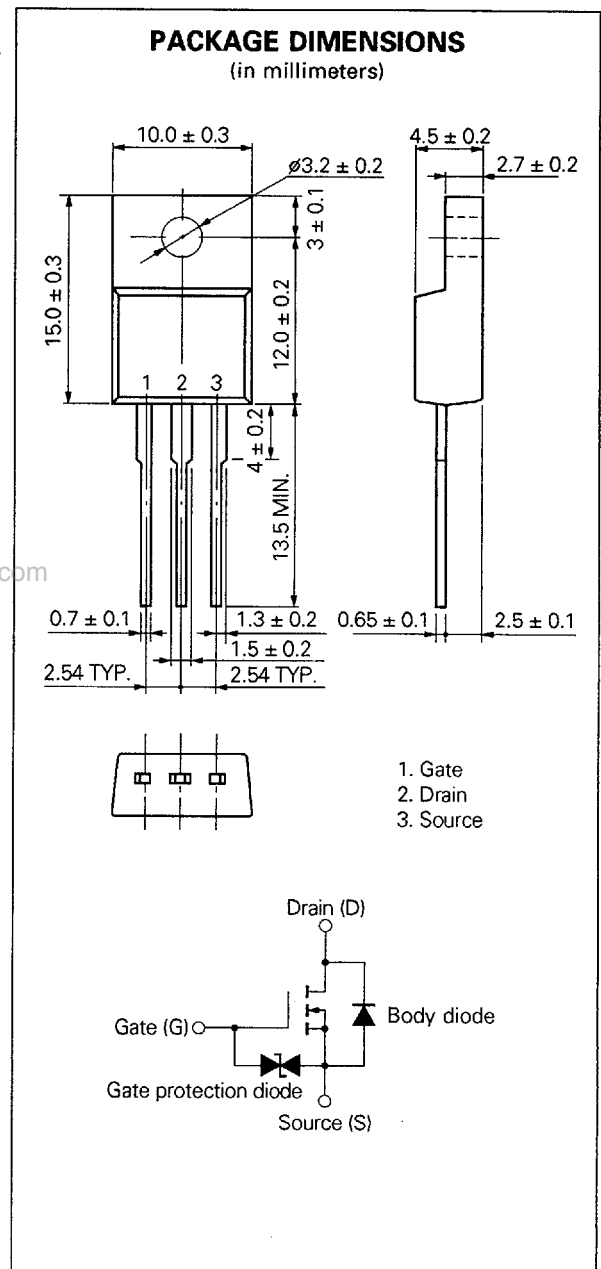
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25 \text{ }^\circ\text{C}$)

Drain to Source Voltage	V_{DSS}	450/500	V
Gate to Source Voltage	V_{GSS}	± 30	V
Drain Current (DC)	$I_{D(DC)}$	± 6.0	A
Drain Current (pulse)	$I_{D(pulse)^*}$	± 24	A
Total Power Dissipation ($T_c = 25 \text{ }^\circ\text{C}$)	P_{T1}	35	W
Total Power Dissipation ($T_a = 25 \text{ }^\circ\text{C}$)	P_{T2}	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current	I_{AS}^{**}	9.0	A
Single Avalanche Energy	E_{AS}^{**}	243	mJ

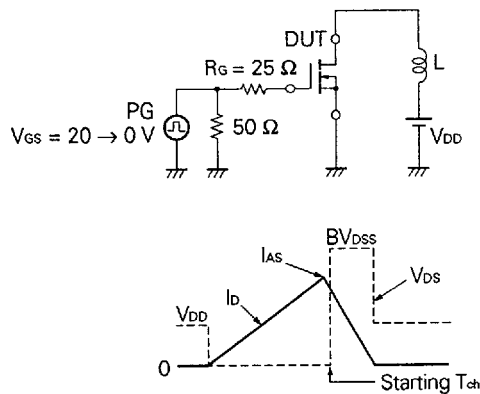
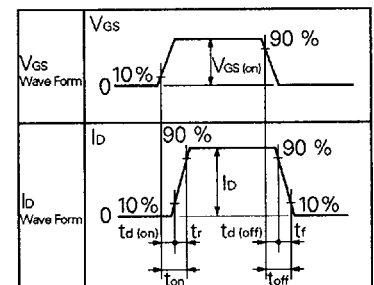
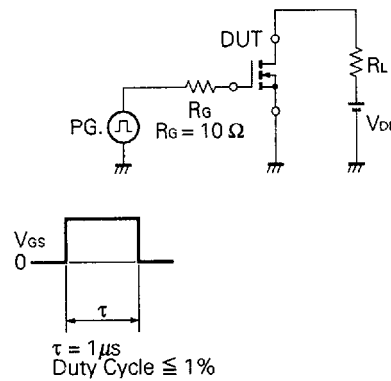
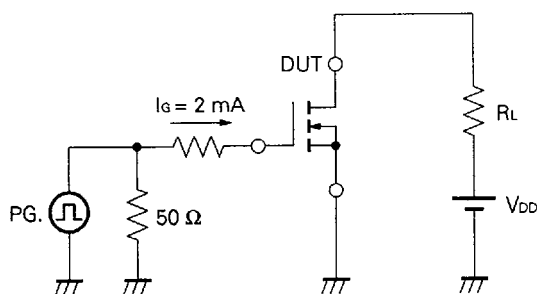
* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1 \%$

** Starting $T_{ch} = 25 \text{ }^\circ\text{C}$, $R_\theta = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0$

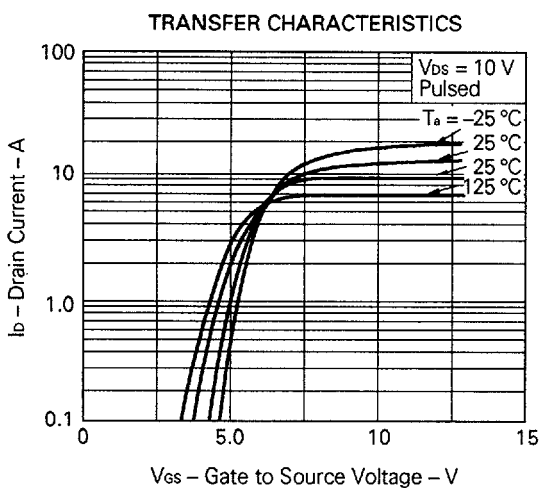
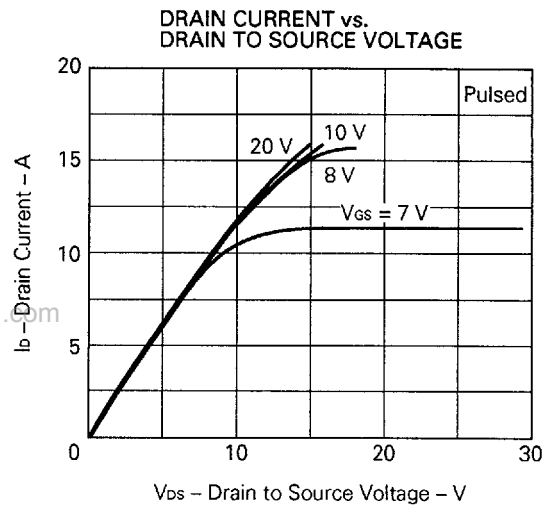
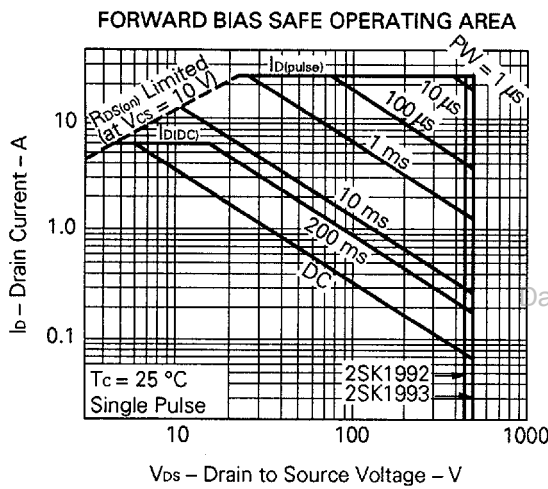
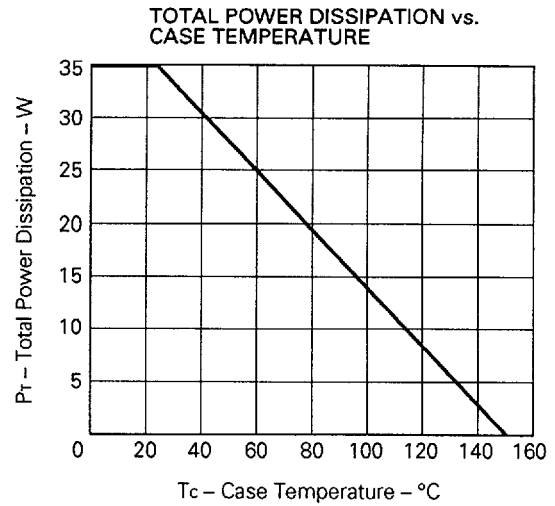
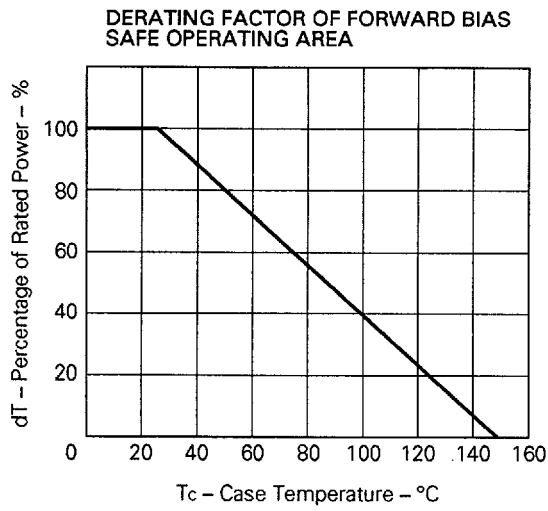


ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

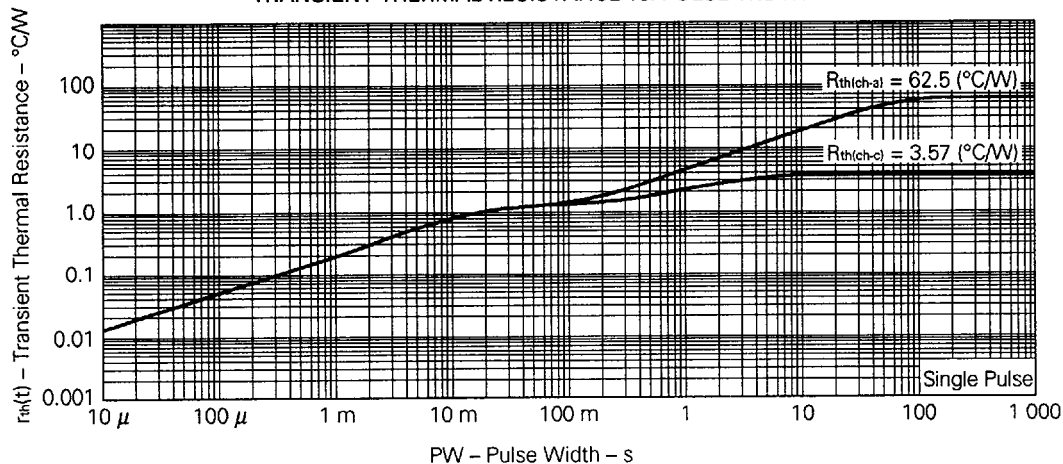
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance (2SK1992)	R _{DS(on)}		0.7	0.9	Ω	V _{GS} = 10 V, I _b = 3.0 A
Drain to Source On-state Resistance (2SK1993)			0.8	1.0	Ω	V _{GS} = 10 V, I _b = 3.0 A
Gate to Source Cutoff Voltage	V _{GS(off)}	2.5		3.5	V	V _{DS} = 10 V, I _b = 1 mA
Forward Transfer Admittance	y _{fs}	2.8			S	V _{DS} = 10 V, I _b = 3.0 A
Drain Leakage Current (2SK1992/1993)	I _{DSS}			100	μA	V _{DS} = 450/500 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±30 V, V _{DS} = 0
Input Capacitance	C _{ies}		1 060		pF	V _{DS} = 10 V V _{GS} = 0 f = 1 MHz
Output Capacitance	C _{oss}		340		pF	
Reverse Transfer Capacitance	C _{res}		150		pF	
Turn-On Delay Time	t _{d(on)}		20		ns	V _{GS} = 10 V V _{DD} = 150 V I _b = 3.0 A, R _G = 10 Ω R _L = 50 Ω
Rise Time	t _r		30		ns	
Turn-Off Delay Time	t _{d(off)}		70		ns	
Fall Time	t _f		20		ns	
Total Gate Charge	Q _G		36		nC	V _{GS} = 10 V I _b = 6 A V _{DD} = 400 V
Gate to Source Charge	Q _{GS}		7		nC	
Gate to Drain Charge	Q _{GD}		21		nC	
Diode Forward Voltage	V _{F(S-D)}		0.9		V	I _F = 6 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		420		ns	I _F = 6 A
Reverse Recovery Charge	Q _{rr}		2.0		μC	di/dt = 50 A/μs

Test Circuit 1: Avalanche Capability**Test Circuit 2: Switching Time****Test Circuit 3: Gate Charge**

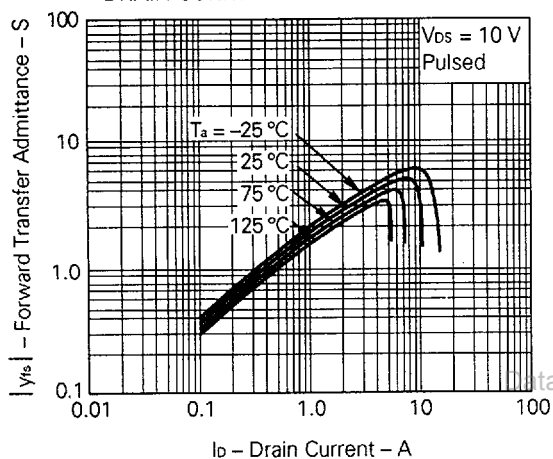
TYPICAL CHARACTERISTICS (T_a = 25 °C)



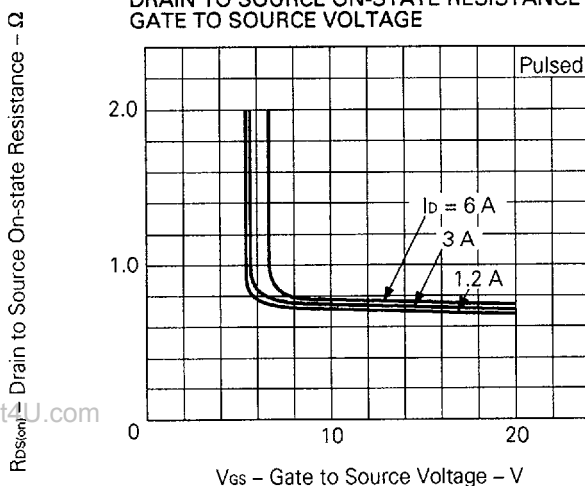
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



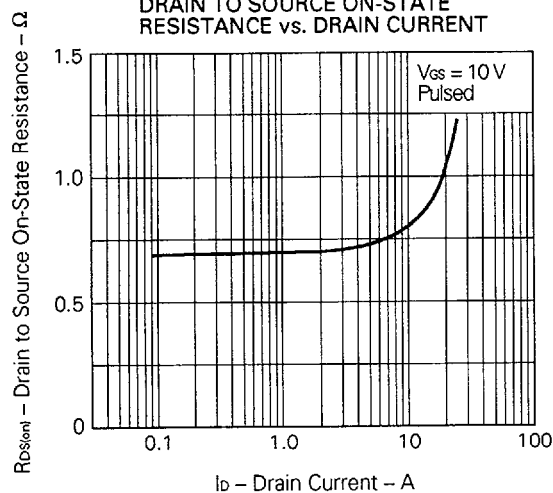
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



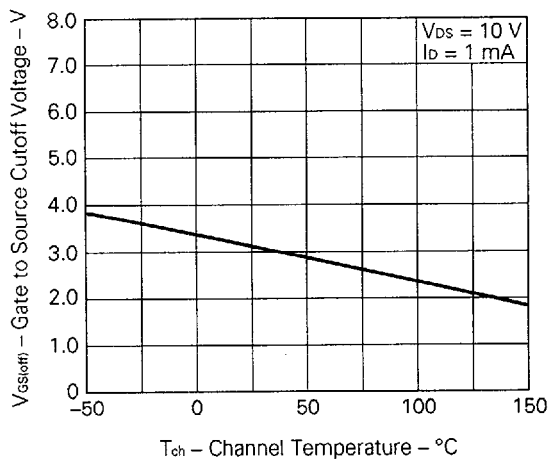
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

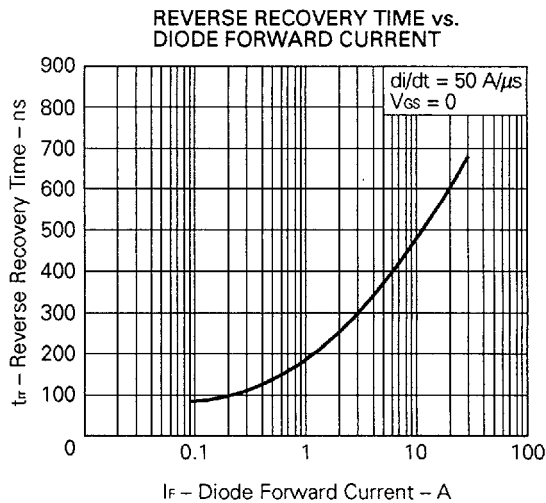
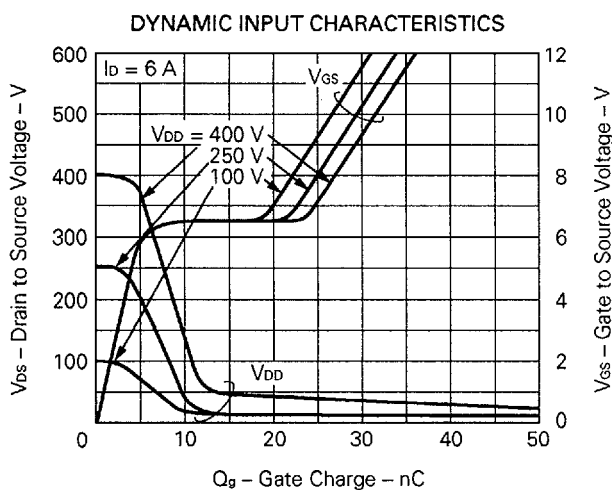
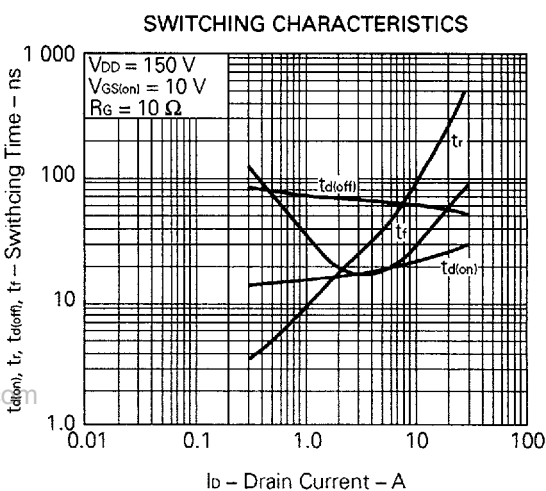
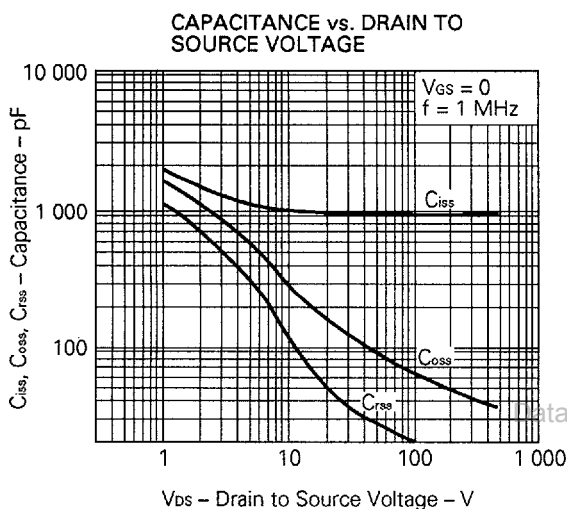
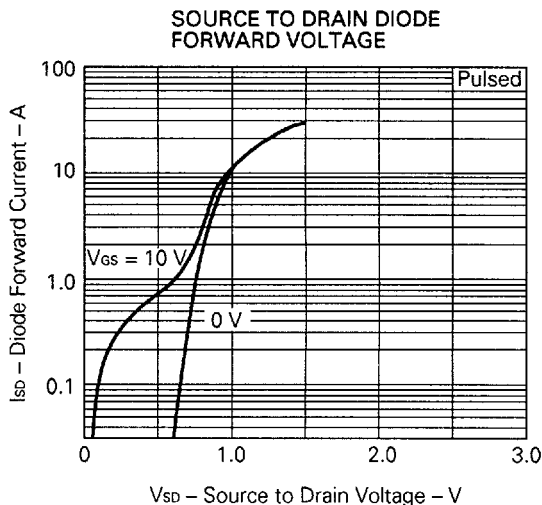
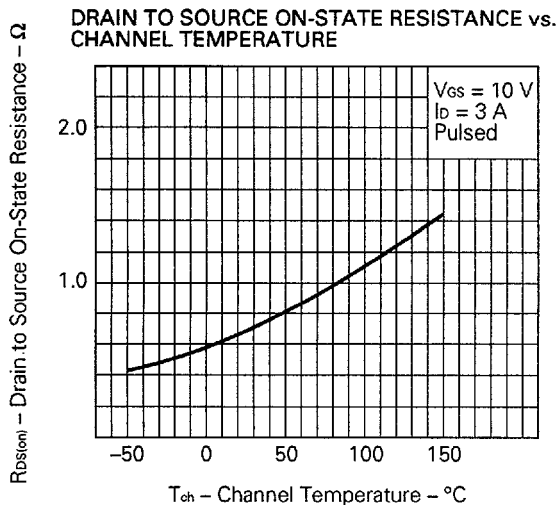


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

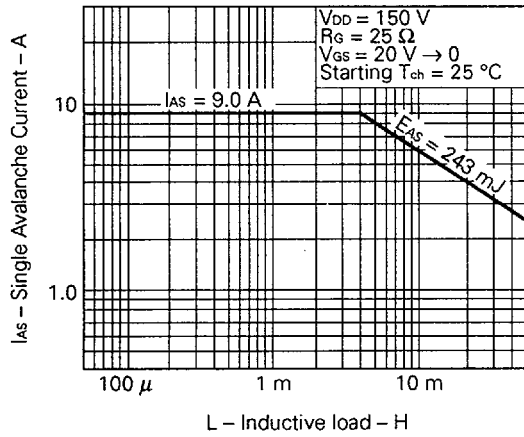


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

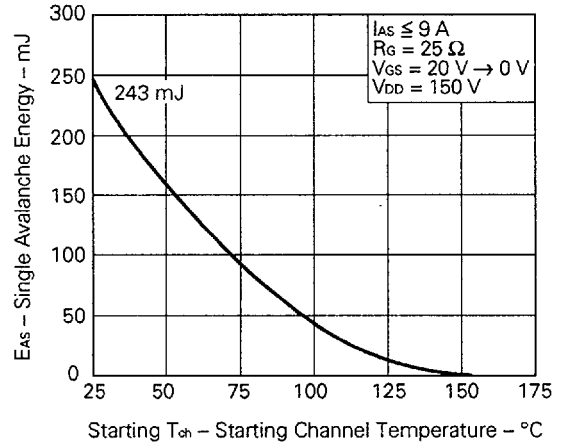




SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs. STARTING CHANNEL TEMPERATURE



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Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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