Features

Overall

- Audio/video synchronization
- Audio and video error detection, concealment, and notification
- 208 pin, plastic quad flat pack (PQFP) package

Audio Decoder

- Audio Decoder with two channel outputs (six channels with Dolby® Digital
- Supports ISO/IEC 13818-3 MPEG-1 and 2, Layers I and II audio
- Decodes elementary streams (ES) or packetized elementary streams (PES)
- Multiple playback sampling frequencies
- Multiple playback modes including PCM and Karaoke
- Dolby Digital Audio decoding and playback (STB13010 only)
- Host controlled programming interface
- 64 step audio attenuation with smooth transition between steps

Transport Demultiplexer

- 160 Mbps (parallel) or 60 Mbps (serial) maximum continuous input rate
- Table selection filtering
- Packet Identifier (PID) Filtering
- DVB Descrambler

Video Decoder

- Compliant with ISO/IEC 13818-2 Profile @ Main Level
- Supports European DVB standard
- Horizontal and vertical filters
- Supports pan and scan in 1/16 pel accuracy
- Supports multiple input image sizes
- On-Screen Display (OSD)
- Programmable output interface
- Programmable PTS filtering
- 3:2 pull-down support
- Supports VBI output

Description

The IBM STB130x0 A/V Transport/Decoders are full function companion decoders, designed to allow seamless integration with IBM's Digital Set-Top Box Integrated Controllers.

Advanced multiple stream applications are enabled when an IBM STB130x0 chip is paired with one of IBM's Digital Set-Top Controllers. Applications include decoding one stream for display on a TV while decoding and recording another to a VCR, picture-in-picture support, or decoding/displaying one stream on a TV, while storing another encoded stream on a hard drive.

When using one of IBM's STB Integrated Controllers with one of the STB130x0 chips setup and control of the companion decoder is simplified due to the seamless interface to the PowerPC processor found in the main controller.

The IBM STB130x0 decoders provide an MPEG transport demultiplexer, MPEG video decoder and an MPEG audio decoder. The STB13010 provides the added functionality to decode Dolby Digital Audio. The transport demultiplexer can receive transport streams up to 160 Mbps. The video decoder can decode MPEG-2 Main Profile video packetized elementary streams. The audio decoder can decode MPEG Layers I and II and Dolby Digital (STB13010 only) packetized elementary streams.

The IBM STB130x0 products each contain two built-in PLLs. One provides system clocks and the other generates the audio sampling frequencies. Both also function to support audio and video synchronization. Additionally, gen-lock is supported by providing separate video and system time clock inputs.

Both products of the STB130x0 family are 208 pin, plastic quad flat pack (PQFP) package devices.

Ordering Information

IBM Part Number	Audio MPEG-2 Layer I and Layer II	Audio Dolby Digital
IBM39STB13000PFA16C	Yes	No
IBM39STB13010PFA16C	Yes	Yes[1]

[1] This part includes Dolby Digital enabling software and requires the user to obtain a license fromDolby Laboratories Licensing Corporation. Please see “Dolby Digital Licensing” on page 3

Conventions and Notation

Throughout this document, IBM notation is used, meaning that bits and bytes are numbered in ascending order from left to right. Thus, for a 4-byte word, bit 0 is the most significant bit and bit 31 is the least significant bit.

Overbars, e.g. $\overline{\text{TxEnb}}$, designate signals that are active low.

Numeric notation is as follows:

Hexadecimal values are in single quotes and preceded by "x" or "X." For example: x’0B00’.

Binary values are spelled out (zero and one) or appear in single quotes and preceded by a "b."
For example: b‘10101’.

Settings of a bit or field are binary numbers but are often displayed in tabular form without quotes or the preceding "b."
For example:

00:30 frames per second
01:15 frames per second
11:10 frames per second

Throughout this document, the word "device" refers to the IBM STB130x0.

Licensing Requirements

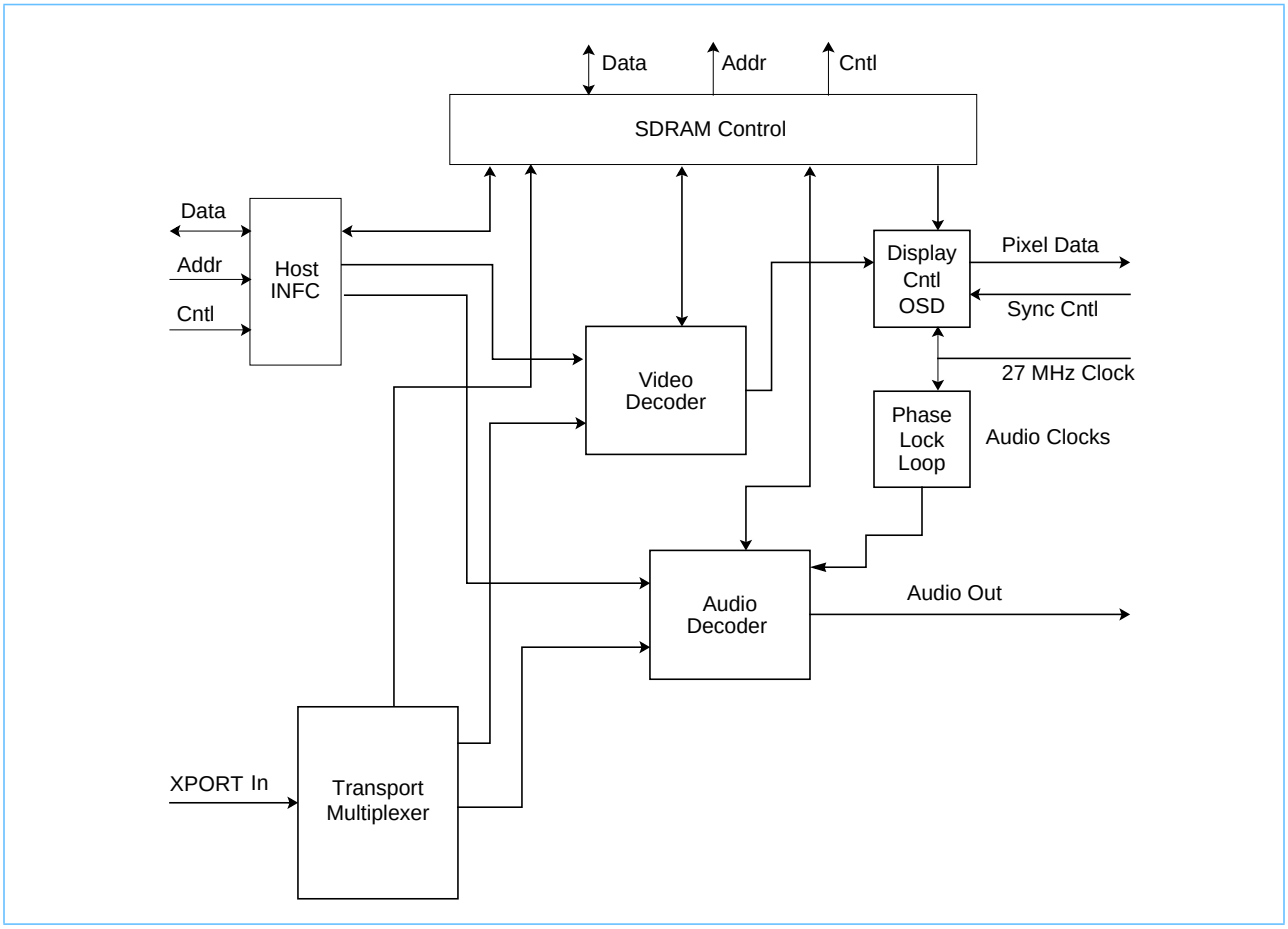
Dolby Digital Licensing

Dolby Digital audio enabling software is provided with the IBM39STB13010 product.

Supply of this implementation of Dolby Technology does not convey a license nor imply a right under any patent, or any other industrial or Intellectual Property Right of Dolby Laboratories, to use this implementation in a finished end-user or ready-to-use final product. Companies planning to use this implementation in any finished products must obtain a license from Dolby Laboratories Licensing Corporation before designing such products. Additional per-chip royalties may be required and are to be paid by the purchaser to Dolby Laboratories, Inc. Details of the OEM Dolby Digital license can be obtained by writing to:
Dolby Laboratories Inc.
Dolby Laboratories Licensing Corporation
Attn: Intellectual Property Manager
100 Potrero Avenue
San Francisco, CA 94103-4813

Architecture and Subsystem Information

Block Diagram



Transport Demultiplexer

The transport demultiplexer performs MPEG-2 transport stream parsing to extract packetized elementary streams (PES) for the audio and video decoders. It provides a full set of demultiplexing functions, including synchronization, PID filtering, clock recovery, table section filtering, CRC checking, and data management. These basic functions are configured by the application and implemented in hardware for improved performance and to minimize the impact on the remainder of the system.

The transport demultiplexer is compliant with ISO/IEC 13818-1 system layer standard, and operates at up to 160 Mbps (parallel) or 60 Mbps (serial) maximum continuous input rate.

MPEG-2 Transport Synchronization

The transport demultiplexer accepts either parallel (8-bit) or serial data. It detects the synchronization character and establishes transport packet boundaries. In the case of serial input, where only a bit clock is provided, it also establishes byte alignment. There are input controls for error flagging and to force packet alignment if already established by a previous device.

PID Filtering

Up to 32 programmable Packet Identifier (PID) values are used to filter the transport stream. The PID filter associates a 5-bit PID index with each of the 32 entries. Entries in the PID filter can be disabled by writing the null PID value. PID index 31 is reserved for the video PID, PID index 30 is for the Audio PID. All other values are defined by the application.

Clock Recovery

The transport demultiplexer assists in recovering the program clock from the transport stream. It extracts Program Clock References (PCRs) from the indicated PID, calculates the offset from the current System Time Clock (STC) value, and compares it against a threshold defined by the application to determine if clock frequency correction is required.

The demultiplexer can either filter the clock difference directly, using a simple hardware algorithm, or it can provide an interrupt to allow the application to filter the difference. The output of the filter is loaded into a pulse modulating register, and the serial pulse train output is used to regulate an external Voltage-Controlled Crystal Oscillator (VCXO) or similar device.

Time Base Changes

When a system time base change occurs in the PCR PID stream, the transport demultiplexer automatically loads the STC with the new time base value. The first audio and video packets which arrive after the system time base change are marked. The transport indicates the first data byte following the time base change to each decoder.

Table Section Filtering

The transport demultiplexer hardware can filter table sections, which reduces the processing load on the application and minimizes the size of temporary work spaces in system memory.

Up to 64 different 4-byte filter blocks consisting of a bit pattern and a bit mask can be defined by the application. Section filters can be constructed from one or more filter blocks to provide deep filtering into a table section. Multiple section filters can be attached to a single PID. Filter blocks can be assigned to the 32 PID indexes as needed by the application. The filtering mechanism supports multiple sections per packet as well as sections that span multiple packets.

Error Handling

The transport demultiplexer simplifies the system-level tasks of error handling and time base (STC) changes by using the compressed data connection to communicate directly with the decoders. Errors are detected and flagged in the data stream, allowing the decoders to mask the error and recover without system intervention.

Video Decoder

The video decoder is compliant with ISO/IEC 13818-2 Main Profile at Main Level, and the European DVB standard is also supported.

Horizontal and vertical filters deliver high quality video. Pan and scan are supported with 1/16 pel accuracy, and PTS filtering is programmable. A sophisticated transport mechanism supports error concealment.

The internal processor is the central point of control for the video decoder. It interacts with the host processor through the host interface to process high level commands and report status changes. Internally, the video decoder's processor interacts with a Huffman decoder (Variable Length Code Decoder (VLCD)), Inverse Quantizer, Inverse Discrete Cosine Transform (IDCT) Unit, and a Motion Compensation Unit.

Video Input

Elementary Streams (ES) and Packetized Elementary Streams (PES) are decoded at speeds up to 15 Mbps sustained data rate.

For source material derived from film, frame rate conversion using 3:2 pulldown is supported. The MPEG-2 Pan Scan feature is supported which allows conversion of 16:9 aspect ratio images to conventional 4:3 aspect ratio displays.

The host data bus is used to input compressed audio and video data when a transport stream is not used.

Supported Input Image Sizes

Size	Aspect Ratio	Format
352 x 240 (288)	4:3	NTSC(PAL)
352 x 480 (576)	4:3	NTSC(PAL)
480 x 480 (576)	4:3	NTSC(PAL)
544 x 480 (576)	4:3	NTSC(PAL)
720 x 480 (576)	16:9	pan and scan in NTSC(PAL)
544 x 480 (576)	16:9	pan and scan in NTSC(PAL)
480 x480 (576)	16:9	pan and scan in NTSC(PAL)
352 x 240 (288)	16:9	pan and scan in NTSC(PAL)
352 x 480 (576)	16:9	pan and scan in NTSC(PAL)

Synchronization

The video decoder synchronizes video stream decoding to the STC, which is set by the host processor. The decoder compares PTS with the STC and, if the difference exceeds tolerance settings, the current decoded picture will either be repeated or the next B-frame will be skipped to recover synchronization. If a B-frame is not available, synchronization is accomplished by skipping a P-frame.

On-Screen Display (OSD) and Output Interface

A versatile OSD enhances the user's ability to control video decoding. It includes a multi-region link list with a color table for each region. Advanced features of the OSD include block copying, overlay and video blending, video shading (in OSD area), and animation support. OSD supports Professional Profile Display sizes up to 512 lines NTSC, 608 lines for PAL.

OSD supports Direct color (16 bits per pixel bitmap) resolution.

Through the OSD, the resolution of each region of the bitmap can be programmed separately, with the following options:

- 2 bits/pixel pair
- 2 bits/pixel
- 4 bits/pixel pair
- 4 bits/pixel
- 8 bits/pixel pair
- 8 bits/pixel

The output interface supports three sync modes: composite blanking with field ID, H/V Sync and CCIR 656 Master Mode. Signal polarity is programmable. The pixel data bus can be 8 or 16 bits.

Memory Interface

The Memory Interface is based on a 16-bit bus, and is designed to use either 16 or 64 Mb, 125 MHz SDRAM, for a 4- or 8-MB configuration.

Audio Decoder

The device contains an audio decoder which is configured by the host processor through its own set of host-accessible registers.

The audio decoder in the IBM STB13010 device can perform Dolby Digital decoding as well as MPEG decoding. The IBM STB13000 device has no Dolby Digital capabilities.

Audio Input

The audio decoder receives and decodes either PES (Packetized Elementary Stream) or ES (Elementary Stream) audio data via a 20-bit Digital Signal Processor (DSP) engine. Compressed audio data can be received from the audio PID in the transport stream through the transport demultiplexer or through the host data bus as a PES or ES Stream. Input bit rate is supported up to 640 Kbps.

The audio DSP is a 20-bit computational engine which decodes the audio MPEG and Dolby Digital bitstreams, and formats PCM data for playback. PCM playback, and the MPEG and Dolby Digital algorithms, are executed via microcode downloaded through the Host Interface.

Tone Generation

The audio decoder is capable of generating a specified tone frequency with a duration from 0.1 second to three seconds. The user may select from 128 possible tones, 31 durations and eight attenuations. Tones cover 10 octaves of American Standard pitch (“A” = 440 Hz). Audio attenuation is performed in 64 steps with smooth transitions between steps.

Audio Output

The audio decoder supports the playback of either 16-, 18-, or 20-bit unformatted PCM bitstreams. Six sampling frequencies (16, 22.05, 24, 32, 44.1, and 48 kHz) are supported for unformatted PCM bitstreams. Both one channel (mono) and two channel (stereo) output is supported for MPEG decoding and PCM inputs, while up to six channels are possible for Dolby Digital decoding.

The interface can be programmed to support the I^2S mode, the Left Justified mode, or the Right Justified mode. To maximize compatibility with a wide variety of audio DACs, the Audio CLK signal can be programmed to 64 times the sampling clock to support the 20-bit output sample, or 32 times to support the 16-bit output sample.

In addition to the PCM output, a S/PDIF (IEC958) interface is provided. This interface can either output encoded Dolby Digital data while decoding a Dolby Digital stream, or one of three pairs of channels of PCM data.

Synchronization

The audio decoder synchronizes the decoding of the audio stream to the STC, which is set by the host processor by comparing PTS with the STC. If the difference exceeds tolerance settings, the decoder skips or repeats samples. Audio synchronization can be disabled.

Audio / video synchronization is supported with PTS/STC comparison on each audio frame. There is a built-in phase-locked-loop to provide the audio clocks for audio and video synchronization.

Error Checking

Errors are checked and concealed to ensure high quality audio. MPEG error checking uses frame-size calculations for each frame. Audio bitstream error concealment is performed, either by sample repeats or muting, due to loss of Audio Frame synchronization or detection of CRC errors.

Dolby Digital (IBM STB13010 only)

The IBM STB13010 device is fully compatible with Dolby Digital. This device can decode Dolby Digital input, and can output three audio data out signals to support the six channels in Dolby Digital. An S/PDIF output is also available for either two channels of decoded data or output of the Dolby Digital stream.

Additionally, Dolby Digital Karaoke mode and Dolby Digital Surround mode (DSMOD) are supported. DSMOD pins interface to external surround mode circuitry.

Support is also provided for several downmix combinations, dialog normalization, and dynamic range control.

Pin and Signal Information

In the following tables the use of overbars, for example $\overline{\text{RESET}}$, designates signals that are active low. All signals with no overbar are assumed to be active high.

Pin Descriptions

Signal Name	Description	Pin Type
27 MHz CLK	27 MHz Clock	Input
64MBIT_A1	64MBIT_A11	Output
64MBIT_BA1	64MBIT_BA1	Output
AUD CLK	Audio Clock	Output
AUD DAC CLK	Audio DAC Clock	Output
AUD DATA(n)	Audio Data Out(n)	Output
AUD DEEMPHASIS(n)	Audio Deemphasis(n)	Output
AUD DSURMOD(n)	Audio Dolby Sur Mode(n)	Output
AUD L/R	Audio Left / Right	Output
AUD REQ	Audio Data Request	Output
AUD SPDIF	Audio S/PDIF	Output
$\overline{\text{AUD STROBE}}$	Audio Compressed Data Strobe	Input
BA0	BA0	Output
$\overline{\text{CAS}}$	Column Address Select	Output
CKE	SDRAM Clock Enable	Output
CLK	SDRAM Clock	Output
CREF	Video Clock Reference	Output
$\overline{\text{CS}}$	Chip Select	Input
$\overline{\text{CS0}}$	SDRAM Chip Select 0	Output
$\overline{\text{CS1}}$	SDRAM Chip Select 1	Output
DTACK MODE	Dtack Mode	Input
GND	Ground	Ground
HOST ADDR(n)	Host Address Bus(n)	Input
HOST DATA(n)	Host Data Bus(n)	Bi-directional
HSC	Horizontal Sync Control	Input
IRQ	Interrupt Request	Output
LDQM	SDRAM LDQM	Output
LOW WORD	Low Word	Input

Pin Descriptions

Signal Name	Description	Pin Type
MA(n)	Memory Address(n)	Output
MD(n)	Memory Data(n)	Bi-directional
N/C	No Connect	No Connect
$\overline{OE}$	Output Enable	Input
OSC SEL	OSC Select	Input
PIXEL DATA(n)	Pixel Data(n)	Output
$\overline{RAS}$	Row Address Select	Output
RD/$\overline{WR}$	Read / Write	Input
READY	Ready	Output
$\overline{RESET}$	Reset	Input
STC 27 MHz CLK	STC 27 MHz CLK	Input
TTX DATA	Teletext Data	Output
TTX DATA REQ	Teletext Data Request	Input
UDQM	SDRAM UDQM	Output
V_{DD}	Voltage (3.3 V)	Power
V_{DDA1}	Voltage (2.5 V)	Power
V_{DDA2}	Voltage (2.5 V)	Power
VID REQ	Video Data Request	Output
$\overline{VID\ STROBE}$	Video Compressed Data Strobe	Input
VSC	Vertical Sync Control	Input
$\overline{WE}$	Write Enable	Output
$\overline{WP}$	Write Pulse	Input
XPORT CLK	Transport Stream Data Clock	Input
XPORT DATA(n)	Transport Data In(n)	Input
XPORT ERROR	Transport Error	Input
$\overline{XPORT\ PWM}$	Transport PWM	Output
XPORT START	Transport Start	Input
XPORT VALID	Transport Data Valid	Input

Pin Assignments, Sorted by Signal Name

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
27 MHz CLK	42	CLK	8	GND	201
64MBIT_A1	21	CREF	178	GND	202
64MBIT_BA1	20	$\overline{CS}$	78	GND	205
AUD CLK	131	$\overline{CS0}$	15	GND	208
$\overline{AUD\ STROBE}$	85	$\overline{CS1}$	16	HSC	181
AUD DAC CLK	132	DTACK MODE	185	HOST ADDR 0	60
AUD DATA 0	142	GND	2	HOST ADDR 1	62
AUD DATA 1	143	GND	11	HOST ADDR 2	63
AUD DATA 2	145	GND	24	HOST ADDR 3	64
AUD REQ	75	GND	31	HOST ADDR 4	65
AUD DEEMPHASIS 0	141	GND	41	HOST ADDR 5	66
AUD DEEMPHASIS 1	140	GND	52	HOST ADDR 6	71
AUD DSURMOD 0	137	GND	54	HOST ADDR 7	72
AUD DSURMOD 1	136	GND	61	HOST DATA 0	89
AUD L/R	133	GND	76	HOST DATA 1	92
AUD SPDIF	135	GND	90	HOST DATA 2	93
N/C	116	GND	104	HOST DATA 3	95
N/C	119	GND	106	HOST DATA 4	96
N/C	130	GND	114	HOST DATA 5	98
N/C	129	GND	117	HOST DATA 6	99
N/C	127	GND	128	HOST DATA 7	100
N/C	77	GND	138	HOST DATA 8	102
N/C	126	GND	149	HOST DATA 9	107
N/C	125	GND	156	HOST DATA 10	108
N/C	124	GND	158	HOST DATA 11	109
N/C	122	GND	169	HOST DATA 12	110
N/C	120	GND	180	HOST DATA 13	112
N/C	121	GND	183	HOST DATA 14	113
BA0	19	GND	190	HOST DATA 15	115
$\overline{CAS}$	12	GND	193	IRQ	73
CKE	9	GND	198	LDQM	6

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
LOW WORD	87	N/C	195	V_{DD}	14
MA2	22	$\overline{OE}$	88	V_{DD}	17
MA3	23	OSC SEL	70	V_{DD}	18
MA4	25	PIXEL DATA 0	146	V_{DD}	30
MA5	26	PIXEL DATA 1	147	V_{DD}	33
MA6	27	PIXEL DATA 2	148	V_{DD}	39
MA7	28	PIXEL DATA 3	150	V_{DD}	51
MA8	29	PIXEL DATA 4	151	V_{DD}	53
MA9	34	PIXEL DATA 5	152	V_{DD}	67
MA10	36	PIXEL DATA 6	154	V_{DD}	69
MA11	37	PIXEL DATA 7	159	V_{DD}	82
MA12	38	PIXEL DATA 8	160	V_{DD}	84
MD0	176	PIXEL DATA 9	161	V_{DD}	86
MD1	177	PIXEL DATA 10	162	V_{DD}	91
MD2	187	PIXEL DATA 11	164	V_{DD}	94
MD3	188	PIXEL DATA 12	165	V_{DD}	97
MD4	189	PIXEL DATA 13	167	V_{DD}	101
MD5	191	PIXEL DATA 14	168	V_{DD}	103
MD6	192	PIXEL DATA 15	170	V_{DD}	105
MD7	194	RD/$\overline{WR}$	79	V_{DD}	111
MD8	197	$\overline{RAS}$	13	V_{DD}	123
MD9	199	READY	81	V_{DD}	134
MD10	200	$\overline{RESET}$	35	V_{DD}	144
MD11	203	STC 27 MHz CLK	139	V_{DD}	153
MD12	204	TTX DATA	182	V_{DD}	155
MD13	206	TTX DATA REQ	179	V_{DD}	157
MD14	3	UDQM	5	V_{DD}	163
MD 15	4	VID REQ	74	V_{DD}	166
N/C	44	$\overline{VID\ STROBE}$	83	V_{DD}	172
N/C	68	V_{DD}	1	V_{DD}	174
N/C	118	V_{DD}	7	V_{DD}	175

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
V_{DD}	186	$\overline{WP}$	80	XPORT DATA 6	58
V_{DD}	196	XPORT CLK	40	XPORT DATA 7	59
V_{DD}	207	XPORT DATA 0	48	XPORT ERROR	43
V_{DDA1}	32	XPORT DATA 1	49	$\overline{XPORT\ PWM}$	47
V_{DDA2}	173	XPORT DATA 2	50	XPORT START	46
V_{DDA2}	184	XPORT DATA 3	55	XPORT VALID	45
VSC	171	XPORT DATA 4	56		
$\overline{WE}$	10	XPORT DATA 5	57		

Pin Assignments, Sorted by Pin Number

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1	V_{DD}	31	GND	61	GND
2	GND	32	V_{DDA1}	62	HOST ADDR 1
3	MD14	33	V_{DD}	63	HOST ADDR 2
4	MD 15	34	MA9	64	HOST ADDR 3
5	UDQM	35	$\overline{\text{RESET}}$	65	HOST ADDR 4
6	LDQM	36	MA10	66	HOST ADDR 5
7	V_{DD}	37	MA11	67	V_{DD}
8	CLK	38	MA12	68	N/C
9	CKE	39	V_{DD}	69	V_{DD}
10	$\overline{\text{WE}}$	40	XPORT CLK	70	OSC SEL
11	GND	41	GND	71	HOST ADDR 6
12	$\overline{\text{CAS}}$	42	27 MHz CLK	72	HOST ADDR 7
13	$\overline{\text{RAS}}$	43	XPORT ERROR	73	IRQ
14	V_{DD}	44	N/C	74	VID REQ
15	$\overline{\text{CS0}}$	45	XPORT VALID	75	AUD REQ
16	$\overline{\text{CS1}}$	46	XPORT START	76	GND
17	V_{DD}	47	$\overline{\text{XPORT PWM}}$	77	N/C
18	V_{DD}	48	XPORT DATA 0	78	$\overline{\text{CS}}$
19	BA0	49	XPORT DATA 1	79	RD/$\overline{\text{WR}}$
20	64MBIT_BA1	50	XPORT DATA 2	80	$\overline{\text{WP}}$
21	64MBIT_A1	51	V_{DD}	81	READY
22	MA2	52	GND	82	V_{DD}
23	MA3	53	V_{DD}	83	$\overline{\text{VID STROBE}}$
24	GND	54	GND	84	V_{DD}
25	MA4	55	XPORT DATA 3	85	$\overline{\text{AUD STROBE}}$
26	MA5	56	XPORT DATA 4	86	N/C
27	MA6	57	XPORT DATA 5	87	LOW WORD
28	MA7	58	XPORT DATA 6	88	$\overline{\text{OE}}$
29	MA8	59	XPORT DATA 7	89	HOST DATA 0
30	V_{DD}	60	HOST ADDR 0	90	GND

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
91	V_{DD}	121	N/C	151	PIXEL DATA 4
92	HOST DATA 1	122	N/C	152	PIXEL DATA 5
93	HOST DATA 2	123	V_{DD}	153	V_{DD}
94	V_{DD}	124	N/C	154	PIXEL DATA 6
95	HOST DATA 3	125	N/C	155	V_{DD}
96	HOST DATA 4	126	N/C	156	GND
97	V_{DD}	127	N/C	157	V_{DD}
98	HOST DATA 5	128	GND	158	GND
99	HOST DATA 6	129	N/C	159	PIXEL DATA 7
100	HOST DATA 7	130	N/C	160	PIXEL DATA 8
101	V_{DD}	131	AUD CLK	161	PIXEL DATA 9
102	HOST DATA 8	132	AUD DAC CLK	162	PIXEL DATA 10
103	V_{DD}	133	AUD L/R	163	V_{DD}
104	GND	134	V_{DD}	164	PIXEL DATA 11
105	V_{DD}	135	AUD SPDIF	165	PIXEL DATA 12
106	GND	136	AUD DSURMOD 1	166	V_{DD}
107	HOST DATA 9	137	AUD DSURMOD 0	167	PIXEL DATA 13
108	HOST DATA 10	138	GND	168	PIXEL DATA 14
109	HOST DATA 11	139	STC 27 MHz CLK	169	GND
110	HOST DATA 12	140	AUD DEEMPHASIS 1	170	PIXEL DATA 15
111	V_{DD}	141	AUD DEEMPHASIS 0	171	VSC
112	HOST DATA 13	142	AUD DATA 0	172	V_{DD}
113	HOST DATA 14	143	AUD DATA 1	173	V_{DDA2}
114	GND	144	V_{DD}	174	V_{DD}
115	HOST DATA 15	145	AUD DATA 2	175	V_{DD}
116	N/C	146	PIXEL DATA 0	176	MD 0
117	GND	147	PIXEL DATA 1	177	MD 1
118	N/C	148	PIXEL DATA 2	178	CREF
119	N/C	149	GND	179	TTX DATA REQ
120	N/C	150	PIXEL DATA 3	180	GND

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
181	HSC	191	MD 5	200	MD 10
182	TTX DATA	192	MD 6	201	GND
183	GND	193	GND	202	GND
184	V_{DDA2}	194	MD 7	203	MD 11
185	DTACK MODE	195	N/C	204	MD 12
186	V_{DD}	196	V_{DD}	205	GND
187	MD 2	197	MD 8	206	MD 13
188	MD 3	198	GND	207	V_{DD}
189	MD 4	199	MD 9	208	GND
190	GND				

Electrical Information

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Supply Voltage (3.3 V)	3.80	V	1
V_{DDA1}	Supply Voltage (2.5 V)	2.70	V	1
V_{DDA2}	Supply Voltage (2.5 V)	2.70	V	1
T_A	Ambient operating temperature range	70	°C	1, 2
T_S	Storage temperature range	150	°C	1, 3
P_D	Power Dissipation	1	W	

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Operating temperature range is based on ambient air temperature with natural convection.
3. Storage temperature range is guaranteed for up to 100 worst case cycles.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{DD}	Supply Voltage (3.3 V)		3.14	3.3	3.47	V
V_{DDA1}	Supply Voltage (2.5 V)		2.38	2.5	2.63	V
V_{DDA2}	Supply Voltage (2.5 V)		2.38	2.5	2.63	V
I_{CC}	Supply Current	3.3 V		250		mA
		2.5 V		80		mA
T_A	Ambient operating temperature range		0		70	°C
T_S	Storage temperature range		-65		150	°C

Current Specifications

Symbol	Parameter	RAS/CAS/ Host Data	All other drivers	Units	Notes
I_{SINK}(DC)	Sink Current	8.0	6.0	mA	1
I_{SOURCE}(DC)	Source Current	12.0	9.0	mA	2

1. I_{SINK} is measured at 0.4 V
2. I_{SOURCE} is measured at 2.4 V

DC Electrical Characteristics

Usage	MAUL	MPUL	LPUL	MPDL	LPDL	MADL	Units
3.3 V LVTTL Receiver	3.80	3.30	2.00	0.80	0.00	-0.60	V
3.3 V LVTTL Driver	3.80	3.30	2.40	0.40	0.00	-0.60	V

Definitions
MAUL: Maximum Allowable Up Level
MPUL: Maximum Positive Up Level
LPUL: Least Positive Up Level
MPDL: Maximum Positive Down Level
LPDL: Least Positive Down Level
MADL: Minimum Allowable Down Level

Revision Log

Revision	Contents of Modification
Feb. 2000	First release date .(Revision 00).
June 30, 2000	Various updates. (Revision 01).
July 12, 2000	Minor updates. (Revision 02).
July 20, 2000	Various Updates to footers and formats for consistancy.(Revision 03).
July 26, 2000	Minor Corrections to Pin Descriptions Tables. (Revision 04).
Sept. 7, 2000	Minor corrections to formats. (Revision 05).

Note: This document contains information on products in the design, sampling and/or initial production phases of development. This information is subject to change without notice. Verify with your IBM field applications engineer that you have the latest version of this document before finalizing a design.

Copyright and Disclaimer

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6351

The IBM home page can be found at http://www.ibm.com

The IBM Microelectronics Division home page can be found at http://www.chips.ibm.com

STB130x0_sds_080900.fm.05
Sept. 7, 2000