# CEM4204

## N-Channel Enhancement Mode Field Effect Transistor

## FEATURES

■ 40V, 7.3A, $R_{DS(ON)}$ = 28mΩ @$V_{GS}$ = 10V.

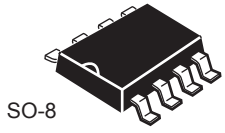
$R_{DS(ON)}$ = 42mΩ @$V_{GS}$ = 4.5V.

■ Super high dense cell design for extremely low $R_{DS(ON)}$.

■ High power and current handing capability.

■ Lead free product is acquired.

■ Surface mount Package.



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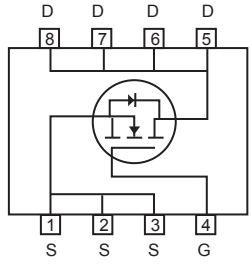


## ABSOLUTE MAXIMUM RATINGS $T_A$ = 25°C unless otherwise noted

| Parameter | Symbol | Limit | Units |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 40 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | V |
| Drain Current-Continuous | $I_D$ | 7.3 | A |
| Drain Current-Pulsed [a] | $I_{DM}$ | 25 | A |
| Maximum Power Dissipation | $P_D$ | 2.5 | W |
| Operating and Store Temperature Range | $T_J$,$T_{stg}$ | -55 to 150 | °C |

## Thermal Characteristics

| Parameter | Symbol | Limit | Units |
|---|---|---|---|
| Thermal Resistance, Junction-to-Ambient [b] | $R_{\theta JA}$ | 50 | °C/W |

## Electrical Characteristics $T_C$ = 25°C unless otherwise noted

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$ = 0V, $I_D$ = 250μA | 40 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 32V, $V_{GS}$ = 0V | | | 1 | μA |
| Gate Body Leakage Current, Forward | $I_{GSSF}$ | $V_{GS}$ = 20V, $V_{DS}$ = 0V | | | 100 | nA |
| Gate Body Leakage Current, Reverse | $I_{GSSR}$ | $V_{GS}$ = -20V, $V_{DS}$ = 0V | | | -100 | nA |
| **On Characteristics** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250μA | 1 | | 3 | V |
| Static Drain-Source On-Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10V, $I_D$ = 6A | | 22 | 28 | mΩ |
| | | $V_{GS}$ = 4.5V, $I_D$ = 3A | | 32 | 42 | mΩ |
| **Dynamic Characteristics** [c] | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 20V, $V_{GS}$ = 0V, f = 1.0 MHz | | 590 | | pF |
| Output Capacitance | $C_{oss}$ | | | 90 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 60 | | pF |
| **Switching Characteristics** [c] | | | | | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 20V, $I_D$ = 6A, $V_{GS}$ = 10V, $R_{GEN}$ = 3Ω | | 10 | 20 | ns |
| Turn-On Rise Time | $t_r$ | | | 3 | 6 | ns |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 26 | 52 | ns |
| Turn-Off Fall Time | $t_f$ | | | 4 | 8 | ns |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 20V, $I_D$ = 6A, $V_{GS}$ = 10V | | 13 | 16.9 | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 1.7 | | nC |
| Gate-Drain Charge | $Q_{gd}$ | | | 3.5 | | nC |
| **Drain-Source Diode Characteristics and Maximun Ratings** | | | | | | |
| Drain-Source Diode Forward Current | $I_S$ | | | | 7.3 | A |
| Drain-Source Diode Forward Voltage [b] | $V_{SD}$ | $V_{GS}$ = 0V, $I_S$ = 1A | | | 1.2 | V |

**Notes :**
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
c.Guaranteed by design, not subject to production testing.

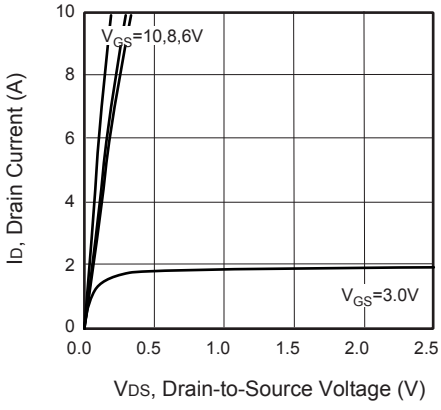


**Figure 1. Output Characteristics**

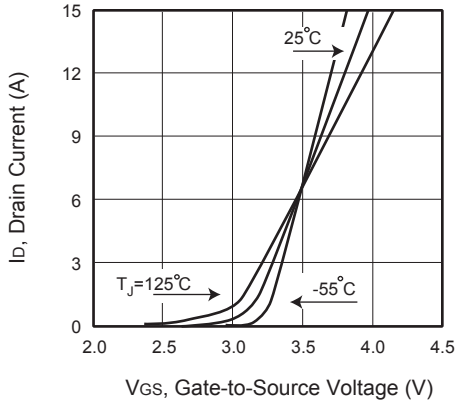


**Figure 2. Transfer Characteristics**

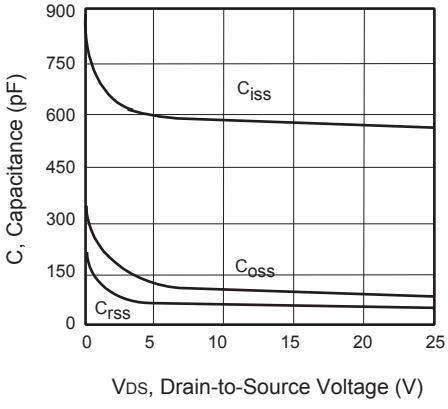


**Figure 3. Capacitance**

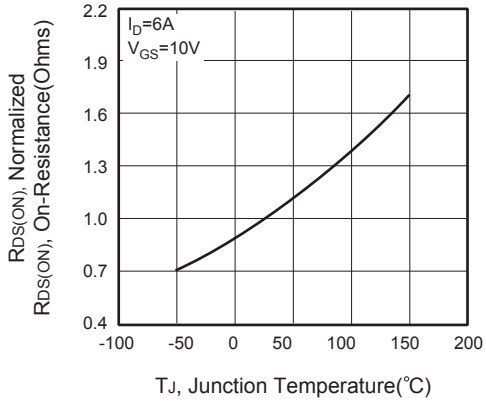


**Figure 4. On-Resistance Variation with Temperature**

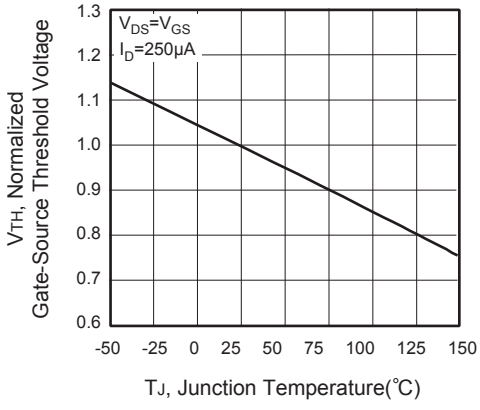


**Figure 5. Gate Threshold Variation with Temperature**

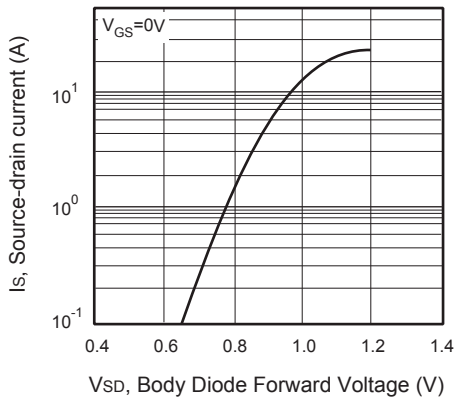


**Figure 6. Body Diode Forward Voltage Variation with Source Current**

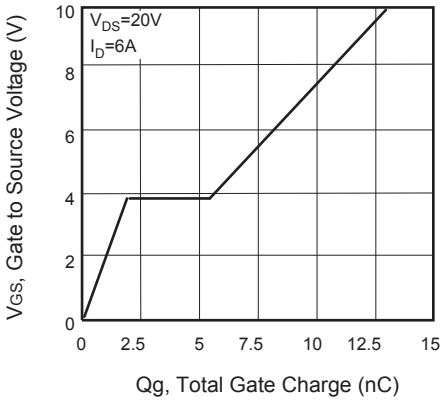


**Figure 7. Gate Charge**

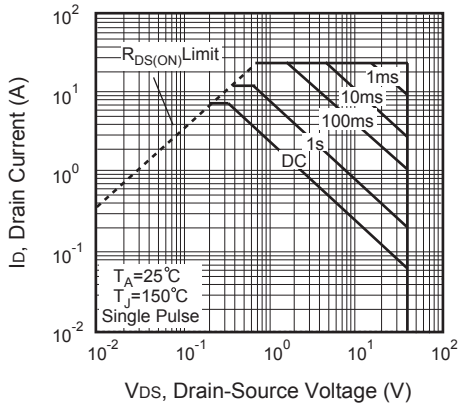


**Figure 8. Maximum Safe Operating Area**

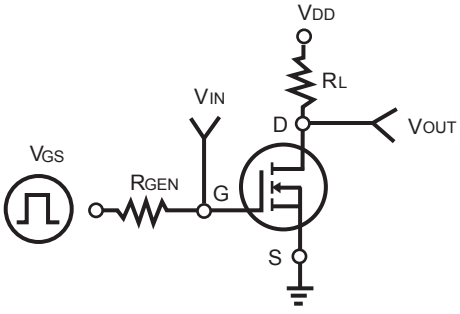


**Figure 9. Switching Test Circuit**

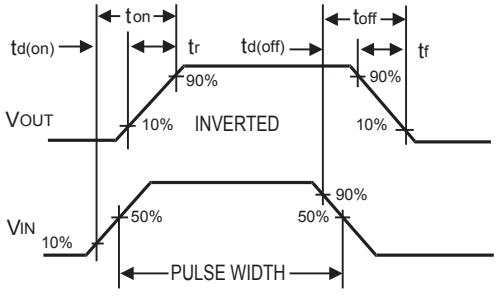


**Figure 10. Switching Waveforms**

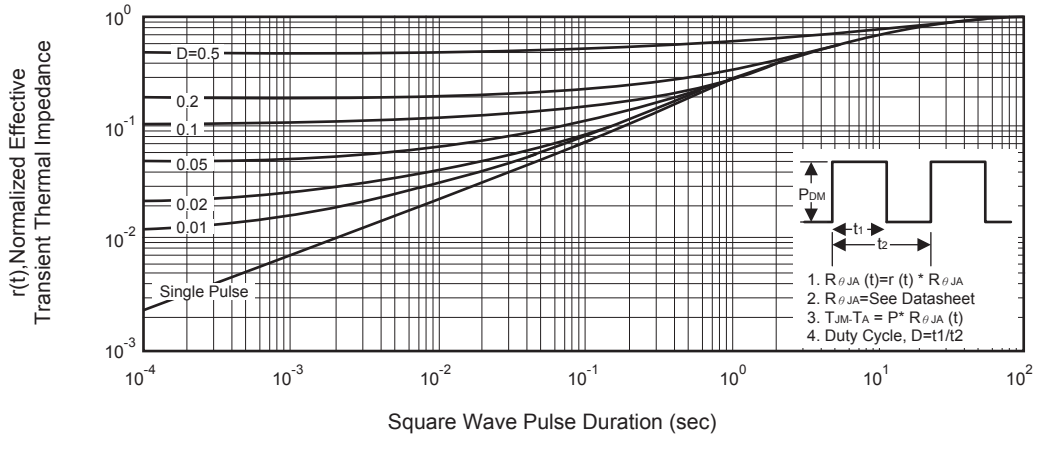


**Figure 11. Normalized Thermal Transient Impedance Curve**